Process Development And Characterization Of The Stencil Printing Process For Small Apertures

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Abstract
The consumer's interest for smaller, lighter and higher performance electronics products has increased the use of ultra fine pitch packages, such as Flip Chips and Chip Scale Packages, in printed circuit board (PCB) assembly. The assembly processes for these ultra fine pitch packages are extremely complex and each step in the assembly process influences the assembly yield and reliability.

Generally speaking, end-of-line SMT defects can be greatly influenced by the stencil printing operation. The importance of the stencil printing process progressively increases as the pitch and the package size decreases. A thorough understanding of basic stencil printing principles would facilitate the design of printers, stencils and pastes, and would ultimately permit the extension of reliable print techniques to the ultra fine print arena.

Stencil design and stencil fabrication techniques are critical factors that affect the stencil printing process. This work compares the stencil design elements, such as aperture wall taper and aperture wall finish that play a major role in the print performance of the small apertures. Designed experiments are performed to determine the 'optimum' level of aperture taper and aperture wall finish. The study also compares three major stencil-manufacturing techniques (chemical etching, laser cutting and electroforming) for small aperture printing. From the knowledge gathered, guidelines are being developed for the stencil design and the stencil printing process for small apertures.

Introduction
The need for more reliable, lighter and smaller products has increased the use of Flip Chip (FC's), Chip Scale Packages (CSP's), Micro-BGA (BGA™), and 0201s in the electronics industry. Aside from the newer 01005 components that are starting to receive attention, the aforementioned components are widely used in cellular phones, personal digital assistants (PDAs), camcorders, etc., where reliability is of main concern[1]. The quality of the solder joints affects the reliability of these packages, especially where they are subjected to very harsh conditions. Stencil printing is the most common method for depositing solder for these packages (e.g., CSP, BGA)[2]. The use of ultra fine pitch packages makes the stencil printing process more critical to produce a reliable solder joint. For fine pitch packages, solder paste volume and consistency are critical to solder joint reliability. The process becomes more challenging when the combination of paste rheology and stencil geometry causes inadequate or inconsistent solder paste transfer.

The volume of solder paste deposited on their pads affects the reliability of Flip Chip, CSP and BGA packages[3,4]. For Flip Chip and CSP packages, the standoff from the board has been determined to be an important parameter for predicting long term solder joint reliability with pad size and solder volume being the primary factors that influence the standoff[5,6]. Therefore, it is important to maximize the volume of solder paste deposited and increase the reliability of these packages.

This research focuses on the characterization and optimization of the stencil printing process for ultra fine pitch packages to understand the stencil printing process through experimentation and technical approaches. In so doing, this work compares the stencil design elements, such as aperture wall taper and aperture wall finish that play a major role in the print performance of the small apertures. Designed experiments are performed to determine the 'optimum' level of aperture taper and aperture wall finish. The study also compares three major stencil-manufacturing techniques (chemical etching, laser cutting and electroforming) for small aperture printing.

Problem Statement and Research Objective
The various stencil design elements that affect the solder paste release are aperture size, aperture shape, aperture wall taper and wall finish[6]. While these elements are widely considered to be of importance, there is not a well-known supply of data that shows the interaction between the aperture taper and the wall surface finish. In this research work, an attempt has been made to study the effect of these stencil design elements on paste transfer efficiency for small apertures.

The primary objective of this study is to develop an optimal stencil printing process for ultra fine pitch apertures. An effort is made to compare the stencil design elements, such as wall taper and aperture wall finish, in a single print stroke. The comparisons of these parameters in a single print stroke reduce the variability of the printing process. Sub-objectives that are studied to help achieve the primary objective are listed below:

- Develop a stencil with a test pattern that will enable comparison of print performance with different levels of taper and electropolish on transfer efficiency for Flip Chips, CSPs and 0201s.
- Gage repeatability and reproducibility study for the stencil aperture measurements and solder paste measurements. Comprehensive GR&R studies were performed on all of the analytical equipment used in this study prior to carrying out the experimentation and can be found elsewhere[7]. Due to size restrictions, the GR&R analysis are not included herein.
- Using design of experiments (DOE), determine optimal printing parameters while considering different levels of taper and electropolish.
- Comparison of the effects of different levels of taper and electropolish on the aperture transfer efficiencies at the optimal printing parameters.

Research Methodology

An example of the test vehicles used in this study is shown in Figure 1**.** The test vehicles are 10 inches x 13 inches x 0.062 inches, bare copper boards**.** They have four tooling holes that are used as fiducials for print alignment and contain no pads**.** Since X-Y co-ordinate accuracy of print deposits are not considered in this work, bare copper boards are more than adequate for experimentation purposes. Additional advantages of using the bare copper boards are the following:

- They are very economical as compared to 'real' substrates with pads and circuitry.
- They provide optimum reference points for height measurements with the 3-D laser paste inspection system. i.e., variations in pad height on a 'real' substrate are eliminated from study.
- They are easier for visual inspection.
- They have reduced gasketing problems.
- They are easier to clean and reuse providing another economic benefit.

Figure 1. Test Vehicle - Bare Copper Board

Stencil Design

Stencil design is a very important factor affecting the volume of paste deposited. Print volume and consistency for fine pitch components like FC, CSP, BGA and 0201 components could be maximized by carefully choosing the stencil design parameters. Many CSP pitches lie in the range of 7.87 mils to 19.68 mils with pad sizes ranging from 8 to 16 mils[3,8]. A stencil thickness of 5 mils is standard for CSP, BGA, 0201 and other SMT components[9]. A reduction in stencil thickness to 4 mils would help in increasing the transfer efficiency; however, this would decrease the volume of paste deposited, which ultimately affects the reliability of the solder joints. Therefore, a stencil thickness of 5 mils was chosen for the study. We do realize that moving to 01005 components may need a thinner stencil.

To determine the best combination of taper and electropolish, test stencils were designed with the following geometries: circle, square, home plate, rectangle (5:1) and oblong (5:1). However, only circular apertures were chosen for this study as they are used for printing of CSPs, BGAs and 0201 components. Three levels of taper – low, medium and high and four

levels of electropolish – no polish, low polish, medium polish and high polish were used in this study. The test matrix consisted of 12 cells as shown in Figure 2, with different combinations of tapers and electropolish levels. The aperture sizes used in the study were 12 mils, 10 mils, 8 mils, 6 mils and 4 mils. Since, 4 mil apertures provided issues with volume measurements and poor print performance, they were omitted from the later part of the study.

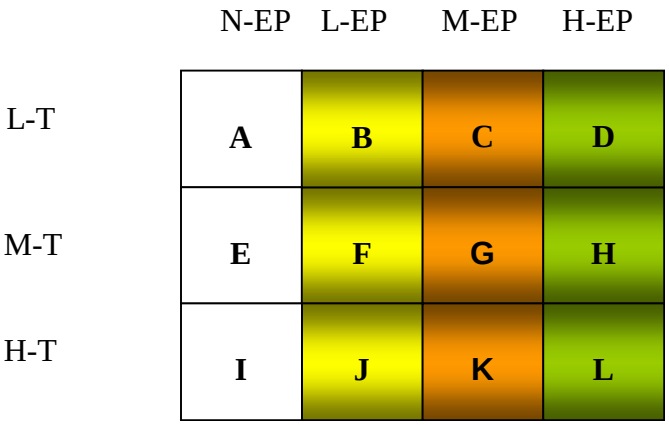

Figure 2. Layout of Test Stencil

Legend:
Taper: L-T: Low Taper, M-T: Medium Taper, H-T: High Taper;
Electropolish: N-EP: No Electropolish, L-EP: Low Electropolish, M-EP: Medium Electropolish, H-EP: High Electropolish

Each cell consisted of 14 circles for each size. The total number of apertures on the stencil, considering all sizes and shapes, was9408. The total number of apertures considered in this work (circles only) was 840. These aperture sizes and shapes cover most stencil printing scenarios for FC, CSP, BGA and 0201 applications. Each individual aperture used in the study was measured for size and taper using an optical coordinate measuring machine. Actual volume for each aperture was calculated using these measurements. Figure 3 shows the layout of apertures in a single cell.

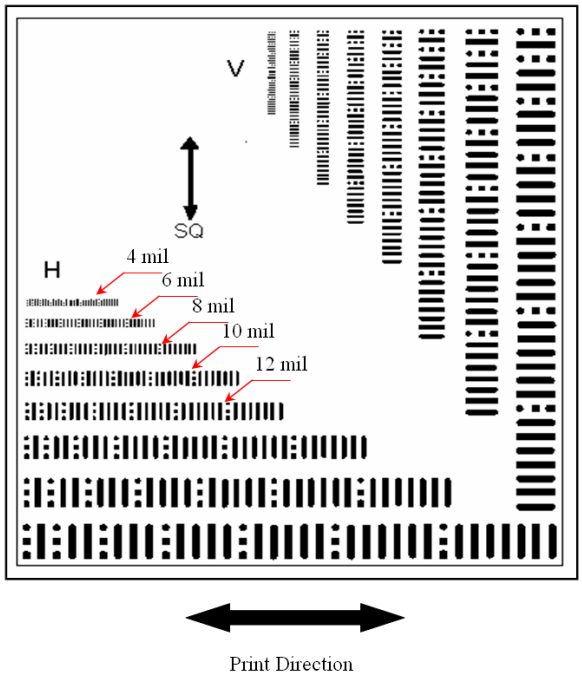

Figure 3. Layout of Apertures in a Cell

Additionally, to compare the different stencil manufacturing techniques in a single print stroke, three stencils were made with a combination of manufacturing methods. Figure 4 shows a layout of all the three stencils used in the study. All the cells in stencil 'A' were manufactured using a laser cut process except Cell D, which was manufactured using a chemical etching process. Stencil 'B' was manufactured using electroforming and laser cutting techniques. Since electropolish was not required for the electroforming process, a total of 9 cells were made using the electroforming process. The last three cells as shown in Figure 4 were made using a laser cutting process. Stencil 'C' was manufactured using chemical etching and a laser cutting process. In the chemical etching process, different levels of etching and different levels of electropolish were used. A total of 9 cells were made using the chemical etching process. A laser cutting process was carried out for 3 cells with different levels of taper.

An important design feature of this experiment wasthe following: These combinations of different stencil manufacturing techniques (twelve combinations on each of the three stencils!) will help to compare the manufacturing methods under a single stroke and largely eliminates the source of variations obtained if using a different stencil for each manufacturing technique. Had a different stencil been used for each combination, then 36 stencils instead of 3 would have been required, thus potentially introducing tremendous variability.

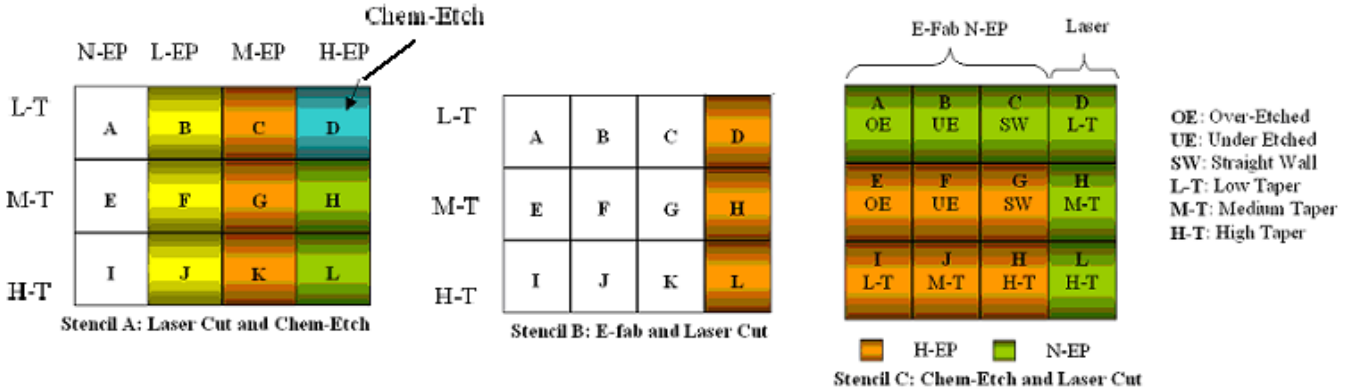

Figure 4. Layouts of Test Stencils, A, B and C

Legend:
Taper: L-T: Low Taper, M-T: Medium Taper, H-T: High Taper;
Electropolish: N-EP: No Electropolish, L-EP: Low Electropolish, M-EP: Medium Electropolish, H-EP: High Electropolish

Solder Paste

A commercially available Type III, no-clean, 63Sn/37Pb solder paste was used throughout the study. The paste had 90% metal loading and a stencil life greater than 8 hrs at 50%RH, 74^{o}F. The primary reason for choosing a Type III paste over Type IV or V was the fact that Type III paste is widely used in today's assembly processes due to cost advantage and readily available body of knowledge.

Experiments Conducted

The following sequence of experiments was used as the methodology for conducting the study:

- Optimization Study – To optimize the factors and determine the best parameter settings for depositing a desired amount of solder paste.
- Validation Study – To verify the performance of the optimized parameter settings.
- Comparison Study – To compare the effect of taper and electropolish on print performance and to compare different stencil manufacturing techniques.

Response Variables

The main purpose of the study was to optimize the parameters that affect the solder paste volume deposition over a variety of different apertures. The response variables chosen for the study were volume of paste deposited, transfer efficiency, and ratio of standard deviation to volume. The volumes were measured using a GSI SVS 8200.

Optimization Study

A Central Composite Design (CCD) with two factors was used for the optimization of print speed and print pressure. The design was blocked by stroke direction to eliminate the influence of stroke direction on the print performance. Optimization was carried for 6 to 12 mils circular apertures and used Stencil A, because it represents an industry standard stencil manufacturing method for CSPs, BGAs and 0201s. Additionally, the optimization was performed for the apertures in Cell F, with medium taper and low polish – this cell represents typical taper and electropolish settings used in the industry. The fixed factors and the variable factors associated with the design are listed below:

Fixed Factors:

1. Metal Squeegee	MPM – metal
2. Stencil	5-mil thick (Laser cut)
3. Squeegee Size	8" blade
4. PC Board	Bare Copper Board [0.062 inch thick]
5. Screen Printer	MPM UP3000
6. Snap off speed	Slow snap off (8 mils over 80 mils)
7. Snap off distance	-0.008"
8. Geometry	6, 8, 10 and 12 mil circles

Variable Factors:

	Levels		
Factors	Low	Middle	High
Print Speed	1 in/sec	3.5 in/sec	6 in/sec
Print Pressure	12 lb	18 lb	24 lb

A detailed description of the analysis (including Response Surface Methodology (RSM), Normal Probability Plots, Response Optimizer Plots (in MINITAB), and others) of the optimization study is published elsewhere[7] . Herein, we will summarize the findings: a print speed of 5 in/sec and a print force of 24 lbs was chosen as the optimized parameters. While determining the optimized parameters, more importance was given to hard-to-print apertures such as the 10 mil and 8 mil circles.

Validation Study

The main aim of the validation study was to verify the optimized parameters obtained using the central composite design. To perform the validation study, a total of 30 boards were printed in each print direction. A sample size of 30 was chosen to ensure statistical validity to the analysis. Figure 5 shows the comparison of the predicted and actual transfer efficiency and Figure 6 shows the comparison of the predicted and actual paste volume standard deviation, respectively. The graphs show good agreement between the predicted and actual transfer efficiencies and standard deviation for all geometries and thus confirming the validation of the optimized print parameters.

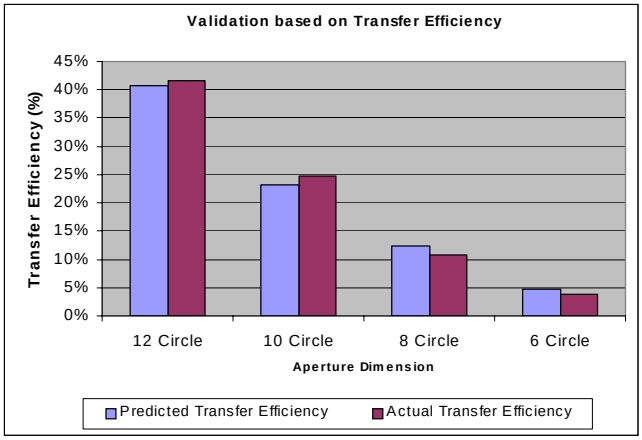

Figure 5. Comparison of Predicted and Actual Transfer Efficiency

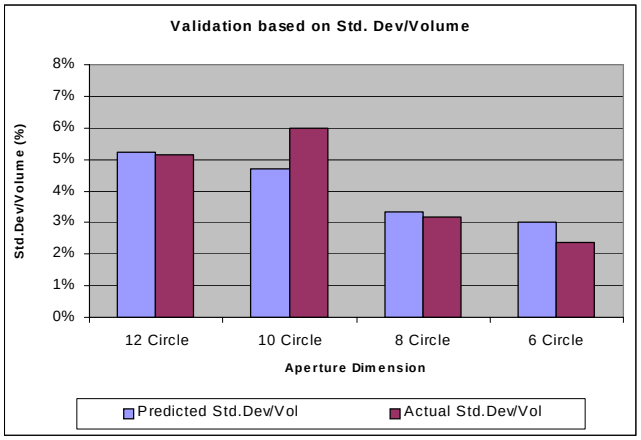

Figure 6. Comparison of Predicted and Actual Standard Deviation/Volume

Comparison Study

Due to the large size of the comparison study[7] a description of the steps undertaken and summary of important findings will be presented here. The main objective of the comparison study was to determine an optimum level of taper and degree of electropolish for the three different manufacturing techniques and to compare the print performance of three different stencil fabrication methods (i.e., Laser cut, E-fab and Chem-etch) for small apertures ranging from 4 to 12 mils. The performances of the stencils were studied based on volume of solder paste deposited, transfer efficiency and standard deviation as a percentage of the volume deposited (Std. dev/Volume). The aperture dimension measurements for E-fab (Stencil B) and Chem-etch (Stencil C) stencils might not reveal the true dimensions of the apertures due to the blooming effect and irregular shapes of the apertures. In order to compensate for this effect, volume of paste deposited on the boards was taken as one of the primary response factors and all the data were analyzed with respect to the volume.

To compare the effect of taper and electropolish, 60 boards were printed with the optimized parameters obtained using the RSM optimization design. A total of 30 boards were printed in each stroke direction and analyses were therefore blocked according to stroke direction to eliminate its influence. The procedure used for the study is represented in the form of a flowchart in Figure 7. The comparison tests were performed at the optimized parameters of print pressure 24 lbs (3 lbs per linear inch) and print speed of 5 in/sec. The same parameters were used for Stencil B and Stencil C. The reason for using the same optimized parameters for Stencil B and Stencil C are due to the same theoretical volume as compared to Stencil A. Therefore, it was assumed that both the stencils (Stencil B and Stencil C) will behave similarly to Stencil A.

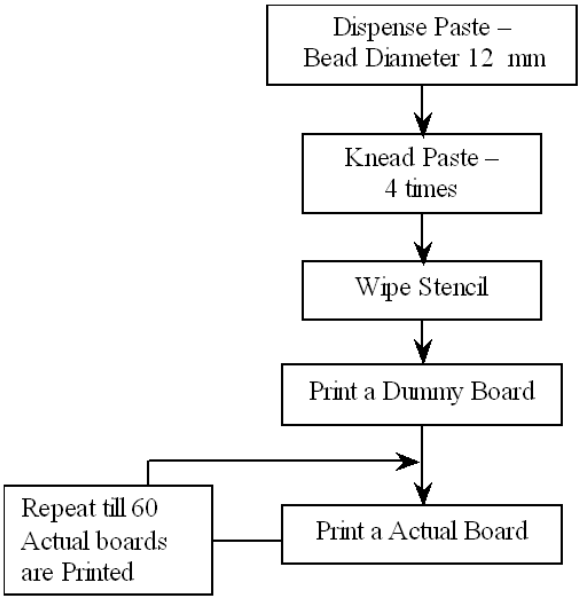

Figure 7. Experimental Procedure for Comparing Stencil Manufacturing Conditions

Additionally, stencil wiping was not performed between the printed boards. A screening test was performed to determine the wiping frequency to eliminate the clogging of the apertures. A total of 100 boards were printed at the optimized parameters without any underside wiping of the stencil. After analyzing the data, there were no drastic changes in the transfer efficiency and standard deviation/mean volume, which indicates that apertures were not clogged even after 100 prints. Figures 8,a-d, shows the plots of transfer efficiency and standard deviation/volume over 100 boards for the various aperture sizes indicate that there were no drastic changes in the transfer efficiency and standard deviation/volume in the absence of underside wiping.

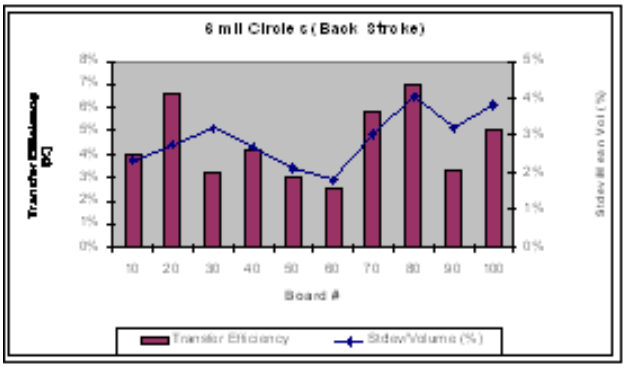

Figure 8a. Transfer efficiency and std.dev/volume for 6 mil Circle

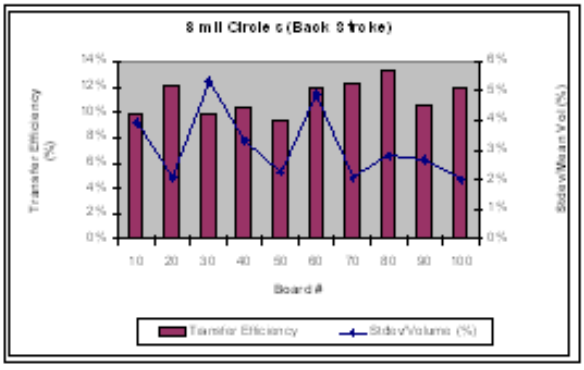

Figure 8b. Transfer efficiency and std.dev/volume for 8 mil Circle

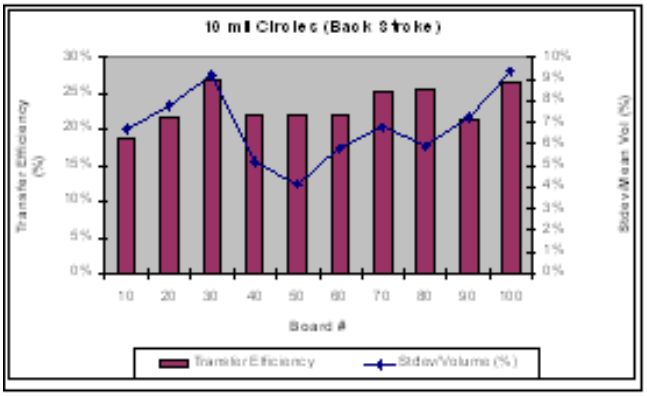

Figure 8c. Transfer efficiency and std.dev/volume for 10 mil Circle

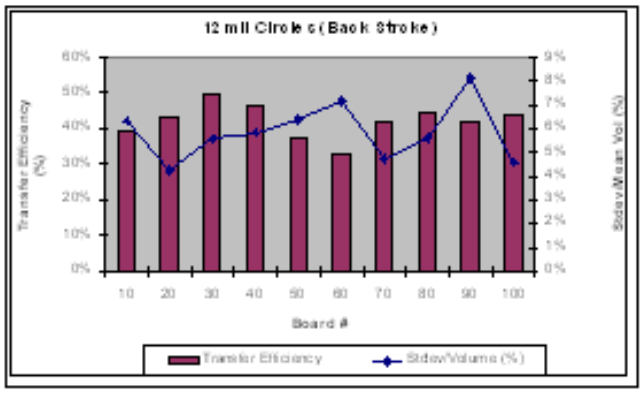

Figure 8d. Transfer efficiency and std.dev/volume for 12 mil Circle

Techniques Utilized for Statistical Comparisons

To determine the optimal combination of taper and electropolish, a multiple comparison test was performed to compare the performance (mean, or average behavior) of the cells on a stencil. In order to perform the multiple comparison tests of means for the different stencil manufacturing conditions, a Tukey's multiple comparison test was used. In performing Tukey's test, the data from one cell are compared, as a group, to the data in another cell. If during this comparison that one cell is shown to be significantly different from another cell, then the analysis can stop at that point and a better performer can be selected. On the other hand, if one group appears to be inseparable from another group using Tukey's analysis, then there is a fall-back analysis we perform. Referring to the earlier, important design aspect in that multiple cells (manufacturing conditions) exist on the same stencil, all the deposits on that stencil are made during the same stroke. This allows us to have paired data! Thus, if Tukey's method (that does not automatically pair data) fails to show a significant difference in the cells' performance, then we can follow that analysis with a paired-t test. While all of Tukey's analyses in the earlier work[7] cannot be shown here due to page length restrictions, we will demonstrate one such analysis. Shown below is an example of a multiple comparison test using Tukey's method for the volume of paste deposited in 12 mil circles on Stencil A.

The cell with the maximum volume of paste is determined from the data below. Cell L has the highest mean and hence it is the best. However, it is necessary to determine if Cell L is statistically the best. Therefore, the statistically best and worst cells are determined by using the confidence intervals for each cell as shown below. The mean transfer efficiency over 30 boards is compared for each cell.

Analysis based on Volume: Tukey's Test on 12 mil Circles for Stencil A
One-way ANOVA: Average GSI Volume versus Cell ID

Analysis of Variance for Avg GSI

Source	DF	SS	MS	F	P
Cell ID	10	697788	69779	203.52	0.000
Error	319	109371	343		
Total	329	807159			

Individual 95% CIs For Mean
Based on Pooled StDev

Level	N	Mean	StDev	-+---------+---------+---------+-----
Cell_A	30	156.39	14.60	(*-)
Cell_B	30	171.52	16.57	(*-)
Cell_C	30	195.34	16.39	(*)
Cell_E	30	220.81	23.34	(*)
Cell_F	30	237.81	18.77	(-*)
Cell_G	30	254.07	19.49	(-*)
Cell_H	30	284.75	16.78	(*)
Cell_I	30	257.86	28.11	(-*)
Cell_J	30	270.70	16.65	(*)
Cell_K	30	274.28	13.84	(*)
Cell_L	30	307.69	14.06	(-*)

-+---------+---------+---------+-----
Pooled StDev = 18.52 150 200 250 300

Tukey's pairwise comparisons

Family error rate = 0.0500
Individual error rate = 0.00143

Critical value = 4.55

Intervals for (column level mean) - (row level mean)

	Cell_A	Cell_B	Cell_C	Cell_E	Cell_F	Cell_G
Cell_B	-80.52 0.25					
Cell_C	-54.33 -23.57	-39.20 -8.43				
Cell_E	-79.81 -49.04	-64.67 -33.91	-40.86 -10.09			
Cell_F	-96.81 -66.04	-81.67 -50.91	-57.86 -27.09	-32.38 -1.62		
Cell_G	-113.06 -82.30	-97.93 -67.17	-74.11 -43.35	-48.64 -17.87	-31.64 -0.88	
Cell_H	-143.75 -112.98	-128.62 -97.85	-104.80 -74.03	-79.32 -48.56	-62.32 -31.56	-46.07 -15.30
Cell_I	-116.85 -86.09	-101.72 -70.96	-77.90 -47.14	-52.43 -21.66	-35.43 -4.67	-19.17 11.59
Cell_J	-129.69 -98.93	-114.56 -83.79	-90.74 -59.98	-65.26 -34.50	-48.27 -17.50	-32.01 -1.24
Cell_K	-133.27 -102.51	-118.14 -87.38	-94.32 -63.56	-68.85 -38.08	-51.85 -21.08	-35.59 -4.83
Cell_L	-166.68 -135.92	-151.55 -120.78	-127.73 -96.97	-102.26 -71.49	-85.26 -54.49	-69.00 -38.24

	Cell_H	Cell_I	Cell_J	Cell_K
Cell_I	11.51 42.28			
Cell_J	-1.32 29.44	-28.22 2.55		
Cell_K	-4.91 25.86	-31.80 -1.04	-18.97 11.80	
Cell_L	-38.32 -7.55	-65.21 -34.45	-52.37 -21.61	-48.79 -18.03

The cells are compared with other cells and a confidence interval is generated for each comparison. The worst performing cells are colored in red and the best performing cells are colored in green. From the above analysis, Cell L is the best

performing cell and no further analysis on it needs to be performed because all CIs pertaining to Cell L do not contain zero. The cells that include zero in their confidence interval are not statistically different, as a group-to-group comparison. Consider the comparison of Cell A to Cell B. The confidence interval goes from a negative number (-30.52) to a positive number (0.25) and this includes zero and hence they are not statistically different according to Tukey's test. A paired-t test is necessary to determine if the cells are statistically different considering that the data can, in fact, be paired for analysis. Cell A is compared to all the other cells and a paired-t test is performed for combinations whose confidence interval contains zero to determine the best Cell/Cells.

Paired – t Test

In the paired–t test every board for a cell is compared to the board for the other cell. The difference between two cells is calculated. If the confidence interval for the combination again contains zero and the p-value is greater than 0.05, then the Cells are not statistically different.

Shown below is the paired–t test to determine if Cell B and Cell A have statistically different performance for print deposits for 12 mil Circles after the data are paired.

12 mil Circle Worst Cell

Paired T-Test and CI: Cell_B, Cell_A

Paired T for Cell_B - Cell_A

	N	Mean	StDev	SE Mean
Cell_B	30	171.52	16.57	3.03
Cell_A	30	156.39	14.60	2.67
Difference	30	15.13	18.07	3.30

95% CI for mean difference: (8.38, 21.88)
T-Test of mean difference = 0 (vs not = 0): T-Value = 4.59 P-Value = 0.000

The CI and p-value indicate that Cells A and B are statistically different, after pairing their data, and that the mean volume deposited for 12 mil Circles of Cell B is greater than Cell A. Similar analyses are performed for transfer efficiency and std. dev/ volume and for all aperture sizes and can be found elsewhere[7].

Summary of the Comparison Study Findings

Multiple comparison tests based on Tukey's test and paired-t test were performed to statistically determine the best and worst performing cells for different stencil fabrication techniques. From the analysis it was found that, for a laser cut aperture, a high tapered aperture with high electropolish improved the performance of the stencil. However, the effect of electropolish is unclear due to the reduced stencil thickness for high electropolished apertures. An increase in the level of taper caused an increase in the volume of paste deposited and this trend was noted for all the aperture sizes considered in the study.

For E-fab apertures, a medium tapered cell performed the best when compared to the other E-fab apertures. The same trend was observed for all the apertures. The effect of taper was more predominant in 12 mil and 10 mil circles. In the case of the chemical etching process, over-etched aperture cells performed better than the other apertures. However, the better performance of the over-etched apertures can be attributed to the larger board side diameter.

Among the three stencil fabrication techniques, the laser-cutting process seems to perform better than the E-fab and chemical etching process for apertures from 6 to 10 mils. For 12 mil circles, both the laser cutting and E-fab processes have comparable performance.

Conclusion and Future Considerations

The above findings are but the "tip of the iceberg" of the information that is contained in Aravamudhan's thesis[7]. We will continue to publish work from that document, in conjunction with some of our current studies in 01005 assembly process development.

Some of our future and ongoing studies will include the following:
Stencils with different levels of electropolish (maintaining the same thickness) and determine the effect of electropolish on the print performance of the small apertures.

- All the experiments in the present study are performed on a bare copper board, for many good reasons mentioned above. The future experiments will use a real PCB (i.e., with pads, circuitry, and surface finish).
- Future experimentation will also include different paste types, such as Type IV and Type V to compare with the current results.
- This work utilized Sn/Pb paste, ongoing activities utilize Pb-free, SAC pastes.

Acknowledgements
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References

1. Goodman, T., "CSPs In Japanese Portable Products", Proceedings of SMTA International Conference, 1999.

2. Primavera, A., "Influence of PCB Parameters On Chip Scale Package Assembly and Reliability", Proceedings – SMTA International Conference, San Jose Convention Center, San Jose, CA, September 1999.

3. Partridge, J., et al., "Paste Printing and Characterization for Chip Scale Package Assemblies", Proceedings of SMTA International Conference, San Jose, California, August 1998, pp. 405 – 416.

4. Clech, J., "Flip-Chip / CSP Assembly Reliability and Solder Volume Effects", Proceeding of Surface Mount International Conference, August 1997, pp. 315 – 324.

5. Yee, S., "Optimization of Design and Process Parameters for CSP Solder Joints", Proceedings - APEX Conference, January 2000, pp. 55-58.

6. Painaik, M., "Process Development for Fine Feature Stencil Printing" Master's Thesis, State University of New York at Binghamton, New York, 2002.

7. Aravamudhan, S., "Process Development and Characterization of Stencil Printing Process for Small Stencil Apertures," Master's Thesis, State University of New York at Binghamton, New York, 2003.

8. Solberg, V., et al., "Developing a Repeatable SMT Assembly Process for Chip Scale Packaging" Proceedings of Apex Technical Program, Long Beach Convention Center, Long Beach, California, March, 2000, Session P-AP8, pp. 2-1 to 2-4.

9. Burr, D., "Printing Guidelines for BGA and CSP Assemblies", Proceedings of Surface Mount International Conference, San Jose Convention Center, San Jose, California, August 1998, pp. 417 –424.