

Soldering the QFN Stacked Die Sensors to a PC Board

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INTRODUCTION

The purpose of this application note is to describe suggested methods of soldering sensor QFN devices to a printed circuit board (PCB) for both automotive and consumer applications. Actual experience and surface mount development efforts are required to optimize the process per individual device requirements and practices.

Figure 1 shows the bottom view of QFN 16 lead, 6x6, individual sensor packaged device.



Figure 1. QFN 16-Lead, 6x6 mm Stacked Die Sensor

OVERVIEW OF SOLDERING CONSIDERATIONS

Solder Joint Reliability (SJR) testing is performed to determine a measure of board level reliability when exposed to thermal cycling. Information provided here is based on experiments executed on QFN devices but PCB designs should be used as guidelines only. Actual surface mount process and design optimizations are recommended to develop an application specific solution.

For automotive grade product applications, Freescale typically prefers to reach a minimum of 2000 cycles before first solder joint failure in SJR experiments. The widely accepted temperature range for testing is -40°C to +125°C. For these automotive applications, it is recommended to solder the exposed pad to the PCB for greater board level reliability. The footprint recommendations for automotive applications are displayed in Figure 2.

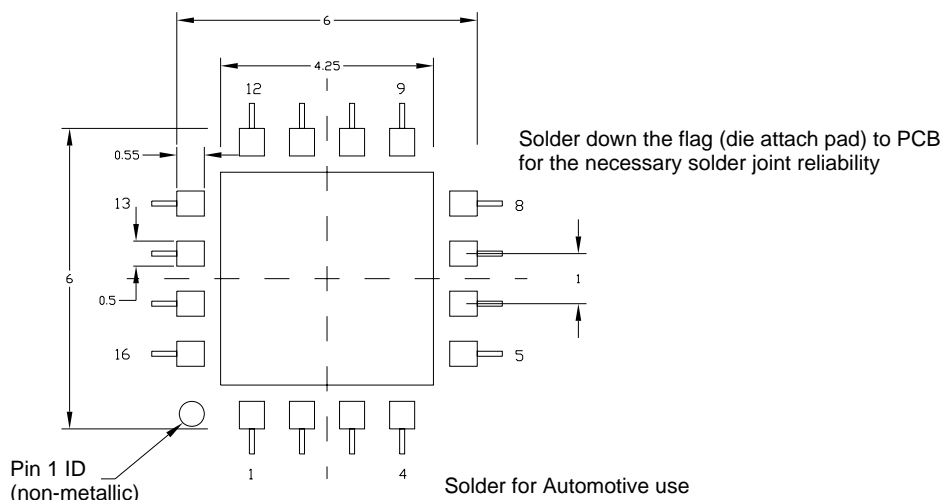
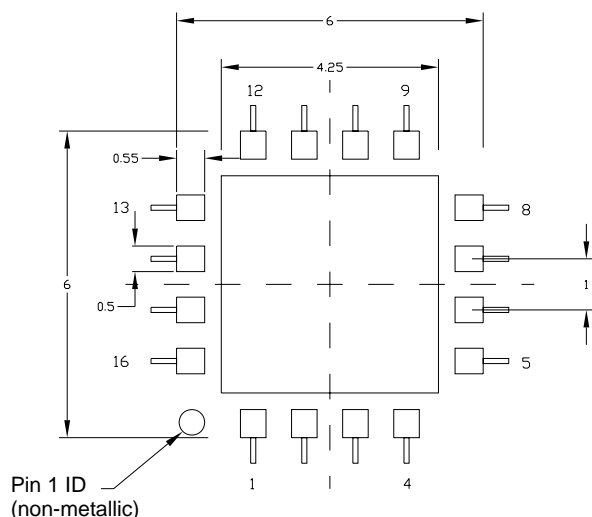


Figure 2. PCB Footprint for 16-Lead QFN, 6x6 mm for Automotive Grade Products and Application

For consumer grade product applications, it is recommended to not solder down the center flag area. Product data sheets should be referenced for device specific recommendations. Consumer SJR temperature cycling conditions may vary widely depending on the application and specific user. Typically, Freescale consumer SJR testing is

performed from 0°C to +100°C and can meet customer performance requirements without soldering down the exposed pad. SJR evaluation experiments have been done comparing a soldered down and non-soldered down flag area. Both soldering configurations pass 500 cycles before failure with a temperature range between -25°C to +125°C.



Do not solder down flag and 4 corner ground pads on the package for consumer application

Do not place any top metal patterns or via structures beneath the package.

Note: The die pad (flag) is not generally recommended to be soldered down for consumer product application. All dimensions are in mm.

Figure 3. PCB Footprint for 16-Lead QFN, 6x6 mm for Consumer Grade Products and Applications

PCB DESIGN GUIDELINES

The following are the general recommended guidelines for mounting QFN sensors for either automotive or consumer applications.

1. Use PCB land pad (footprint) for consumer (Figure 2), and automotive (Figure 3) applications.
2. Do not solder down the flag for consumer applications as shown in Figure 3, while automotive application require soldering the flag as shown in Figure 2.
3. Do not solder small corner pad features which are used as mold lock features. These are already neglected on the footprint recommendations (Figure 2 and Figure 3).
4. Use the NSMD (Non Solder Mask Defined) pattern guideline shown in Figure 4 for perimeter lands.

5. Solder mask opening = PCB land pad +0.125 mm.
6. Stencil aperture size = PCB land pad – 0.025mm, (5-6) mil thick stencil as shown in Figure 5.
7. Do not place insertion components or vias at a distance less than 2mm from the package land area.
8. Signal trace connected to pads should be as symmetric as possible. Put dummy traces if there are no-connect (NC) pads, in order to have same length of exposed trace for all pads. Signal traces with 0.1mm width and min. 0.5mm length for all PCB land pad near package are recommended as shown in Figure 4 and Figure 5. Wider trace can be continued after the 0.5mm zone.

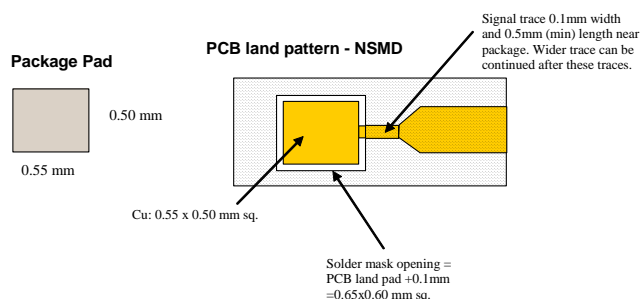


Figure 4. NSMD Solder Mask Design Guidelines

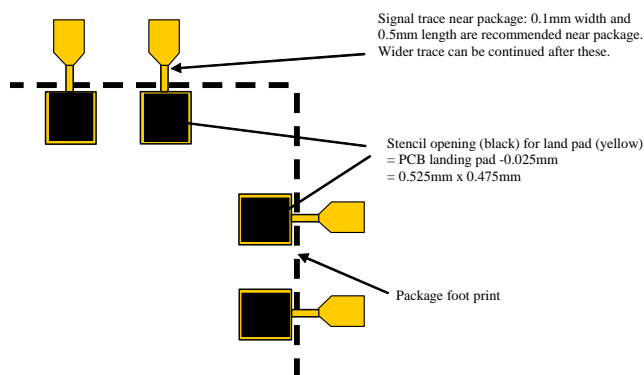


Figure 5. Stencil Design Guidelines

9. Use a standard pick and place process and equipment (no hand soldering process).
10. It is recommended to avoid screwing down the PCB to fix it into an enclosure since this may cause the PCB to bend.
11. PC boards should be rated for multiple reflow of lead-free conditions with 260°C maximum temperature.

12. Recommended surface finishes are Organic Surface Protection (OSP), Electroless Nickel Immersion Gold (ENIG), or white tin (Stannous). Hot Air Leveling (HAL) can cause uneven surface issues.
13. Please cross reference with the device datasheet for any additional mounting guidelines specific to the exact device used.

STENCIL DESIGN FOR EXPOSED FLAG AREA (AUTOMOTIVE APPLICATIONS)

An array design (pattern) is recommended in the stencil opening for the exposed flag region. The array pattern with stencil openings representing 50-80% of total area has the following benefits as compared to a complete one-to-one opening size:

1. Reduced solder volume and chance of overflow bridging to the adjacent perimeter lead pads.
2. Reduced voiding caused by trapped flux out-gassing during reflow processing.

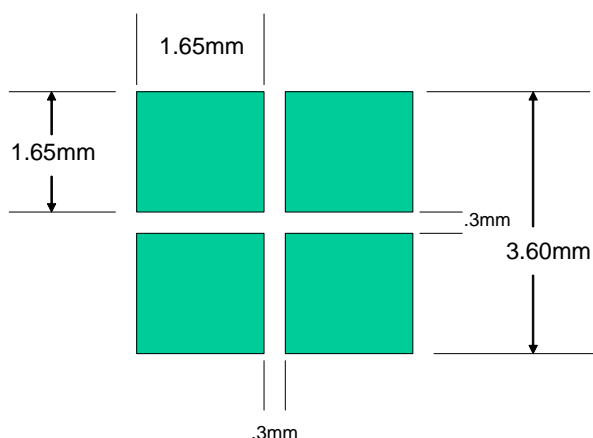


Figure 6. "Window Frame" Solder Stencil Array

3. Reduced chance of solder scooping caused by bending of squeegee blade during screen printing.

Figure 6 shows an example of a solder stencil flag design used in development of automotive SJR test boards.

Circular stencil openings (Figure 7) may also be evaluated as an alternative to the array design above. Some experimentation has shown reduced trapped voiding with this type of opening array.

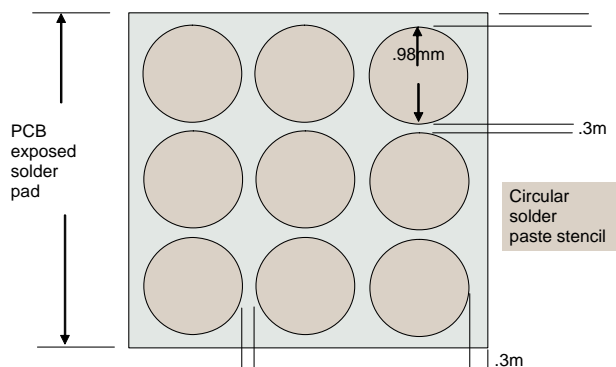


Figure 7. "Circular" Solder Stencil Array

REFLOW SOLDERING

The purpose of the reflow process is to melt solder particles, wet the surfaces to be joined, and solidify the solder into a stronger metallurgical joint. Prior to the melting phase, several other key phases occur in the sequence of events described in Figure 8.

Temperature profile is the most important control in reflow soldering and must be fine tuned to establish a robust process. Generally, when the largest thermal mass device(s) on a PCB reach reflow temperature, all other devices on the PCB will have also reached the reflow temperature. A thermocouple can be placed beneath the largest thermal mass device(s) to determine when the appropriate temperature has been reached.

The selected solder paste will have a flux. The flux dominates the reflow profile for phases such as soak time, soak temperature, and ramp rates. Peak reflow temperature is the temperature when the solder paste metal melts plus a safety factor to ensure all solder paste on the PCB reflows.

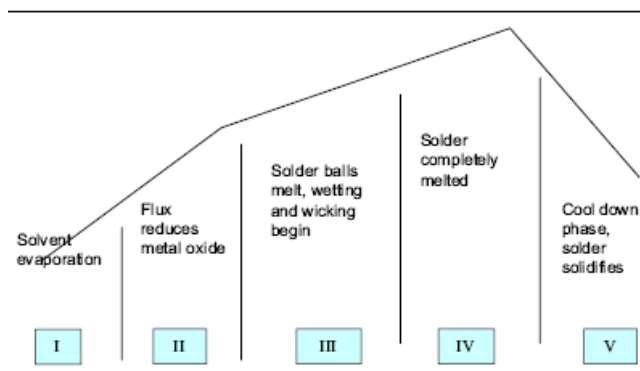


Figure 8. General Solder Reflow Phases

The reflow profile should follow the solder paste supplier's recommended profile. Some deviations are likely to be made during processing optimizations for a particular PCB application and density of devices. It is recommended to

evaluate deviations first using a copper (Cu) coupon test. The area of solder paste coverage can be measured either as a diameter or in “x” and “y” lengths. The Cu-coupon is then reflowed at a particular reflow profile and the solder area is re-measured in diameter or “x” and “y” lengths. The goal is to

have a reflow profile that produces the most horizontal spread caused by solder wetting. For best results, the Cu-coupon should be lightly sanded before use to remove Cu-oxide build up. Resulting reflow profile will vary with application and solder paste selection.

INSPECTION

Unlike traditional leaded components, the solder joints of QFN are formed primarily underneath the package. Optical inspection and x-ray inspection are recommended to verify any open or short circuits (bridging) after reflow. Micro-Sectioning is another method of inspecting solder joint quality during process optimizations but is less suitable to production inspection due to slow processing.

Figure 9 shows a typical x-ray of an assembled part. Note: This is the expected x-ray image of a commercial

component, showing the dummy traces and the paddle unsoldered.

Figure 10 shows the expected x-ray image of an automotive component, showing the dummy traces and a soldered paddle. The voids under the paddle are not regarded as defective. Note that the dummy traces provide uniformity in temperature during reflow, which reduces voids in the assembly.

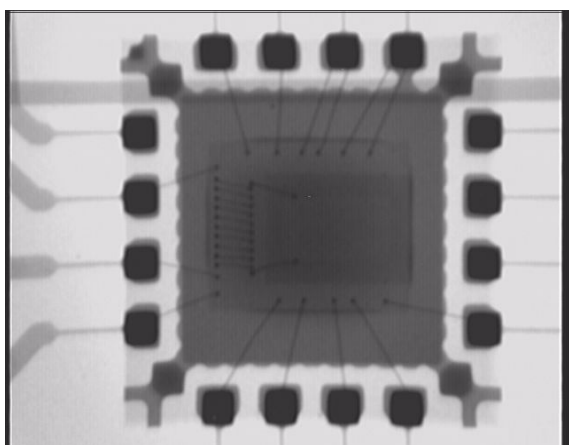


Figure 9. X-ray Image of a Commercial Component

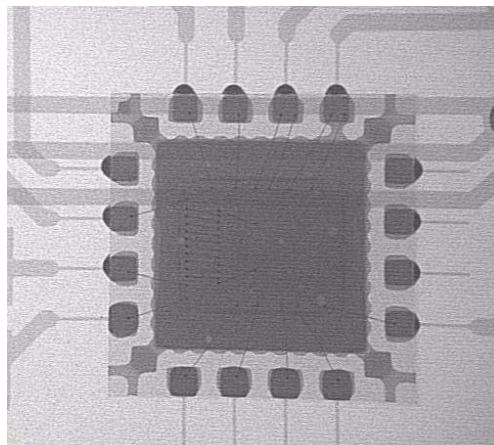


Figure 10. X-ray Image of an Automotive Component

REWORK PROCEDURE

A dedicated rework station can be designed with a split light system, an XY table for alignment, and a hot air reflow system with top and bottom heater for component removal. To remove a QFN component from a PCB, hot air should be applied simultaneously from the top and bottom heaters. An air nozzle with correct size should be used to apply the heat to the QFN such that the vacuum pick-up tool can properly remove the component as the solder begins to reflow. The pictorial procedure is shown below in Figure 11. Careful optimization of time and temperature exposure must be characterized for

each application specific situation in order to avoid damage to PCB construction. Many assembly sites have extensive in-house knowledge on rework and their experts should be consulted for further guidance.

Once the QFN component is removed, the site is to be cleaned and dressed to prepare for the new component placement. A de-soldering station can be used for solder dressing. Again, experts on reworking should be consulted for further guidance.



Figure 11. QFN Package Removal Process

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