CONFERENCE:
September 11 – 13

EXHIBITION:
Wednesday, September 12

Register by August 13 and save!

REGISTER NOW!

Santa Clara Convention Center, CA


CONNECTING DESIGN TO FAB TO ASSEMBLY
PCB WEST 2018
Conference & Exhibition
pcbwest.com
VIEW THE CONFERENCE CATALOG
SEE WHO'S EXHIBITING

UP Media Group

PRINTED CIRCUIT DESIGN & FAB

CIRCUITS ASSEMBLY

pcdandf.com
circuitsassembly.com
July 2018

High-Current Traces

Why the IPC Charts Aren't Enough

High-Speed Flex Design

Zestron: 'Cleaning Up' in Asia

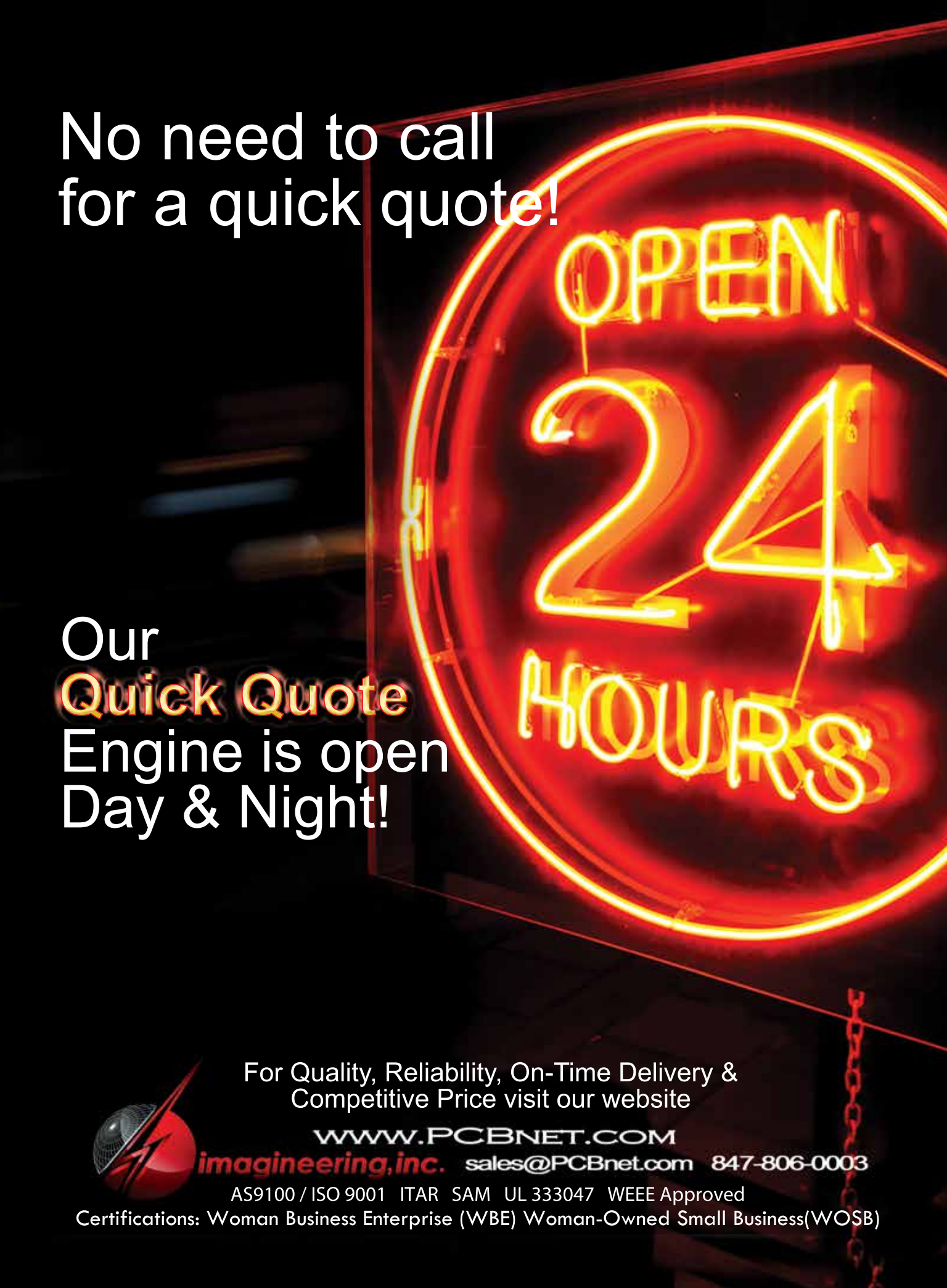
X-ray Magnification

SIERRA CIRCUITS

Losing control of your impedance?

DOWNLOAD THE FREE DESIGN

landing.protoexpress.com/controlimpedancedesignguide


No need to call
for a quick quote!
OPEN
24
HOURS
Our
Quick Quote
Engine is open
Day & Night!
For Quality, Reliability, On-Time Delivery &
Competitive Price visit our website
WWW.PCBNET.COM
imagineering,inc.
sales@PCBnet.com 847-806-0003
AS9100 / ISO 9001 ITAR SAM UL 333047 WEEE Approved
Certifications: Woman Business Enterprise (WBE) Woman-Owned Small Business(WOSB)

How important are your connections?

Plasma to improve reliability – *no bad connections!*

VIA™ Series
Plasma System

> Desmear
> Etchback
> Panel Cleaning

Plasma treatment in PCB Manufacturing:

- Removing resin smear
- Removing carbon byproducts from blind vias
- Efficient, economical and environmentally benign

Contact us now to learn more.
+1-800-326-1151
+1-925-827-1240
info@nordsonmarch.com

nordsonmarch.com

Nordson MARCH

sensors MIDWEST

OCTOBER 16-17 2018

Donald E. Stephens Convention Center
ROSEMONT, IL

1,500+ ATTENDEES LOOKING FOR SENSOR SOLUTIONS

65+ EXHIBITORS SHOWCASING LEADING TECHNOLOGIES

45+ KNOWLEDGEABLE SPEAKERS AND EXPERTS

30+ TECHNICAL SESSIONS COVERING THE LATEST INDUSTRY TRENDS

2 FULL DAYS OF ESSENTIAL EDUCATION

1 EVENT YOU CAN'T AFFORD TO MISS!

Register Now!
www.sensorsmidwest.com

THE EVENT FOR SENSORS DESIGN & INDUSTRIAL IoT

INDUSTRY SPONSOR
PRINTED CIRCUIT DESIGN & FAB/ CIRCUITS ASSEMBLY

OFFICIAL PUBLICATION:
sensors ONLINE

PRODUCED BY:
QUESTEX LLC

SIZE MATTERS.

Visit Us At Booth #408

Sierra Circuits is a better fit.

We manufacture high quality HDI PCBS

- **Blind and buried vias**
- **Fine lines and spaces down to 30 microns**
- **Sequential lamination**
- **Fine pitch devices down to 200 microns**
- **50 micron laser drilled via-in-pad**

visit www.protoexpress.com/hdi
to learn more and get a Free Design Guide

CONNECTING
DESIGN
TO FAB
TO ASSEMBLY

CONFERENCE CATALOG

PCB WEST 2018

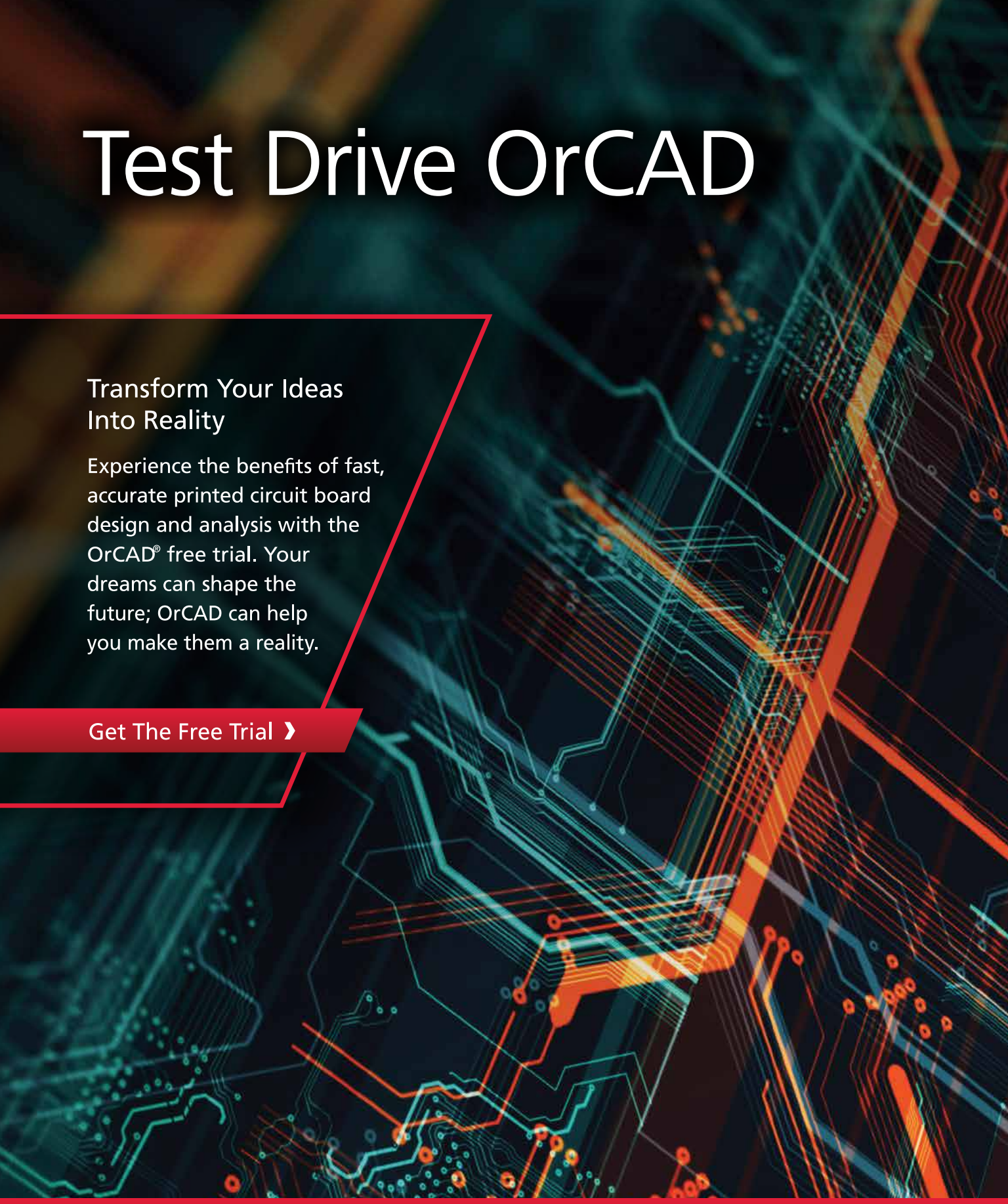
Conference & Exhibition

Conference:
September 11 – 13
Exhibition:
Wednesday, September 12
Santa Clara Convention Center, CA

PRINTED CIRCUIT
DESIGN & FAB

CIRCUITS ASSEMBLY

pcbwest.com


Test Drive OrCAD
Transform Your Ideas Into Reality
Experience the benefits of fast, accurate printed circuit board design and analysis with the OrCAD® free trial. Your dreams can shape the future; OrCAD can help you make them a reality.
Get The Free Trial ›
Visit Us at PCB West Booth #400
OrCAD™
CADENCE PCB SOLUTIONS
EMA Design Automation®

FROM THE CONFERENCE CHAIR

For 27 years PCB West has trained designers, fabricators and, lately, assemblers on making printed circuit boards for every product or use imaginable. How far we've come! Last year's event attracted nearly 2,000 designers and engineers and more than 100 exhibitors for the three-day technical conference and sold-out exhibition.

From high reliability military/aerospace to cutting-edge IoT and wearables, there's something for everyone involved in the electronics supply chain. And we've added tracks for fabricators and assemblers as well. This is one show you cannot afford to miss. See you in September!

Mike Buetow

VENUE AND TRAVEL INFO:

EVENT LOCATION

Santa Clara Convention Center
5001 Great America Parkway
Santa Clara, CA 95054
408-748-7000
santaclara.org/conventioncenter

- Easy access from Interstate 101
- Free parking
- Attached to the Hyatt Regency Santa Clara Hotel

AIRPORTS

San Jose International Airport (SJC)
Hotel direction: 4 mi south
Estimated taxi fare to hotel: $17 (one way)
San Francisco (SFO)
Hotel direction: 30 mi south
Estimated taxi fare to hotel: $90 (one way)

SHUTTLE INFORMATION

The Santa Clara Convention Center and Hyatt Regency Santa Clara are located just 12 minutes (6 miles) from Mineta San Jose International Airport (SJC) and 35 minutes (31 miles) from San Francisco International Airport.

Super Shuttle is offering PCB West attendees a 10% discount on all services. To book a shuttle in advance, please click the below link: http://groups.supershuttle.com/pcbwest.html

HEADQUARTERS HOTEL

Hyatt Regency Santa Clara
5101 Great America Parkway
Santa Clara, California, USA, 95054

2018 Group Rate: $309/night.
Reservations can be made by calling 408-200-1234 or 888-421-1442 or https://aws.passkey.com/go/pcbwest18
Please be sure to mention "PCB West 2018" to ensure you get the blocked rate.
The deadline to reserve a room is August 20, 2018.
As the block rate sells out, any reservation made will be based on availability, and prevailing rates will apply.

CONFERENCE PRICING AND POLICIES

Register by the Early-Bird Deadline of August 13 to save up to $100

ROW SEAT

SECTION
FREE
EXHIBITION ONLY
12 SEPTEMBER 2018

Exhibition Only Pass
FREE!

(Wed., September 12 Only)

Admission to the following events on Wednesday, September 12:
One-day exhibition
FREE technical sessions
Lunch and an evening reception

ROW SEAT

SECTION
BEST VALUE
3-DAY
ALL-INCLUSIVE
TECHNICAL
CONFERENCE PASS
11-13 SEPTEMBER 2018

3-Day All-inclusive Technical Conference Pass
BEST VALUE!

$1195 through August 13 ... $1295 after August 13 (Tues., September 11 – Thurs., September 13)

3-Day technical conference pass includes:

Choice of any conference sessions during the entire Tuesday, Wednesday and Thursday technical conference
One copy of the conference proceedings
Lunch-n-Learn sponsored by Streamline Circuits on Tuesday
Lunch-n-Learn sponsored by Polar Instruments on Thursday
Conference WiFi sponsored by Mentor
Conference Coffee sponsored by Sierra Circuits
Admission to the following events on Wednesday, September 12:

- One-day exhibition
- FREE technical sessions
- Lunch break sponsored by Sierra Circuits
- Evening reception sponsored by Ultra Librarian

One-day Technical Conference Pass Options:

$595 per day through August 13...$695 per day after August 13

(Choose One Day Only: Tues., September 11; Wed., September 12; OR Thurs., September 13)

One-Day Tuesday Technical Conference Pass

Tues., September 11:

Choice of any conference sessions on Tuesday
Lunch-n-Learn sponsored by Streamline Circuits
Admission to the following events on Wed., Sept. 12th:

- One-day exhibition
- FREE technical sessions
- Lunch sponsored by Sierra Circuits
- Evening Reception sponsored by Ultra Librarian

ROW SEAT

One-Day Wednesday Technical Conference Pass

Wed., September 12:

Choice of any conference sessions on Wednesday
Admission to the following events on Wednesday, September 12th:

- One-day exhibition
- FREE technical sessions
- Lunch sponsored by Sierra Circuits
- Evening Reception sponsored by Ultra Librarian

ROW SEAT

One-Day Thursday Technical Conference Pass

Thurs., September 13:

Choice of any conference sessions on Thursday
Lunch-n-Learn sponsored by Polar Instruments
Admission to the following events on Wed., Sept 12th:

- One-day exhibition
- FREE technical sessions
- Lunch sponsored by Sierra Circuits
- Evening Reception sponsored by Ultra Librarian

ROW SEAT

Note: The conference proceedings are NOT included in the one-day pass. During registration you will have the option to add a copy for $200.

REGISTER NOW!

IPC 4-DAY DESIGNER CERTIFICATION PROGRAMS

September 7 – 10, 2018

Questions regarding the IPC Certification Program? Please contact Cheryl Fisher at 800.643.7822 x223 or cherylfisher@eptac.com.

IPC Designer Certification Program (CID)

$1960
Programs powered by EPTAC

The IPC Designer Certification or CID (Certified Interconnect Designer) is the industry's premier professional program directly focused on PCB design philosophy and requirements. If your passion is the transformation of electrical schematics into works of art that can be manufactured, assembled and tested, this program is for you. Already CID certified? Go Advanced now!

IPC Advanced Designer Certification Program (CID+)

$1960
Programs powered by EPTAC

Continuing the educational series for PCB Design, the IPC Advanced Designer Certification or CID+ (Advanced Certified Interconnect Designer) is the ultimate professional industry certification for a designer looking to obtain what we would consider a master's in PCB Design.

Questions?

Contact the PCB West Registration Desk at 855.290.2441

Payment Policies:

All payments for the conference must be received prior to attending. Payments can be made by credit card, check or wire transfer. Registrations without complete payment information will not be processed.
Check payments should be made to UP Media Group, Attn: PCB West 2018, P.O. Box 470, Canton, GA 30169.
ALL wire transfers are charged a $50 processing fee per registration.
Credit card payments will show a charge from UP Media Group.

Refunds and Cancellations:

A $25 cancellation fee will be withheld from any registration fees refunded. All refund requests must be made in writing no later than August 21, 2018, Attn. Alyson Corey, acorey@upmediagroup.com. "No shows" who have not made a written request by August 21 are fully liable for conference tuition/fees. Registrations made after August 21 are considered confirmed, and no refund requests will be accepted; registrants will be fully liable for conference tuition/fees and will be invoiced accordingly.

REGISTER NOW!

TUESDAY, SEPTEMBER 11

TITLE	SPEAKER	CATEGORY
8:00am CONFERENCE COFFEE BREAK, *Sponsored by Sierra Circuits*		
8:30am - 12:00pm		
1: PCB Design Strategy for High Density BGA and CSP Components	Vern Solberg, Solberg Technical Consulting	DfF/DfM/DfA/DfT
9:00am - 11:00am		
2: Layout of Switch Mode Power Supplies	Rick Hartley, RHartley Enterprises	EMI/EMC/PCB Design
3: Power Distribution Made Easy	Daniel Beeker, NXP Semiconductor	PCB Design/Layout/ Placement
9:00am - 5:00pm		
4: The Basics of PCB Design	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
5: What's New in the IPC Design Standards, and How to Use Them	Gary Ferrari, FTG Circuits	PCB Design/Layout/ Placement/Standards
6: PCB Stackup Design and Materials Selection	Bill Hargin, Z-zero	PCB Design
7: Troubleshooting and Defect Resolution of SMT Assembly Processes	Jim Hall and Phil Zarrow, ITM Consulting	SMT/Electronics Assembly
11:00am - 12:00pm		
8: Managing Your Impedance, Coupling and Return Paths in Design and Avoid Unnecessary Iterations with SI/PI Engineers	Dennis Nagle, Cadence Design Systems	High Speed
9: Evaluating an Appropriate Power Plane through Power Integrity Simulation	Richard Villamor Legaspino, Analog Devices	Power Integrity
10: PCB Library Development and Management – A Treatise	Vijayakumar David, Tessolve Semiconductor	Libraries
12:00pm – 1:00pm LUNCH-N-LEARN, *Sponsored by Streamline Circuits (Tuesday conference attendees only)*		
1:00pm - 3:00pm		
11: Power Integrity & Decoupling Primer for PCB Designers	Ralf Bruening, Zuken	SI/PI
12: Laying Out Analog/Digital Planes	Robert Hanson, Americom	SI/PI
1:00pm - 4:30pm		
13: Effective PCB Design: Techniques to Improve Performance	Daniel Beeker, NXP Semiconductor	PCB Design/Layout/ Placement
14: Circuit Grounding to Control Noise and EMI	Rick Hartley, RHartley Enterprises	EMI/EMC & PCB Design
3:00pm - 5:00pm		
15: Thermal Integrity within an Electrical Design Flow	Jim DeLap, Ansys	PCB Design/Layout/ Placement
16: How to Fight Magnetic Noise Gremlins	Keven Coates, Geospace	EMI/EMC

WEDNESDAY, SEPTEMBER 12

8:00am CONFERENCE COFFEE BREAK, *Sponsored by Sierra Circuits*		
8:30am - 12:00pm		
17: The Complexities of Fine Pitch BGA Design	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
9:00am - 10:00am		
18: PCB Reverse Engineering Countermeasures	Jeremy Hong, Hong's Electronics	PCB Design/Layout/ Placement
9:00am - 11:00am		
19: Multi-Board Design: Castellation, Connection, SI, Alignment	Ben Jordan, Altium	PCB Design/Layout/ Placement
20: An Intuitive Approach to Understanding Basic High-speed Layout	Keven Coates, Geospace	SI/PI
21: A Beginner's Introduction to PCB Trace Impedance	Ken Taylor, Polar Instruments	PCB Design
9:00am - 5:00pm		
22: Cost Reduction through Design for Manufacturing and Assembly	Gary Ferrari, FTG Circuits	DfF/DfM/DfA/DfT
23: The Complete Guide to Understanding Transmission Lines	Robert Hanson, Americom	High Speed
10:00am – 6:00pm EXHIBITION FLOOR OPEN		
10:00am – 2:00pm EXHIBIT HALL BOOTH BARISTA, *Sponsored by Zuken*		

REGISTER NOW!

WEDNESDAY, SEPTEMBER 12 (continued)

TITLE	SPEAKER	CATEGORY
10:00am - 12:00pm		
24: iPhone X – Steve Jobs' iPhone	Bill Cardoso, Creative Electron	PCB Design/Layout/ Placement
11:00am - 12:00pm		
25: Continuing Test Point Management throughout a PCB Design Flow	Mark Laing, Mentor	PCB Design/Layout/ Placement
26: Clock Jitter Behavior on Different PCB Layout Approach	Marcus Miguel Villaflores Vicedo, Analog Devices	PCB Design/Layout/ Placement
27: ECAD-MCAD Co-design for a Competitive Advantage	John McMillan, Mentor	PCB Design/Layout/ Placement
12:00pm – 1:00pm LUNCH ON EXHIBIT FLOOR, *Sponsored by Sierra Circuits*		
1:00pm - 3:00pm		
28: Thermal Design Considerations for SMD PCBs	Keven Coates, Geospace	PCB Design/Layout/ Placement
29: Signal Attenuation in Very High Speed Circuits	Rick Hartley, RHartley Enterprises	High Speed/PCB Design
1:00pm - 4:30pm		
30: HDI Routing Solutions	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
31: The Basics of PCB Fabrication (101)	Paul Cooke, FTG Circuits	Fabrication
3:00pm - 5:00pm		
32: Differential Pair Routing for SI Control	Rick Hartley, RHartley Enterprises	High Speed/PCB Design
33: Evaluating the VIA Transition through TDR Simulation	Richard Villamor Legaspino, Analog Devices	RF/Microwave/PCB Design

FREE WEDNESDAY, SEPTEMBER 12

9am - 11:00am		
F1: Routing & Termination for Control of Signal Integrity	Rick Hartley, RHartley Enterprises	High Speed/PCB Design
9am - 10:00am		
F2: HDI: High Density Interconnect	Chris Nuttall, NCAB Group	PCB Design/Fabrication
10:00am - 11:00am		
F3: AI and Machine Learning Disrupting the Manufacturing of Your Products	Albert Yanez, AsteelFlash	Automation/Process Improvement
11:00am - 12:00pm		
KEYNOTE: Is Past Prologue? The Future of the PCB Design Industry - Walden Rhines, CEO, Mentor		
F4: Designing in the Age of Prototypes	Milan Shah, Royal Circuits	PCB Design
1:00pm - 2:00pm		
F5: Industry 4.0 and IPC-2581	Hemant Shah, IPC-2581 Consortium	Electronics Data Transfer/Standards
1:00pm - 3:00pm		
F6: The 10+ 21 Most Common Design Errors Caught by Fabrication (and How to Prevent Them)	David Hoover, TTM Technologies	DfF/DfM/DfA/DfT
2:00pm - 3:00pm		
F7: Efficient PCB Interposer Design Using a Novel Smart Router Based on Neural Networks and Genetic Algorithms	Xiao Ming Gao, Intel	PCB Design
3:00pm - 4:00pm		
F8: Optimizing Hardware for Your IoT Solution	Sean Priddy, Creation Technologies	Business/Markets
F9: PANEL: The Future of PCB Engineers	Phil Marcoux, PPM, Moderator	3D Printing/Fabrication
4:00pm - 5:00pm		
F10: 3D Printed Electronics: A New Dimension in Prototyping & Manufacturing	Simon Fried, Nano Dimension	Printed Electronics
F11: PANEL: Understanding the AS9100D Standard	Peter Bigelow, IMI, Moderator	Standards

CAD TOOL CORNER – FREE – WEDNESDAY, SEPTEMBER 12

1:00pm - 2:00pm		
C1: Ensure Your Electronic Design is Reliable and Robust by Simulation – During Schematic, Before Manufacturing and Testing	Yizhak Bot, BQR	PCB Design
2:00pm - 3:00pm		
C2: Retargeting Your Libraries for Newer, Better Processes without Breaking Your Bank	Vince Di Lello, Cadence Design Systems	PCB Design/Layout/ Placement
3:00pm - 4:00pm		
C3: Designing PCBs in the Context of a System	Gary Hinde, Cadence Design Systems	PCB Design
4:00pm - 5:00pm		
C4: Multi-Domain Collaboration for Electronics Systems Design	David Wiens, Mentor	PCB Design

THURSDAY, SEPTEMBER 13

TITLE	SPEAKER	CATEGORY
8:00am CONFERENCE COFFEE BREAK, *Sponsored by Sierra Circuits*		
8:30am - 12:00pm		
34: Design of Power Distribution and Decoupling	Rick Hartley, RHartley Enterprises	EMI/EMC & SI/PI & PCB Design
35: Part Placement Choices and Consequences	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
9:00am - 10:00am		
36: Intelligent DfM for Assembly	Kevin Webb, Mentor	PCB Design/Layout/ Placement
37: Providing Solutions for Thermal Management within RF Designs	James Barry, PCB Technologies	RF/Microwave/Thermal Management
9:00am - 11:00am		
38: The Mystery of Bypass Capacitors	Keven Coates, Geospace	SI/PI
39: Ask the Flexperts – Flexible Circuit Design through Test with Lessons Learned	Mark Finstad, Flex Circuit Technologies, and Nick Koop, TTM Technologies	PCB Design & Fabrication Processes
9:00am - 12:00pm		
40: Designing Embedded Passives and Related Technologies	Gary Ferrari, FTG Circuits	Embedded Passives/ Fabrication/Components
10:00am - 11:00pm		
41: DfM: Getting It Right from the Start	Chris Nuttall, NCAB Group	DfF/DfM/DfA/DfT
42: Arriving at an Optimal Stackup for Printed Circuit Boards Used in Silicon Validation	Vijay Nanjai Anandan, Tessolve Semiconductor	Fabrication
11:00am - 12:00pm		
43: Leveraging 3-D Layout to Optimize Rigid-Flex Designs	John McMillan, Mentor	PCB Design/Layout/ Placement
44: Overview of Several RF Structures and How They Work	John Coonrod, Rogers	RF/Microwave/PCB Design
12:00 pm – 1:00 pm LUNCH-N-LEARN, *Sponsored by Polar Instruments (Thursday conference attendees only)*		
1:00pm - 3:00pm		
45: Electromagnetic Fields for Normal Folks: Show Me the Pictures and Hold the Equations, Please!	Daniel Beeker, NXP Semiconductor	EMI/EMC
1:00pm - 4:30pm		
46: Flexible and Rigid-Flex Circuit Design and Assembly Process Principles	Vern Solberg, Solberg Technical Consulting	DfF/DfM/DfA/DfT
47: Best DfM Practices for Board Engineers	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
48: RF and Mixed Signal Board Design	Rick Hartley, RHartley Enterprises	RF/Microwave/PCB Design
3:00pm - 5:00pm		
49: PCB Design Techniques to Improve ESD Robustness	Daniel Beeker, NXP Semiconductor	EMI/EMC

DYCONEX

an MST company

Explore DYCONEX' advanced solutions in interconnect technology for high-reliability applications at booth# 203

- HDI and ultra-HDI/microvia PCBs
- Flex and rigid-flex substrates for 3D miniaturization
- LCP substrates for biocompatible and HF applications
- Advanced packaging substrates
- Comprehensive inspection and test concepts
- ISO 9001, ISO 13485 and EN 9100 certified

www.mst.com/dyconex

MST

Micro Systems Technologies

engineering for life

DYCONEX AG
Grindelstrasse 40, CH-8303 Bassersdorf, Switzerland
Phone +41 43 266 11 00, mail.dyconex@mst.com, www.mst.com/dyconex

Sales office USA:
Micro Systems Technologies, Inc., 6024 SW Jean Road, Lake Oswego, OR 97035
Phone +1 (503) 744 8500, sales.msti@mst.com, www.mst.com

MST Group. Active around the globe, the Micro Systems Technologies (MST) Group consists of four technology companies with more than 1100 employees in three countries: DYCONEX AG, Switzerland | Litronik Batterietechnologie GmbH, Germany | Micro Systems Engineering GmbH, Germany | Micro Systems Engineering, Inc., USA

TUESDAY, SEPTEMBER 11

8:00 am CONFERENCE COFFEE BREAK, Sponsored by Sierra Circuits

8:30 AM – 12 NOON

1: PCB DESIGN STRATEGY FOR HIGH DENSITY BGA AND CSP COMPONENTS

Vern Solberg, Solberg Technical Consulting

The ball grid array and chip-scale package families of components are recognized by many as the best solution for meeting the space restrictions of next-generation portable and handheld electronic products, but companies are also expecting improvements in functionality and performance. Because of the higher terminal density of BGA, fine-pitch BGA and CSP, PCB designers have realized the implementation of proven design rules ensures a positive effect on PCB fabrication yield, assembly process efficiency and end product cost. Furthermore, attendees will be able to explore a number of alternative 2.5-D and 3-D semiconductor packaging methodologies, review manufacturers design guidelines and assess alternative assembly process variations for HDI applications. This half-day tutorial will include a study of land pattern geometry options, HDI circuit routing guidelines, as well as the important factors related to specifying base materials and surface finishes that are most compatible with high-volume automated assembly processing. Participants will also have an opportunity to review and discuss JEDEC packaging standards for array configured components, the latest version of the IPC-7094, "Die Size and Flip-Chip BGA Design Standard," and IPC-7095, "BGA Design Standard," a document that includes both wide and fine-pitch array packaging methodology. Topics covered: 1. BGA/CSP process technologies and standards; single die package-level assembly variations; 2-D and 3-D multiple die package methodologies; JEDEC standards for BGA and CSP; IPC standards for implementing BGA and CSP. 2. PCB design guidelines for BGA and CSP; component selection and surface area planning; evaluating BGA and CSP terminal variations; land pattern development for array configured components; circuit routing strategies for BGA and CSP. 3. HDI circuit and Microvia design implementation; defining circuit complexity classifications (IPC-2226); analysis and consideration when estimating circuit density; benefits for implementing blind and buried microvias; guidelines for stacked, staggered and in-land microvias. 4. Specifying PCB base material, surface finish and coatings; reviewing established standards for circuit substrate materials; studying alternative high-performance material variations; choosing solder-compatible surface finishes for HDI circuits; specifying suitable solder mask coatings for the PCB. 5. Preparation for high-volume assembly processing; system requirements for BGA and CSP device placement; basic features needed for SMT assembly processing; palletizing to maximize assembly process efficiency; solder stencil development and solder alloy variations.

Who should attend: PCB Designer, System Designer, Hardware Engineer, Fabricator Engineer/Operator, Assembly Engineer/ Operator, Test Engineer

Target audience: Beginner, Intermediate

9:00 AM TO 11:00 AM

2: LAYOUT OF SWITCH MODE POWER SUPPLIES

Rick Hartley, Rick RHartley Enterprises

When executing PCB layout, we tend to treat digital circuits differently from analog circuits. Each has its own critical requirements. Switch mode power supplies are another wrinkle altogether and usually need to be treated differently from either analog or digital structures. All switch mode power supplies have four to five circuit loops, all of which are important, but a couple of these loops are downright critical in terms of PCB layout. An improperly designed switch mode supply often will not function as intended, and in some cases, not at all. In contrast, understanding what makes up a switcher circuit and knowing how to take care of the loops during PCB layout will allow these supplies to operate flawlessly, and with very high efficiency.

This course will outline the difference between switchers and series-regulated supplies, the different types of switcher circuits (buck, boost, etc.), basic theory of operation of switcher circuits and the impact of the various components, definition and behavior of the five loops, layout to isolate loops from one another to minimize voltage drop and to control current paths, layout to minimize noise and EMI, effect of paralleling output capacitors and proper grounding technique.

Who should attend: PCB Designer, Circuit/Hardware Engineer, SI Engineer, System Engineer

Target audience: Intermediate

3: POWER DISTRIBUTION MADE EASY

Daniel Beeker, NXP Semiconductor

This presentation will present a simple EM physics and geometry-based approach to designing power distribution networks on PCBs. From input power connection to the IC die, the simple rules discussed can be used to reduce power supply noise and improve EMC.

Who should attend: PCB Designers, System Designers, Hardware Engineers, SI Engineers

Target audience: Beginner, Intermediate

9:00 AM TO 5:00 PM

4: THE BASICS OF PCB DESIGN

Susy Webb, Fairfield Industries

Technical sessions at conferences often emphasize the latest techniques and technologies, but those classes are often too in-depth for a novice designer, and don't speak to the questions from the engineers who need to design their own boards. This class features an overview of the entire process of designing a board, from start to finish. We will begin with creating manufacturable footprints that meet the IPC specs. Then we will address some common placement techniques like floor planning, color coding, flow, orientation, and placement to set up routing. We will follow that with a discussion of planes and stackups and how to configure them to get the best results for parts and signals. Next, we move on to some fanout and routing techniques that are helpful for completing the design connections to meet the number one design rule: good electrical performance. We will complete the process by discussing some manufacturability concerns that can be affected by the way the board is designed, some finishing issues, and sending out good documentation that the manufacturers can easily understand and use.

Who should attend: PCB Designer

Target audience: Beginner

5: WHAT'S NEW IN THE IPC DESIGN STANDARDS, AND HOW TO USE THEM

Gary Ferrari, FTG Circuits

Designers are under pressure to not only lay out a circuit board to meet functional requirements, but produce a cost-effective design that meets the requirements of fabrication, assembly, test, and field service. As a result, designers must keep up with the latest changes/additions to the industry standards they must use. IPC has shortened the development cycle for many of its standards. This session will identify a minimum set of standards

Available courses:

IPC Designer Certification
IPC Advanced Designer Certification

September 7-10th, 2018

Enroll today, space is limited.

1-800-64-EPTAC or visit eptac.com/pcbwest2018

$1,960 each plus shipping for prep materials prior to class

Innovation never gets old.

eptac
TRAIN. WORK SMARTER. SUCCEED.

PCB WEST 2018
Conference & Exhibition

EPTAC makes it easy. Complete the course, pass the exam, receive your certification.
Best of all, add credentials to your technical expertise with an industry recognized certification.

Call **1-800-64-EPTAC**, email **sales@eptac.com** or visit **eptac.com** to find a class near you!

that the designer should be familiar with. Highlighted will be recent important changes to the most used design, materials, fabrication, assembly and test standards. The changes are **significant,** and affect all classes of products.

Attendees will learn recommended minimum standard set for designers, standards that affect the design of printed boards, and design changes that affect manufacture and reliability of a product.

Who should attend: PCB Designer, Electrical Engineer
Target audience: Beginner, Intermediate

6: PCB STACKUP DESIGN AND MATERIALS SELECTION

Bill Hargin, Z-zero

The objective of this tutorial is to guide design teams through the process of evaluating and selecting the right laminate for a design, creating PCB stackups that meet the requirements of complex, multilayer boards that work right the first time, within budget, and with reproducible results across multiple fabricators. The course will go into detail on tradeoffs between loss and cost, including dielectric loss, resistive loss, surface roughness, as well as glass-weave skew. After attending this course, students will be knowledgeable of PCB laminate tradeoffs, the laminate-materials market, and the process of troubleshooting problematic stackup designs. Attendees will also be exposed to cost-effective strategies for controlling loss and glass-weave skew.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer, Fabricator Engineer/Operator, Other
Target audience: Beginner, Intermediate, Advanced

7: TROUBLESHOOTING AND DEFECT RESOLUTION OF SMT ASSEMBLY PROCESSES

Jim Hall and Phil Zarrow, ITM Consulting

We don't assemble electronics in a perfect world. Defects happen. This course examines failures and root cause analysis of PCBA defects, starting with a clear definition of the generic types of defects and their impact, such as non-function, reduced reliability, etc. Detection and determination methodologies and procedures will be discussed. Attributes of specific processes and equipment centers, as well as materials that can contribute to defect generation are identified. Specific defects are then analyzed using these background methodologies: type of defect and impacts, detection methods, possible contributing causes, etc. Finally, general strategies and guidelines for preventing defects will be presented. This seminar is for anyone involved in directing, developing, managing and/or executing failure and root cause analysis and defect resolution, including managers, engineers and others in manufacturing, quality and design.

Who should attend: Hardware Engineer, Assembly Engineers/ Operator, Test Engineer
Target audience: Beginner, Intermediate

11:00 AM – 12:00 NOON

8: MANAGING YOUR IMPEDANCE, COUPLING AND RETURN PATHS IN DESIGN AND AVOID UNNECESSARY ITERATIONS WITH SI/PI ENGINEERS

Dennis Nagle, Cadence Design Systems

Are you fixing high-speed issues on your design by iterating with your SI/PI engineers? There is a better way. This talk will describe how PCB designers can screen their designs and identify issues that can avoid impedance mismatch, crosstalk and return path issues before SI/PI analysis.

Who should attend: PCB Designer
Target audience: Beginner, Intermediate, Advanced

9: EVALUATING AN APPROPRIATE POWER PLANE THROUGH POWER INTEGRITY SIMULATION

Richard Villamor Legaspino, Analog Devices

Most automatic test equipment (ATE) final test boards have analog and digital devices. These devices may be operation amplifier (OP-Amp IC), transistors and memory ICs, which require an appropriate power plane PCB design to connect from voltage source to the load devices. The power plane layout must be carefully designed to prevent power integrity issues such as current-resistance (IR) drop, plane current density, power plane density and power plane impedance. The other way to validate these issues is through power integrity simulation. Simulation can be performed at the pre- or post-layout design stage to prevent any respins of the board. In this presentation, the speaker used the Power-DC and Optimize-PI simulation tool to evaluate the appropriate power plane topology. To measure the IR drop, plane current density, power plane density and power plane impedance of the power plane layout.

Who should attend: PCB Designer, SI Engineer, Assembly Engineer/ Operator
Target audience: Intermediate

10: PCB LIBRARY DEVELOPMENT AND MANAGEMENT – A TREATISE

Vijayakumar David, Tessolve Semiconductor

PCB library, the fundamental block of PCB design, shall adhere to global standards such as IPC to ensure quality. Library parts need to be validated for graphical, logical rules and footprint attributes before release. Appropriate pin grouping, pin type, and multi-part shall be a part of symbol creation. Creating test schematic for symbol, version control, maintaining history, role-based access control, reusability, classification, alternate symbol/footprint, lifecycle status, internal part number, RoHS compliance, and automotive/military compliance are essential requirements. Information about footprints that are associated to padstacks is required before updating a padstack. Creating specific padstacks for BGAs meeting DfM according to pitch saves cost. SMD or NSMD padstacks for BGA, oblong pads for tight pitch PTH parts, pads for specific AWG, half PTH vias, paste-in-hole technology, supported mounting holes, pemnuts, holes for screw numbers, solder mask dam and resist, optimal rules definition for test points placement for flying probe tester and courtyard are some of considerations. Coding specific parts as preferred for a scope helps limit the designer using specific parts only for the scope. Updating specific attribute for multiple parts, team design option, symbol in sync with footprint, parts update alert to designer, and scheduling library distribution across different time zones are the requirements to be addressed. Associating datasheet to a part helps designers review the relevant specification document used for part build. Creating footprints with the right IPC-7351 density level facilitates effective real estate usage. Part of schematic or layout created as block and hierarchical split symbols can be a library part. Assigning specific property value on the discrete parts helps the designer with the task of auto-generation of SI DML models. Preference of SMT over TH components, appropriate termination for backdrilling, considerations for edge mount SMA, CQFP, SMP, pin receptacles selection for ATE boards, datasheet recommendations, slot angle definition in EDA tool and importing 3D models are to be promptly implemented. Automating the library creation process and QA will ensure quality and reduce cycle time. Maintaining a centralized library across multiple locations globally poses a challenge. Parts created need to be replicated immediately to all servers located globally and across the firewall too. Deploying toolsets for immediate replication of parts after release across the globe will reduce cycle time, and having any modified parts available dynamically ensures quality and brings the products on time to market. Effective parts search in the library database is a key requirement for quick retrieval and reuse. Implementing IPC-7351, IPC-7251 standards for footprint and padstack naming conventions adds intelligence for storage and retrieval. Adding specific part properties in addition to those reflected in BOM will help locate the exact part required. Deploying process tools meeting QMS requirements will help automate the library part requests, fill creation and QA checklists, update part status live, etc., ensuring quality

The Next ***BIG*** Thing is ***GREEN***

GOOD for the Industry; ***GOOD*** for the Planet

See us at PCB WEST September 12, 2018

Booth 508

GREENSOURCE

FABRICATION

www.greensourcefab.com

process. This talk focuses on the challenges and requirements in PCB library development and management and how these can be effectively addressed.

Who should attend: PCB Designer
Target audience: Intermediate

12:00 noon – 1:00 pm LUNCH-N-LEARN, Sponsored by Streamline Circuits

1:00 PM – 3:00 PM

11: POWER INTEGRITY & DECOUPLING PRIMER FOR PCB DESIGNERS

Ralf Bruening, Zuken

The evolving requirements of new electronic applications in various markets (e.g., automotive, communication, IoT) are forcing engineers to an ongoing improvement of their design processes. The overall performance and the EMC behavior of such electronic systems are determined not only by the design of the circuitry, layout geometry and the IOs, but more these days by the power distribution networks (PDNs). Strict reliability requirements and lack of real estate on such complex systems often prevent first order power integrity countermeasures from the past (e.g., sprinkling the board with 100nF caps). Today's supply voltage decrease with every new silicon generation is contributing to the problem domain in the same amount as the common goal of reducing power consumption of electronic systems does. This and the resulting shrinking noise margins for new ICs define increasing demands for the quality and stability of power supply systems. Hence, tighter requirements and constraints from silicon vendors are defined for the power supply the PCB designers have to follow – in conjunction with tougher decoupling schemes. In this session requirements and the basic of PCB power distribution systems are explained. Issues like plate capacitance, loop inductances and cavity resonance are explained without deep math. Side effects to the signal integrity and EMC domains are shown using illustrated practical examples. Guidelines for a first order covering and resolving power integrity issues are given regardless of the used PCB-design and ECAD process. The how and why of decoupling will be illustrated covering in detail the role of bypass capacitor. Power integrity simulation capabilities will be explained and demonstrated in a generic vendor-neutral manner as a potential problem-solving approach, together with silicon vendor support documents (i.e., constraint and spreadsheet tools) addressing power integrity issues as an essential part of a state-of-the-art PCB design process. Examples from various industries (e.g., automotive) will complement the session with excerpts from practical application experience.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer, Test Engineer
Target audience: Beginner, Intermediate

12: LAYING OUT ANALOG/DIGITAL PLANES

Robert Hanson, Americon

This tutorial will discuss the properties behind ground. This tutorial will address the following questions and more: Which should be used for your design – ground, modified or multipoint ground? What causes near-end and far-end crosstalk, and how is it measured and simulated? Why are solid ground planes best? What is intelligent parts placement, and what is its effect on ground return current? Attendees will learn about the concept of moats/floats/drawbridges, how to layout split planes – CMOS/TTL, PECL, and analog using different biases and also controlling crosstalk, characteristic impedance and cost in 4, 6, 8, and 10-layer stackups using the same bias voltage; how to stack printed circuit board layers (e.g., 4, 6, and 10-layer for Zo and crosstalk control; copper fills on signal layers, minimizing warpage; interplane capacitance: material thickness and selection and stackup placement; SIR vs frequency; software for performing crosstalk; ground bounce tests.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer
Target audience: Intermediate

1:00 PM – 4:30 PM

13: EFFECTIVE PCB DESIGN: TECHNIQUES TO IMPROVE PERFORMANCE

Daniel Beeker, NXP Semiconductor

As IC geometries continue to shrink and switching speeds increase, designing electromagnetic systems and printed circuit boards to meet the required signal integrity and EMC specifications has become even more challenging. A new design methodology is required. Specifically, the utilization of an electromagnetic physics-based design methodology to control the field energy in your design will be discussed. This training module will walk through the development process and provide you with guidelines for building successful, cost-effective printed circuit boards.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer
Target audience: Beginner, Intermediate

14: CIRCUIT GROUNDING TO CONTROL NOISE AND EMI

Rick Hartley, RHartley Enterprises

When a time-varying (AC) current flows, state-changing electric and magnetic fields are present. These fields, when not controlled, are the source of noise and EMI. In recent years, ICs with very fast rise-time outputs have made problems common, even in circuits clocked at low frequencies. Knowing all the basics of proper grounding can contain and control stray fields, making noise and EMI issues virtually nonexistent.

This course will cover the concept of "ground," location of fields in the PCB, when is a circuit a waveguide, where high- and low-frequency currents flow, keys to controlling common mode EMI, cables and other radiators, source control of EMI, effects of IC style and packaging, impact of connector pin-out, effect of component positions on EMI, planes and plane islands in the PCB (to split or not to split ground), routing to control noise, routing and the I/O structure, board stack-up, I/O filtering and blocking for single-ended and differential lines.

Who should attend: PCB Designer, Circuit/Hardware Engineer, SI Engineer, System Engineer
Target audience: Intermediate

KINWONG

景旺电子

7 Dedicated Factories in China:

Shenzhen	Longchuan	Jiangxi
PCB	PCB	PCB
FPC	FPC+SMT	PCB 2.0
	MPCB	

Technology Types:

Rigid-Flex	Metal Core
HDI	High-Frequency
PCB & Flex	Advanced Materials

Contact Us:

Mike Tucker - mike.tucker@kinwong.com (US)

Armando De Vera - armando.devera@kinwong.com (Mexico)

Arturo Mora - arturo.mora@kinwong.com (Mexico)

Local Technical Support in *USA, Mexico and Europe*

please visit us at

Booth 103

www.kinwong.com

3:00 PM – 4:00 PM

15. THERMAL INTEGRITY WITHIN AN ELECTRICAL DESIGN FLOW

James DeLap, Steven G. Pytel Jr. and Mehdi Abarham, Ansys

Modern design requirements necessitate a workflow that allows for free-flowing information and iterations between electrical, thermal, and mechanical design teams. This workshop will explore new simulation tools that enable electrical and thermal co-design and optimization, as well as showcasing best practices for dealing with electrical and mechanical CAD (ECAD and MCAD) files. The workshop targets electrical engineers, providing them an overview of basic thermal dynamics, heat transfer modes, power delivery/consumption optimization in ECAD/MCAD, while keeping the focus on how to identify problematic designs early, thereby creating a collaborative working environment with mechanical engineers.

Who should attend: PCB Designer, System Designer, Hardware Engineer

Target audience: Intermediate

3:00 PM – 5:00 PM

16: HOW TO FIGHT MAGNETIC NOISE GREMLINS

Keven Coates, Geospace

Have you ever had a noise-sensitive circuit and tried to find the noise source? Even after you completely encased sensitive portions in all sorts of shielding, you still had noise? It's very possible this is magnetic noise. Lower frequency magnetic fields can't be contained and shielded against in the same way electric fields can. In this presentation, hear about the author's nine-month long battle with a specific magnetic noise issue, the best tools to fight it, twisted pair, current loops, and the best ways to test for and defeat magnetic noise in your designs.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer

Target audience: Beginner, Intermediate, Advanced

WEDNESDAY, SEPTEMBER 12

8:00 am CONFERENCE COFFEE BREAK, Sponsored by Sierra Circuits

8:30 AM – 12 NOON

17: THE COMPLEXITIES OF FINE PITCH BGA DESIGN

Susy Webb, Fairfield Industries

Designing with BGAs is much more challenging than in the past! The ball pitches are going down, and the total pin counts and package size are going up, making everything more complex. With those changes, the signal integrity and EMI issues become more profound; the fanout and routing are much more challenging, and the power connections more difficult. Add to that the manufacturing concerns that have surfaced from small pad openings and tiny capacitors, and the designer has to face some real complex issues. In this presentation, we will discuss all of those things and more, including choosing effective BGAs, placement for components and caps, grid systems for parts and routing, through-hole and microvia fanout possibilities, and some manufacturing issues unique to these kinds of designs. This class has a lot of illustrations and examples!

Who should attend: PCB Designer

Target audience: Beginner, Intermediate, Advanced

9:00 AM TO 10:00 AM

18: PCB REVERSE ENGINEERING COUNTERMEASURES

Jeremy Hong, Hong's Electronics

Designing circuits and laying out a printed circuit board (PCB) can be a complicated and intensive process. Design engineers use many shortcuts and tricks to cut costs and time of development. As it turns out, many of these shortcuts and tricks can lead to security flaws in a product. Working on both sides, design and reverse engineering, it has been found that implementing security and countermeasures on PCBs are the last priority for design engineers – and sometimes totally ignored. This is apparent in the design of IoT (Internet of things) devices. This presentation points out some fundamental aspects of the hardware design engineering process that can lead to hardware vulnerabilities.

Who should attend: PCB Designer, System Designer, Hardware Engineer, Test Engineer

Target audience: Beginner, Intermediate

9:00 AM TO 11:00 AM

19: MULTI-BOARD DESIGN: CASTELLATION, CONNECTION, SI, ALIGNMENT

Ben Jordan, Altium

Aesthetics, ergonomics and industrial form are paramount design objectives, as new products must appeal to attention-starved consumer audiences. Intelligent people increasingly crave intelligent products. The desire to maximize production efficiency by consolidating all the electronics onto one board is at odds with higher mechanical design priorities. Add to that the desire markets inherently develop for configurations and optional extras, and it's hard to avoid a multi-board design approach. This technical session presents practical approaches to multi-board system-level PCB design, including partition boundaries, subcircuit relocation, interconnect methods, panels and layer stacks, and mechanical integration with enclosure design. We will also cover potential disaster areas and ways to avoid pitfalls, how to effectively manage connectivity, and improve manufacturing outputs for unambiguous fabrication and assembly. Specific topics discussed will be multiboard methodologies overview; partitioning; connectors for board to board; castellated module design approach for IPC-A-610G quality compliance; multiboard signal and power integrity issues; module form factor overview pros and cons; connectivity management and signal probing; 3-D mechanical integration and assembly management. Methods presented in this workshop are extensible and applicable to any toolset or workflow.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer

Target audience: Beginner, Intermediate, Advanced

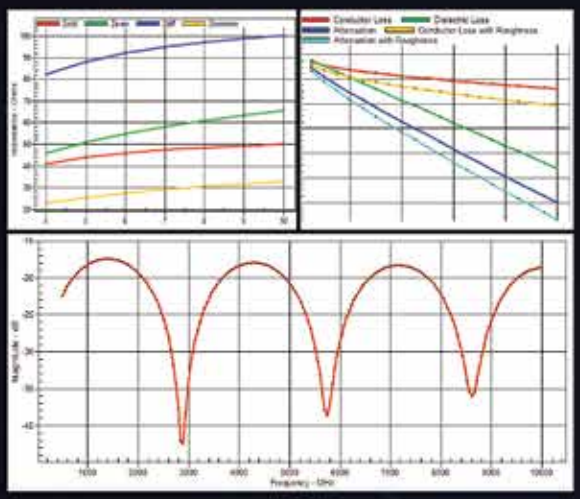
Professional Tools for

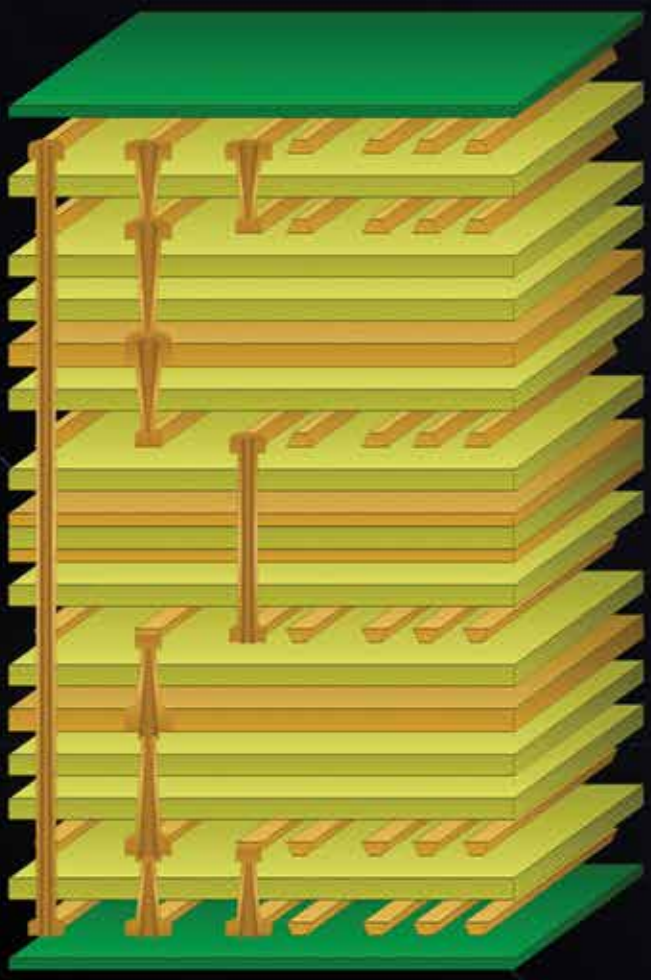
PCB Design and Manufacture

Stack Design

Rigid-Flex

Field Solvers

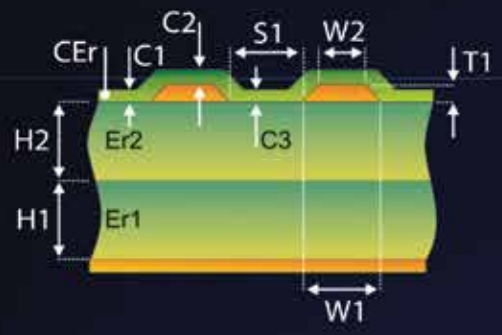




Impedance Measurement

Copper Roughness

Insertion Loss



Thursday conference attendees are invited to join us at the Polar Lunch-n-Learn

Polar

BOOTH 401

polarinstruments.com

20: AN INTUITIVE APPROACH TO UNDERSTANDING BASIC HIGH-SPEED LAYOUT

Keven Coates, Geospace

What is a wire? At high speeds, it behaves very differently from what we were taught in college! This is a presentation on high-speed basics that helps make the subject intuitive in a way that's never been presented before. Learn about how frequency enters the picture, high-speed signal propagation, impedance, noise, and reflections with easy-to-understand animations and analogies to understand this subject on a deeper level.

Who should attend: PCB Designer, System Designer, Hardware Engineer
Target audience: Beginner

21: A BEGINNER'S INTRODUCTION TO PCB TRACE IMPEDANCE

Ken Taylor, Polar Instruments

What is impedance anyway, what causes it, why does it matter, and what happens if we get it wrong? This entry-level presentation describes the component properties of a PCB trace (a transmission line) that come together to determine the impedance. Maybe surprisingly, impedance is experienced in various other forms every day, probably every minute of every day. Most people never thought of it that way. This presentation begins by briefly identifying and acknowledging those experiences, and relates them to the electrical transmission line and its component parts and their characteristics. Next, it looks at the transmitted signal as it progresses from the signal source into the line, as it propagates along the line, and what happens when it eventually reaches the end of the line – depending on how the line is terminated: open/short/matched/mismatched. The mathematics will be kept simple, nothing worse than x = a.y or similar and, of course, the good old square root. A brief review of frequency-dependent problems of dielectric loss (signal energy lost to the line's surrounding environment) and copper loss (signal energy lost to the copper conductor) might be included.

Who should attend: Fabricator Engineer/Operator, Assembly Engineer/Operator, Other
Target audience: Beginner

9:00 AM – 5:00 PM

22: COST REDUCTION THROUGH DESIGN FOR MANUFACTURING AND ASSEMBLY

Gary Ferrari, FTG Circuits

Technologies such as lead-free, small pitch BGAs, microvias, embedded passives, controlled impedance, and EMI present manufacturing challenges that must be addressed by today's designers, not to mention increased costs. It is easy to blame escalating costs on these technologies. Much of the blame may be attributed to a lack of understanding of the manufacturability rules associated with these technologies, however. Designers should be designing for the most cost-effective product without sacrificing performance.

Cost reduction, by design, forms the fundamental building blocks for this session. This session will be divided between lectures and interactive discussion groups. These groups will explore, under guidance, material issues for lead and lead-free environments, high performance, HDI, assembly, and surface finishes for various environments. There will be ample time allocated to look at individual challenges faced by the attendees.

Attendees will gain a clear understanding of overall DfM issues, cost drivers, how to apply DfM concepts to specific designs, and the notes that should be placed on fabrication drawings.

Who should attend: PCB Designer, Electrical Engineer
Target audience: Intermediate, Advanced

23: THE COMPLETE GUIDE TO UNDERSTANDING TRANSMISSION LINES

Robert Hanson, Americon

Fundamentals • Frequency, time, and distance • Lumped versus distributed systems • EM fields • Geometry, C, L, and Zo interrelationships • C&L resonance transmission line characteristics • The quality factor, Q, and why lumped circuits can ring and cause EMI • Infinite uniform transmission line • Effects of source and load impedance • Special transmission line cases • Determining line impedance and propagation delay using TDR and VNA • Skin/proximity effect and dielectric loss • The capacitive load: Zo and propagation delay • Matching Zo with trace alterations (neck-downs): minimizing the C load • 90°, 45° bends: are they concerns? • Characteristics of T lines: coax, pair, micro strip, buried micro strip, stripline and differential: asymmetric, dual, edge.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer
Target audience: Intermediate

10:00 am – 6:00 pm EXHBITION FLOOR OPEN

10:00 am – 2:00 pm BOOTH BARISTA, Sponsored by Zuken

10:00 AM – 12:00 NOON

24: IPHONE X – STEVE JOBS' IPHONE

Bill Cardoso, Creative Electron

It's been 10 years since Steve Jobs introduced the iPhone to the world. Much has happened since then. Over this past decade, the iPhone became a reference design, and the object of desire of a legion of fans who wait anxiously for every launch of the Cupertino company. Undoubtedly, the most advanced iPhone on the market today, the iPhone X is a technology marvel. The double-stacked boards, dual battery, and a face recognition sensor bring the iPhone X to a whole different level. In this presentation, we'll explore these technological advances during a live teardown of the iPhone X. The teardown will be followed by detailed coverage of the technical details of critical parts of the device. This live teardown will be accompanied by x-ray and CT images of the iPhone X, so the audience will get unprecedented insights on what makes this iPhone tick. More important, we will explore the assembly process utilized to put the iPhone X together. This presentation is targeted at a wide technical audience looking for a better understanding on how advanced consumer electronics are designed and assembled.

Who should attend: System Designer, Hardware Engineer, SI Engineer, Fabricator Engineer/Operator, Assembly Engineer/Operator, Test Engineer
Target audience: Beginner

FEELING 'BOARD'?

BOOK A TOUR WITH US!

GET A BEHIND THE SCENES LOOK AT OUR AWARD WINNING FACILITIES!

Visit Us At Booth 408

To schedule your visit, call us at **(800) 763.7503**
or send an email to **sierratours@protoexpress.com**

11:00 AM – 12 NOON

25: CONTINUING TEST POINT MANAGEMENT THROUGHOUT A PCB DESIGN FLOW

Mark Laing, Mentor

At PCB West 2017 I presented how design for test (DfT) needed to become proactive in the PCB design flow. This paper focused on starting DfT analysis as part of the schematic capture phase and not leaving it until late in the layout phase. This presentation will continue this theme, and discuss how PCB layout can further enable improvements in testability and DfT, with ongoing test point management as the next logical step from schematic capture. Existing layouts will be reviewed for testability coverage to find ways they can also be improved in subsequent design revisions.

Who should attend: PCB Designer, Fabricator Engineer/Operator, Assembly Engineer/Operator, Test Engineer

Target audience: Intermediate

26: CLOCK JITTER BEHAVIOR ON DIFFERENT PCB LAYOUT APPROACH

Marcus Miguel Villaflores Vicedo, Analog Devices

Clock signal in a PCB spectrum experiences degradation in the form of clock jitters, broadly known as timing deviation. Jitters limit the maximum SNR that can be achieved, especially in the case of ADC devices. Inherent system properties, such as length of the traces and the frequency of operation, contribute to the timing deviation on the signal. PCB design implementation techniques should be evaluated to determine the effective method to reduce clock jitter. Isolating the jitter aggravators calls for eight unique case setups representing the hypothetical stimulus of noise. These setups were derived from the variable matrix: length of trace, guard shielding, and layer-transposition in the design. This talk only supports deterministic jitter (dJ) analysis; any random Gaussian jitter (rJ) that exists on the real-world setups was disregarded. Each case was subjected to simulation, mapping the phase difference graph. Scattering parameters were also plotted to evaluate each setup's noise performances. Results support the profound effect of trace lengths in the phase difference in each case. Cases subjected to the trace lengths of both extremes give a nonlinear variation, but with relative degree separation in which longer lengths contribute more jitter to the signal. This concludes the rationale of increasing the proximity for T(x) and R(x) lines in clock signal lines. Phase difference on each group of lengths shows consistency, solidifying the matched length effect. Return loss slightly differs between cases of same length and different topology. Hence, different best-design topology does not give drastic advancement or deterioration to the clock performance in comparison within each other. Same goes with insertion loss performance, showing slightly varying results on each grouped trace lengths. This goes to show performance was almost consistent on all types of best layout practices, and only the trace lengths contribute highly to clock jitter.

Who should attend: PCB Designer

Target audience: Intermediate

27: ECAD-MCAD CO-DESIGN FOR A COMPETITIVE ADVANTAGE

John McMillan, Mentor

Many design teams struggle to reduce product development schedules and improve time-to-market. In a recent survey, the need to improve time-to-market was identified as a primary business objective, ahead of the need to reduce product cost and improve product quality. Asked about initiatives to accelerate time-to-market, the leading response was to improve communication and collaboration across engineering. If you were to push down further into a methodology to implement this initiative, you would find that improving ECAD-MCAD collaboration not only reduces product development time, thereby improving time-to-market, it also provides a sustainable competitive advantage for your design team. During this session we will discuss how an efficient ECAD-MCAD co-design process can be an enabler for design teams to eliminate costly electro-mechanical issues during new product development. We will look at the innovative solutions available in the latest generation of software technology and how they can help your team obtain a sustainable competitive advantage. Recommended best practices and a summary of the benefits associated with an optimized ECAD-MCAD collaboration process will be reviewed and discussed.

Who should attend: PCB Designer, Other

Target audience: Beginner

12:00 noon – 1:00 pm LUNCH on the Exhibit Floor, Sponsored by Sierra Circuits

1:00 PM – 3:00 PM

28: THERMAL DESIGN CONSIDERATIONS FOR SMD PCBS

Keven Coates, Geospace

By now everyone has seen those nice aluminum core PCBs that dissipate heat fantastically, but what do you do when all you have to work with is FR-4 and SMD components? How do you keep those MOSFETs and faster processors cool? How are semiconductor packages designed to dissipate heat? What's the best way to utilize that? This class will cover understanding thermal resistance, how airflow affects things, good design goals, estimating junction temperature, and how to pick the right components to minimize the temperature of your design and therefore maximize reliability.

Who should attend: PCB Designer, System Designer, Hardware Engineer

Target audience: Beginner, Intermediate

29: SIGNAL ATTENUATION IN VERY HIGH SPEED CIRCUITS

Rick Hartley, RHartley Enterprises

In all high-speed/high-frequency circuits, signal integrity is dependent on a number of variables, all of which accumulate to impact the noise budget of the circuit. With very high-speed circuits, an even larger number of issues come into play, and all the effects are more extreme. Some problems are driven by design deficiencies, some by the physical structure and design of the ICs, and still more are driven by the PCB's copper style and base material parameters.

This course will outline all the effects impacting signal integrity at very high speeds and will detail such items as via stubs, jitter, inter-symbol interference, impact of copper style on skin effect, loss tangent, impact of layer change during routing and other major signal integrity concerns, as well as the impact some of these items have on timing and the Y-axis attenuation of signal eyes. Also discussed will be solutions to these issues, including some excellent high-speed base materials.

Who should attend: Circuit/Hardware Engineer, SI Engineer, PCB Designer, System Engineer

Target audience: Intermediate, Advanced

STREAMLINE CIRCUITS
TIME AND TECHNOLOGY EXPERTS

Booth #510

Military Grade PCB Mfg.

Rigid, Rigid-Flex, Multilayer Flex

NIST Certified

Industries Served

- Military
- Aerospace
- Medical
- Telecommunications
- DataComm
- Industrial
- Consumer

Certifications

- NIST-800-171
- MIL-PRF-31032
- AS9100 rev. C
- ISO9001
- ITAR
- ISO13485
- Nadcap

Capabilities

- 70 layers (12+ Stacked Vias)
- 9+Lamination Cycle (Blind and Buried)
- IPC 6012/B Class 3 with Copper Wrap
- 3.23 Mil Hole to Copper Technology
- Flat Copper/ Epoxy Filled Vias
- 1.6 Mil Laser Vias
- 3 Mil Mechanical Drills
- .08 MM BGAs
- Cavity Constructions
- 6 oz + Copper Thickness
- Copper Filled Vias

MIL-PRF-31032
Certified

1:00 PM – 4:30 PM

30: HDI ROUTING SOLUTIONS
Susy Webb, Fairfield Industries

With the pitch of parts getting smaller and pin count getting larger, there is a need to get as much routing as possible into very small areas of the PCB. HDI will help accomplish this, but the technology requires some different setup and thought as to what is needed. One has to decide on design priorities, complexity needed, cost required or allowed, the type and size of vias, best via patterns to use, and how signals, power and ground will move from one layer to another. Additionally, the layer structure, impedance, signal return, and layer paired routing all must be considered for signal integrity and EMI control, and a general understanding of manufacturability is needed. We will discuss all those things, the electronics involved, different ways to accomplish the routing, and offer many examples and pictures of how to work with them to reach our goals.

Who should attend: PCB Designer
Target audience: Beginner, Intermediate, Advanced

31: THE BASICS OF PCB FABRICATION (101)
Paul Cooke, FTG Circuits

With ever-decreasing geometries and increased density, today's PCBs are extremely complex. This seminar looks at how a PCB is fabricated, and the challenges the fabricator faces to achieve the design intent and meet the customer and industry standards. We will examine the processes needed to form microvias, image µBGAs, plate copper in holes the thickness of a human hair, and select surface finishes needed for very fine-pitch components. The half-day seminar will be interactive to ensure all questions related to PCB fabrication are answered.

Who should attend: PCB Designer, Fabricator Engineer/Operator, Assembly Engineer/Operator, Test Engineer
Target audience: Beginner

3:00 PM – 5:00 PM

32: DIFFERENTIAL PAIR ROUTING FOR SI CONTROL
Rick Hartley, RHartley Enterprises

Differential pairs have been used in PCBs for years to carry high-speed serial and high-speed parallel data, in a variety of bus formats. Many board designers and engineers believe the rules for differential pairs are the same in a printed circuit board as they are in a cable or a twisted pair of wires. This is not the case!

This course will cover the advantages of differential pairs vs., single-ended lines, which differential pair format gives the best impedance control, what is the right spacing between the lines of a pair, crosstalk between differential pairs, what's important in differential pair routing, how much skew (line length mismatch) is really acceptable, the impact of material type and the impact of vias on signal integrity and EMI.

Who should attend: Circuit/Hardware Engineer, SI Engineer, PCB Designer, System Engineer
Target audience: Intermediate

33: EVALUATING THE VIA TRANSITION THROUGH TDR SIMULATION
Richard Villamor Legaspino, Analog Devices

As PCBs become dense, routing high-speed digital (HSD) traces in a single layer has become complicated. Now most of the layout designs use at least two layers for routing these kinds of signals (RF and HSD). The speaker looks at the effects of having stubs in designs, and further improving it by removing the stubs and controlling the vertical interconnect access (VIA) using a 50 Ohm coaxial approach. Trace-to-vertical interconnect access (VIA) transition has been a common issue in high-speed digital PCB designs and applications. The speaker looks at the effects of having stubs in designs, and further improving it by removing the stubs and controlling the VIA using a 50 Ohm coaxial approach. The speaker explores the five different VIA transitions and the effects of each specific method applied to it using EMPro (electro-magnetic professional) FDTD (finite difference time domain) TDR (time domain reflectometry) simulation in correlation to an actual design. The speaker used a 3-D simulation tool, which is EMPro, using FDTD Solver for TDR and FEM (finite element method) for S-parameter analysis. The speaker fabricated a simple circuit board design using a micro-strip single-ended trace to via transition for correlation.

Who should attend: PCB Designer
Target audience: Intermediate

FREE WEDNESDAY

9:00 AM – 11:00 AM

F1: ROUTING & TERMINATION FOR CONTROL OF SIGNAL INTEGRITY
Rick Hartley, RHartley Enterprises

IC output rise time contributes more heavily to loss of signal quality than the clock frequency of the circuit. Since most ICs today have rise and fall times under 1.0 nanosecond, many engineers and printed circuit designers find themselves fighting signal integrity problems in circuits being clocked in the low to mid tens of megahertz. Traces on circuit boards with rapid rise and fall times are referred to as high-speed transmission lines. The single greatest contributor to signal integrity issues is the lack of proper routing of lines, lack of poor control of impedance and the lack of proper termination.

This course will focus on the issues PCB designers and engineers need to know when designing with today's "high-speed" components. Topics include: At what length a line is high speed, line length's effect on signal integrity when proper routing is not implemented, understanding and controlling line impedance, PCB material impact on impedance, long "Ts" in lines, routing schemes that work, when to terminate a line, proper termination of the line, when termination is not needed and board stack-up.

Who should attend: Circuit/Hardware Engineer, SI Engineer, PCB Designer, System Engineer
Target audience: Beginner, Intermediate

9:00 AM – 10:00 AM

F2: HDI: HIGH DENSITY INTERCONNECT
Chris Nuttall, NCAB Group

How do I get started with HDI? This session explains what defines an HDI board, standards, design rules, and driving forces for HDI.

Who should attend: PCB Designer, System Designer, Hardware Engineer, Test Engineer, Other
Target audience: Intermediate, Advanced

JOIN US AT THE SUMMIT

BOOTH 210

ADVANCED TECHNOLOGY PCBS

RIGID, FLEX, RIGID-FLEX, RF/MICROWAVE

COMPLEX HDI, SEQUENTIAL LAMINATION, BBV, BURIED RESISTORS, METAL BACKED AND METAL CORE

QUICK TURN THROUGH PRODUCTION

SUMMIT INTERCONNECT

www.summit-pcb.com

10:00 AM – 11:00 AM

F3: AI AND MACHINE LEARNING DISRUPTING THE MANUFACTURING OF YOUR PRODUCTS

Albert Yanez, AsteelFlash

In manufacturing, we work systematically at ways to save time while maintaining the highest yields. This has been evident over the past 50 years, as methodologies were born that would help streamline operations and indoctrinate staff. These have helped form today's best practices, followed in every modern manufacturing company globally. These processes and systems can be seen in the assembly line, such as TQM (Total Quality Management), Six Sigma and Lean. We also know future products will be even more design savvy, with intricate and custom fabrication methods and materials. From diagnostics equipment through to the most advanced automotive systems, we could see what was needed to outpace, while providing no decrease in quality. Then, we considered the challenges our clients face forecasting, dealing with supply-chain concerns and distributing key materials as end-products require. We needed a manpower automation solution that could help with indirect labor and lend a hand in production. We wanted to automate indirect labor functions over time, with the goal of maturing into a 50/50 machine-to-human task force ratio. This would allow us to maintain a "mentor" role over the systems, while having an unlimited workforce on call. Today, we are in the early stages of bringing online portions of the intelligence and weaving them into the daily routines of current team members. Using Neural's proprietary methodologies, we targeted chunks of these identified networks, and follow system deployment processes to maintain quality adherence. To help with transformation, we utilize an advanced onboarding concept where we operate as a startup within our own company, consuming the processes internally via Smith (SM) (the Artificial Intelligence), to maintain control during the Neural Corps' Apprentice to Mentor model. We set out to increase our workforce, save time on human processes, and decrease human-to-human networks, which would allow us endless capacity and increased communication speed, which were previously staffed by human-based roles. Smith can provide value in directly realized time equivalent of hundreds of man hours. As it is trained, it evolves, and in time will take on additional duties and solve more problems.

Who should attend: PCB Designer, System Designer, Hardware Engineer, Assembly Engineer/Operator
Target audience: Beginner, Intermediate

11:00 AM – 12:00 NOON

KEYNOTE: IS PAST PROLOGUE? THE FUTURE OF THE PCB DESIGN INDUSTRY

Walden Rhines, Mentor

From Racal-Redac's initial release of a PCB and schematic software nearly 50 years, much has changed in the electronics hardware design space. Routing has become shape-based and automated. Features like component libraries, panelization, design for manufacturing and design rule checks are now the norm. Simulation and analysis tools have been developed and bolted on. And bare boards are no longer conceptualized independently, but rather considered as part of the full system.

As much as the tools have changed, so has the industry itself. Starting as offshoots of larger OEMs, then evolving to a broad mix of independent software developers – some large publicly traded entities, some tiny firms – the tool industry has of late seen consolidation. How have the technology changes influenced consolidation? And as mega-mergers such as Siemens' acquisition of Mentor Graphics take place, will the companies that make tomorrow's tools once again be parts of large, multinational conglomerates?

Perhaps no one is better positioned to chart the course of these industry changes than Wally Rhines. Rhines led Mentor for more than 24 years, making him easily the longest-tenured executive in PCB industry history. In this one-of-a-kind keynote address, Rhines will recap the PCB design industry timeline, from its unheralded early days to its current prominence. And he will lay out Siemens' strategy for Mentor, and how it will shape the industry at large.

F4: DESIGNING IN THE AGE OF PROTOTYPES

Milan Shah, Royal Circuits

We live in an increasingly connected world with new electronics products introduced every day. From coast to coast, engineers are designing everything from life-changing medical devices to new military technology to one-of-a-kind experiments for launch into space. To stay ahead of competitors, companies must be innovative and quick to market. And once a product is launched, designers must immediately start working on the next revision. PCB prototypes play a critical role in this design-revise-design product lifecycle. Prototypes are the first step in bringing new ideas. Yet, getting PCB prototypes fabricated and assembled correctly on-time and on-budget is a challenge. In this panel presentation, three CEOs from some of the industry's most respected PCB prototype manufacturing companies will discuss the challenges of PCB prototypes. Executive speakers will be Milan Shan, president of Royal Circuit Solutions; Lawrence Davis, president of Advanced Assembly, and Scott Kohno, president of Royal Flex Circuits. Drawing on nearly 45 combined years in the industry, these executives will also share practical tips, advice and resources on how to get PCB prototypes manufactured on-time and on-budget. Topics to be covered include the latest trends in PCB prototyping; growing usage of flex prototype circuit boards; common PCB fabrication and assembly mistakes; cost-saving design tips; review of different types of PCB prototyping services.

Who should attend: PCB Designer
Target audience: Beginner, Intermediate, Advanced

1:00 PM TO 2:00 PM

F5: INDUSTRY 4.0 AND IPC-2581

Hemant Shah, IPC-2581 Consortium

Listen to experts from the IPC-2581 Consortium and from IPC-Connected Factory Exchange (CFX) group about Industry 4.0 and what role IPC-2581 plays in it.

Who should attend: PCB Designer
Target audience: Beginner, Intermediate, Advanced

1:00 PM – 3:00 PM

F6: THE 10+ 21 MOST COMMON DESIGN ERRORS CAUGHT BY FABRICATION (AND HOW TO PREVENT THEM)

David Hoover, TTM Technologies

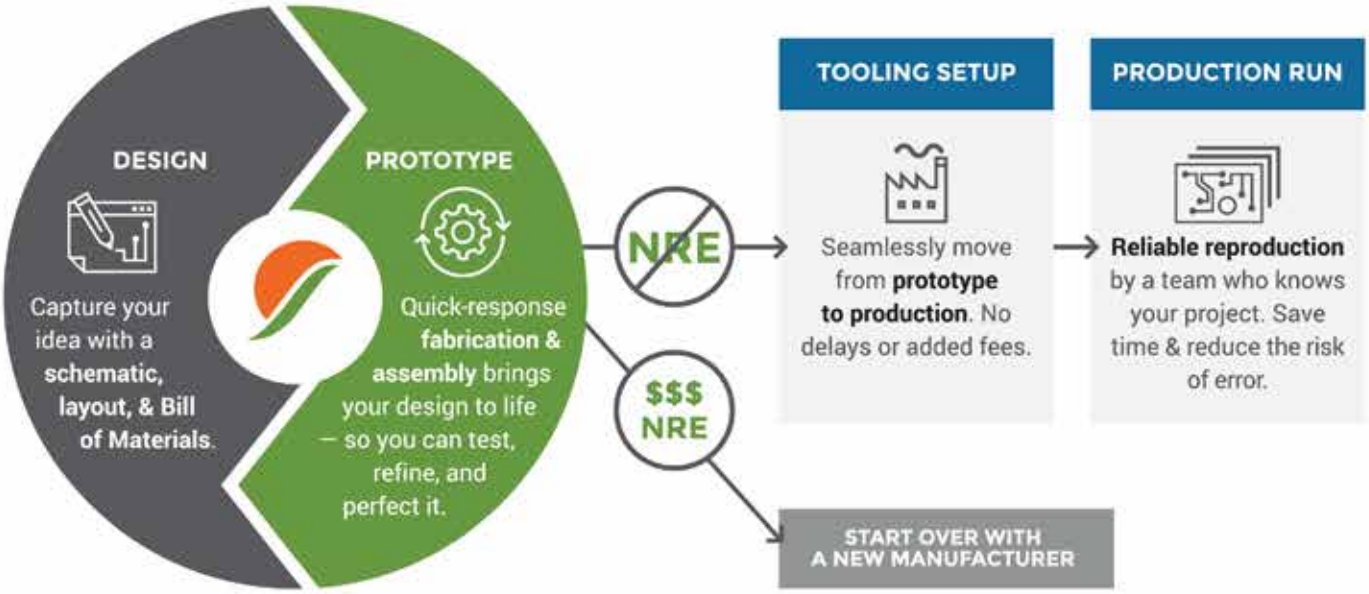
In preparation for this presentation, we talked to many of the largest PCB manufacturers in the US and abroad. We then developed a list of the most common errors found on incoming designs. We started with 10 and now, based on popular demand, we've expanded and keep updating that list! We look at each of the errors and discuss ways to find them before the designs are sent out for manufacturing. Methods we will look at include netlist comparison, design for manufacturing, and design rule analysis. We encourage attendee participation and ask folks to bring their challenges for discussion. After this seminar, the PCB designer will take back some knowledge to better assist them in using their existing tools in the market to produce better and more accurate designs.

Who should attend: PCB Designer, Fabricator Engineer/Operator
Target audience: Beginner, Intermediate

SUNSTONE CIRCUITS

Visit Us At Booth 311

GUARANTEED QUALITY *from* PROTOTYPE TO PRODUCTION



Begin with a **design**, create a **prototype**, and move into **production**, all in one place.

Sunstone is your path to *peace of mind*.

DID YOU KNOW WE OFFER:

- Assembly
- Layout
- CAD Software with SnapEDA
- RF/Microwave
- DFM
- Solder Stencils

LIVE & ON-SITE 24/7/365 CUSTOMER SUPPORT

Contact us at: 1-800-228-8198 or via e-mail at support@sunstone.com

2:00 PM – 3:00 PM

F7: EFFICIENT PCB INTERPOSER DESIGN USING A NOVEL SMART ROUTER BASED ON NEURAL NETWORKS AND GENETIC ALGORITHMS

Xiao Ming Gao, Naveid M. Rahmatullah and Taylor Hogan, Intel

As the complexity and variety of system-on-chip (SOC) and IP development increase, the platforms used to validate silicon electrical and functional performances are becoming increasingly difficult, due to time-to-market and cost constraints. To completely validate these SOC IPs, different platforms have to be designed to target different market segment requirements. Often the time to launch is critical to make sure it will not miss market opportunities. To meet these challenges, the interposers can provide flexible and low-cost solutions. It can be used to adapt silicon to a variety of platforms without changing existing designs and therefore maximize the return on investments. For example, the N-1 interposer is a special kind of PCB adapter that allows prior generation chip, the N-1 silicon to be installed on a current generation system, the N platform for validations. This facilitates platform checkout and deployment before new silicon arrival, enabling early shift left platform strategy, such as Firmware development, BIOS, and test and validation collateral developments. The design of N-1 interposer involves a few steps. First is to collect requirements and define the pin mapping between N and N-1 generation silicon. Next is to use scripts to generate netlist using this mapping file. Finally, define the board stackup and create constraints to route these connections. The last step is always labor-intensive and time-consuming because interposer board size is usually very small, and the package has more than a thousand pins, so the High Density Interconnect (HDI) design has to be used. A combination of irregular routing patterns and constraints on critical signals is beyond the capacity of the most modern automatic routing systems, and the routings have to reply on manual interactive layout. To improve the efficiency, we propose a new machine-learning-based routing algorithm. Multiple routing strategies can be run in parallel to help search the solution space of its domain. Each phase is essentially an optimization problem, and we use a Genetic Optimization engine that concurrently searches through multiple design options looking for the global best. We propose using a deep neural net as the fitness function. This neural net is trained by analyzing the features of previous successful design patterns, using hard-coded heuristics, such as crossovers, length, and congestion. Leveraging this process parallel mechanism, multi-core CPU and clusters-based computing resources can be used to evaluate multiple routing strategies at the same time. We have used the new autorouter to test both CPU and PCH N-1 interposers' layouts. The routing time is reduced from a week of manual routing to only a couple hours using the new router. The course will provide a complete interposer design flow from pin mapping, netlist generation, to final PCB component placement and routing. Focus especially on how to effectively use the proposed smart router to drastically reduce layout time and improve design quality.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer, Test Engineer

Target audience: Beginner, Intermediate, Advanced

3:00 PM – 4:00 PM

F8: OPTIMIZING HARDWARE FOR YOUR IOT SOLUTION

Sean Priddy, Creation Technologies

Most of the IoT hype is about how billions of devices will generate huge data streams that must be communicated, stored, and analyzed to provide operational visibility and insights using machine learning and AI over time and large data sets. However, often neglected is the actual hardware required to acquire sensor data, process the data, react to the data, and communicate the data over a network to other devices or the cloud. Frequently, emerging IoT solutions require the development of specialized hardware to accommodate various environmental, processing, localized storage, power, and networking requirements. Learn how to make the appropriate technical choices so your hardware is optimized for your IoT solution.

Who should attend: PCB Designer, System Designer, Hardware Engineer

Target audience: Beginner

F9: PANEL: THE FUTURE OF PCB ENGINEERS

Phil Marcoux, PPM, Moderator

A common comment from everyone involved in electronics supply chain today is the chronic "graying" of the industry, meaning a lack of younger engineers and professionals. Is this a truism? And what recruiting and management techniques are needed to attract – and keep – the millennials? Panelists include Joel Camarda, Amonix, and others.

4:00 PM – 5:00 PM

F10: 3D PRINTED ELECTRONICS: A NEW DIMENSION IN PROTOTYPING & MANUFACTURING

Simon Fried, Nano Dimension

3D printed electronics technologies are enabling developers to go from idea to working prototype in just days to enable agile electronics development and innovation. By iterating electronic circuits rapidly in-house, 3D printing will transform electronics development and manufacturing processes. During this session, delegates will learn about the disruptive and transformative effect of 3D printing on electronics design and manufacturing, specifically for the aerospace and defense sector. Understand the challenges and technological advancements needed to achieve next-gen 3D printed electronics that ensure high performance and reliability to meet aerospace and defense industry specifications and standards. Determine the scope of 3D printed electronics for a competitive business strategy, and understand how this technology is creating enhanced workflows, improved time to market and agile hardware development processes. Determine how to introduce agile electronics development processes at every prototyping stage to reduce time-to-market, increase innovation and keep proprietary design information in-house.

Who should attend: PCB Designer, Hardware Engineer, Test Engineer

Target audience: Beginner, Intermediate

F11: PANEL: UNDERSTANDING THE AS9100D STANDARD

Peter Bigelow, IMI, Moderator

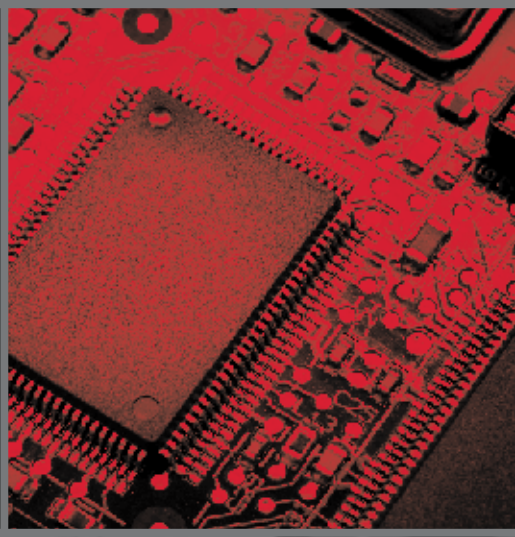
Confusion appears to be growing throughout the supply chain, as it attempts to sort out just how often first article inspection needs to be performed. Manufacturers and their customers face both additional evaluations and a data avalanche, the result of the surge in acceptable quality limit (AQL) samples of FAI measurements as supplied to the customer, which then must enter, sort and distribute (as needed) all that data. It is one thing to impose requirements on suppliers, but in the case of AS9100D, those requirements might be backflowing. Is FAI the QA engineer's revenge? How much inspection is too much? How do you make it work for your supply chain? And does the standard need to change?

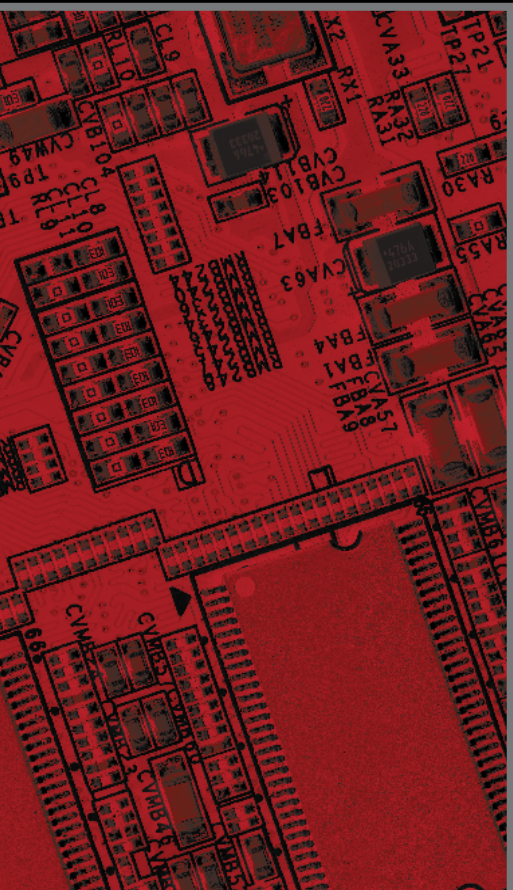
World's Largest PCB CAD Library

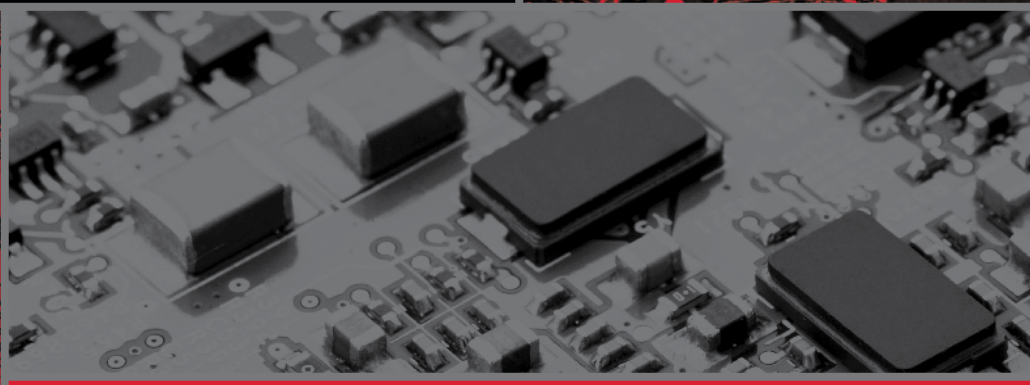
Did we mention it's also FREE?

As an engineer, you already have a million things on your plate. Why make building, sourcing, and verifying CAD libraries one of them? Our massive library of verified PCB symbols, footprints, and 3D models is the solution you have been waiting for. Search, find, and instantly download models in over 20 PCB CAD formats. Let us handle your CAD libraries so you can focus on building the next big thing.

Get Your Parts Today ››







Visit Us At PCB West Booth #509

Ultra Librarian™

CAD TOOL CORNER – FREE!

1:00 PM – 2:00 PM

C1: ENSURE YOUR ELECTRONIC DESIGN IS RELIABLE AND ROBUST BY SIMULATION – DURING SCHEMATIC, BEFORE MANUFACTURING AND TESTING

Yizhak Bot, BQR

To verify that electronic boards are free of hidden design errors, manufacturers perform qualification and integration tests before manufacturing. If failures are detected, the manufacturer implements a root cause analysis to detect the design fault, and then turns to redesign, remanufacturing and retesting. These time-consuming efforts delay the product launch and cause the project's budget to overflow, possibly even leading to project cancellation. In this talk we will describe a new method that will detect hidden design errors by simulation in the schematic phase just before layout, manufacturing, qualification or integration tests. Using the simulator, it is possible to locate hidden design errors that may be discovered as late as during customer use. It also enables tracking of faults in existing products that already operate in the field and are used by customers. An example is a product comprising dozens of PCBs that has been operating in the field for several years, which failed suddenly. During the simulation, the cause of the failure was discovered, and the client verified it in the laboratory. Ostensibly, if the simulation had been performed on time, the problem would be entirely avoided.

Who should attend: PCB Designer, Hardware Engineer, Test Engineer
Target audience: Beginner, Intermediate, Advanced

2:00 PM – 3:00 PM

C2: RETARGETING YOUR LIBRARIES FOR NEWER, BETTER PROCESSES WITHOUT BREAKING YOUR BANK

Vince Di Lello, Cadence Design Systems

Libraries hold a company's IP, most companies will say. Libraries are built for a process that gets outdated. Manufacturing advances and newer fabrication techniques (HDI, embedded) require footprints to be built differently. This talk will show a new methodology and tools to retarget libraries for newer processes in days instead of months/years.

Who should attend: PCB Designer
Target audience: Beginner, Intermediate, Advanced

3:00 PM – 4:00 PM

C3: DESIGNING PCBS IN THE CONTEXT OF A SYSTEM

Gary Hinde, Cadence Design Systems

System design with multiple boards is a team activity for most companies. Traditional design methodologies force PCB Designers to work in silos that result in identifying system level integration issues late in the cycle or through mid-stream design reviews. There is a better way. This presentation will show a methodology that allows for managing critical high-speed system-level signals, as well as dealing with collision issues between multiple boards in an enclosure.

Who should attend: PCB Designer, System Designer
Target audience: Beginner, Intermediate, Advanced

4:00 PM – 5:00 PM

C4: MULTI-DOMAIN COLLABORATION FOR ELECTRONICS SYSTEMS DESIGN

David Wiens, Mentor

System-level product optimization requires teams across all disciplines of product development efficiently collaborate; this includes mechanical, electronics and electrical domains. This approach runs counter to the conventional "black box" design process, where teams operate largely autonomous from each other, coming together only at the end to validate the total system. Even when teams have tried to collaborate during the design process, they have been faced with tool incompatibility barriers, lack of a common review platform, and inconsistent system constraints. This session will discuss efficient methods of multi-domain collaboration, with a focus on how it enables ECAD, MCAD and cabling design teams to optimize electronics systems.

Who should attend: PCB Designer
Target audience: Intermediate

5:00 pm – 6:00 pm EXHIBIT FLOOR RECEPTION, Sponsored by Ultra Librarian

THURSDAY, SEPT. 13

8:00 am CONFERENCE COFFEE BREAK, Sponsored by Sierra Circuits

8:30 AM – 12:00 NOON

34: DESIGN OF POWER DISTRIBUTION AND DECOUPLING

Rick Hartley, RHartley Enterprises

The power distribution section of a PCB is the foundation around which all things work in the circuit. If not designed correctly, the entire circuit is at risk from noise, to say nothing of the severely increased possibilities for EMI. Low impedance in the power bus of a digital circuit across the range of harmonic frequencies is critical. To further complicate matters, analog and digital circuits often need a much different approach for power delivery to ICs.

This course will cover the role of the major components in the power distribution network (PDN), the impact of inductance on the network, the inductance of vias, capacitors and planes, optimum location and mounting configuration for capacitors, energy delivery to IC cores and to I/O drivers, decoupling PCBs with routed power rails / PCBs with widely spaced planes / PCBs with closely spaced planes, impact of IC design on power delivery, ferrites in the PDN, analog power delivery, the real impact of ultra closely spaced planes and the huge impact of board stack-up.

Who should attend: PCB Designer, Circuit/Hardware Engineer, Signal Intgrity Engineer, System Engineer
Target audience: Intermediate, Advanced

35: PART PLACEMENT CHOICES AND CONSEQUENCES

Susy Webb, Fairfield Industries

There are many ways to place parts on any board, but clearly some ways work better for physics, electrical, and mechanical purposes. If a new board works electrically but won't interface properly with the rest of its system, it may require costly and time-consuming re-design and re-testing. Designers must understand the board, electrical and system needs, as well as typical placement and routing guidelines, and the consequences of not adhering to them. When they understand the reasoning behind these things, and the effects they have on one another, designers will intuitively know how to make good decisions for their own board designs, and so avoid problems. In this presentation, we will discuss choosing effective parts, approximate order of overall placement, placement to set up routing, board and system consequences, manufacturability, and more.

Who should attend: PCB Designer

Target audience: Beginner, Intermediate, Advanced

9:00 AM – 10:00 AM

36: INTELLIGENT DFM FOR ASSEMBLY

Kevin Webb, Mentor

Design for manufacturing (DfM) applications have been around for many years and have helped companies reduce product costs, improve quality and get products to market faster. However, PCB assembly analysis has always been difficult to align internal rules to manufacturing supplier's rules. This session discusses a new approach for implementing Assembly DfM analysis. Assembly DfM applications today must be able to intelligently evaluate the component based on many characteristics, such as JEDEC type, body and pin size, pin counts, pin types, etc., to automatically categorize itself for better and consistent DfM rule assignments. Only through an automatic assignment approach can the repeatability of analysis be achieved throughout a design process. This automatic classification approach will permit a consistent set of analyses to be performed in-house, as well as at the manufacturing facility, while considering the manufacturing processes relevant for your PCB assembly. Applications achieving this objective will serve their users better and make the benefits of assembly DfM attainable by a larger audience.

Who should attend: PCB Designer, Other

Target audience: Beginner

37: PROVIDING SOLUTIONS FOR THERMAL MANAGEMENT WITHIN RF DESIGNS

James Barry, PCB Technologies

The presentation will focus on various buildup methodologies to mitigate thermal hot spots. The basics of thermal mitigation will be presented, including heavy copper, internal and external heat sinks, material, and thermal vias. "Coin Technology" and "Air Cavity" will be discussed in depth, including how these buildups can be combined within a structure. Examples of radar boards using Air Cavity will be shown, as well as more complex buildups using a combination of coin, cavity and mixed materials. This presentation will focus on the buildup of products from a cross-sectional point of view.

Who should attend: PCB Designer, SI Engineer

Target audience: Intermediate

9:00 AM – 11:00 AM

38: THE MYSTERY OF BYPASS CAPACITORS

Keven Coates, Geospace

How do you design a high-speed digital circuit with enough bypass caps in the right area to supply all the peak power demands? You can't listen to all the expert advice because it seems they can't even agree! This presentation covers power distribution network basics and shows three approaches with simulation results for each, and some real-world experience and advice on bypassing for high-speed circuits.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer

Target audience: Beginner, Intermediate, Advanced

39: ASK THE FLEXPERTS – FLEXIBLE CIRCUIT DESIGN THROUGH TEST WITH LESSONS LEARNED

Mark Finstad, Flex Circuit Technologies, and Nick Koop, TTM Technologies

This course will cover the gamut of flexible and rigid flex circuits from two of the most recognized names in the industry; Mark Finstad (co-chair of IPC-2223) and Nick Koop (co-chair of IPC-6013). Topics covered will include mechanical design/material selection, cost drivers, bending and forming concerns, testing, and issues unique to rigid flex. Throughout the presentation, the instructors will share many real life stories of flexible circuit applications gained over 30+ years in the industry. Some of these are success stories and others not so much, but all provide excellent lessons learned. The instructors also welcome and encourage questions, and enjoy "wandering off course" with lively interactive discussions on specific topics from the class.

Who should attend: PCB Designer, Hardware Engineer, Fabricator Engineer/Operator, Assembly Engineer/Operator

Target audience: Intermediate

9:00 AM – 12:00 NOON

40: DESIGNING EMBEDDED PASSIVES AND RELATED TECHNOLOGIES

Gary Ferrari, FTG Circuits

We are faced with greater design challenges than yesteryear. Circuit densities and component counts have climbed at an alarming rate. Unfortunately, board area has not increased proportionally. Circuit speeds are increasing, requiring shorter connections and more decoupling capacitors. As a result, embedded passives – those within the printed board structure – have become more attractive. They enable reduced component count, and shorter connections. This session will provide an overview of the various embedded passives technologies.

Attendees will learn how individual embedded discrete components are manufactured, basic design principles for embedded passive devices, and concepts for planar capacitance and resistance layers.

Who should attend: PCB Designer, Electrical Engineer

Target audience: Intermediate

10:00 AM – 11:00 AM

41: DFM: GETTING IT RIGHT FROM THE START

Chris Nuttall, NCAB Group

This seminar describes how to avoid costly production problems with Gerber packages.

Who should attend: PCB Designer, System Designer, Hardware Engineer, Test Engineer

Target audience: Beginner, Intermediate

42: ARRIVING AT AN OPTIMAL STACKUP FOR PRINTED CIRCUIT BOARDS USED IN SILICON VALIDATION

Vijay Nanjai Anandan, Tessolve Semiconductor

Silicon validation of integrated circuits happens at various levels, such as the wafer, package and system levels. The PCB used for the validation at these levels has different mechanical and electrical requirements. For example, the PCB designed for volume test of ICs needs to be thick enough to remain planar when exposed to high mechanical and temperature stress, whereas PCBs designed for system level or a characterization test, apart from the above, should have better signal and power integrity. Furthermore, PCB fabrication yield has to be high, which has an impact on test hardware cost and cycle time. Arriving at an optimal stackup to meet all these requirements is a crucial part in designing the PCB required for silicon validation. Various stackup technologies used to design these PCBs include plated through-hole with backdrilling; plated through-hole with flip drilling; multi-laminate stackup with blind and buried vias; and high-density interconnect (HDI) stackup with microvias and buried vias. This presentation talks about each of these stackup technologies, their advantages and limitations when it comes to fine-pitch BGA such as 0.35mm, how it suits for a particular device type, be it digital, analog, mixed, PMIC or RF, and their fabrication processes. It aims to expose ATE/system-level test engineers and PCB designers to these stackup technologies, and show how to choose one that best suits for the application and requirements.

Who should attend: PCB Designer, Hardware Engineer, Test Engineer

Target audience: Beginner, Intermediate, Advanced

11:00 AM – 12:00 NOON

43: LEVERAGING 3-D LAYOUT TO OPTIMIZE RIGID-FLEX DESIGNS

John McMillan, Mentor

2-D design is no longer sufficient for today's complicated rigid-flex designs. ECAD designers need the ability to leverage 3-D layout in order to properly optimize all elements of a rigid-flex design at the product-level, with the design in its bent state within the enclosure. 3-D layout allows designers to place, route and perform design rule checks with immediate feedback regarding any potential clearance or collision issues. To truly optimize a rigid-flex design, the 3-D environment must be more than just an interpretation of 2-D information; it must provide a realistic view of how the design will be fabricated, no matter how complicated the structure. Properly leveraging 3-D layout functionality also allows the design team to left-shift mechanical validation into the PCB layout stage, making it possible to find and fix electro-mechanical design problems early to eliminate costly, late-cycle redesigns. By considering mechanical requirements during layout and ensuring efficient communication between the electrical and mechanical flows, the rigid-flex design is correctly aligned for manufacturing, avoiding last-minute changes that cost time and money.

Who should attend: PCB Designer, Other

Target audience: Beginner

44: OVERVIEW OF SEVERAL RF STRUCTURES AND HOW THEY WORK

John Coonrod, Rogers

This presentation will give an overview, in relatively simple terms, of several PCB-based RF structures and will describe the basic operations. Initially transmission line circuits will be discussed, and these types of circuits are often used to connect different RF modules together on a PCB. Expanding on transmission line circuit concepts will be discussions for couplers and filters. Finally, PCB-based antenna designs will be discussed. Basic concepts for each structure will be given, models shown, and measured results compared to model outputs. Most structures will be limited to lower microwave frequencies, but some discussion will be given for millimeter-wave frequencies.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer, Test Engineer

Target audience: Beginner

12:00 noon – 1:00 pm LUNCH-N-LEARN, Sponsored by Polar Instruments

1:00 PM – 3:00 PM

45: ELECTROMAGNETIC FIELDS FOR NORMAL FOLKS: SHOW ME THE PICTURES AND HOLD THE EQUATIONS, PLEASE!

Daniel Beeker, NXP Semiconductor

The material presented will be focused on the physics of electromagnetic energy basic principles, presented in easy to understand language with plenty of diagrams. Attendees will discover how understanding the behavior of EM fields can help to design PCBs that will be more robust and have better EMC performance. This is not rocket science, but an easy-to-understand application of PCB geometry.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer, Test Engineer

Target audience: Beginner, Intermediate

1:00 PM – 4:30 PM

46: FLEXIBLE AND RIGID-FLEX CIRCUIT DESIGN AND ASSEMBLY PROCESS PRINCIPLES

Vern Solberg, Solberg Technical Consulting

The design guidelines for flexible circuits, although similar to rigid circuits, are somewhat unique. In essence, flex circuits furnish unlimited freedom of packaging geometry, while retaining the precision density and repeatability of printed circuits. Flex circuits typically replace the common hard-wire interface between electronic assemblies. Flexible circuits, however, have significant advantages over the hard-wired alternative because they fit only one way, eliminate wire routing errors, and save up to 75% on space and weight. Because the flex circuit conductor patterns can maintain uniform electrical characteristics, they contribute to controlling noise, crosstalk, and impedance. The flex circuits will often be designed to replace complex wire harness assemblies and connectors to further improve product reliability. During the half-day tutorial program, participants will have an opportunity to review and discuss the latest revision of IPC-2223, "Sectional Design Standard for Flexible Printed Boards," which includes base material sets, alternative fabrication methodologies and SMT-on-flex assembly processes. The workshop will also furnish practical flex circuit supplier DfM recommendations for ensuring quality, reliability and manufacturing efficiency. Discussion topics: 1. Applications and use environment • Commercial/Consumer • Industrial/Automotive • Medical/Aerospace •

FLEX AND RIGI-FLEX MANUFACTURING CHECKS

Intelligent Checking Based On Manufacturer Rules

Flex designs create challenges for most PCB tools that don't account for the nuances of Flex DFM checks. Incorporate your manufacturer's knowledge into the design process and get it right the first time.

Visit us in Booth #500

ZUKEN®

Establishing end-use criteria. 2. Designing flexible and rigid-flex circuits • Flex circuit outline planning • Circuit routing and interconnect methodologies • Fold and bend requirements • SMT land pattern reinforcement criteria. 3. Material and SMT components • IPC standards for flex and rigid-flex dielectrics • Base material and metallization technologies • Selection criteria for SMT components • SMT land pattern development. 4. Assembly processing of flex and rigid-flex circuits • Dimensioning and tolerance criteria • Palletized layout for inline assembly processing • SMT assembly process variations and methodologies • Alternative joining methods for flexible circuits.

Who should attend: PCB Designer, System Designer, Hardware Engineer, Assembly Engineer/Operator

Target audience: Beginner, Intermediate

47: BEST DFM PRACTICES FOR BOARD ENGINEERS

Susy Webb, Fairfield Industries

There is so much more to board design than placing parts and connecting the signals electrically. Those who design the board can make a *huge* impact on the ease of fabrication and assembly just by the practices they put into place as they work. Knowledge and use of standard (best) practices, whether IPC or company standards, ensures that what is sent to the manufacturer will be understood and incorporated with minimal questions, and that can be a real time and cost savings. In this class, we will talk about good practices for building footprints, how parts might be placed for manufacturability, routing practices that are helpful, trace widths and spacings that are producible, a stackup structure that can realistically get the impedance and return needed, and documentation for the manufacturer that is complete and understandable. This presentation is not about how to build a board, but rather about the practical things the board engineer can do to help make fabrication and assembly easier and therefore increase yields and lower the cost for all.

Who should attend: PCB Designer

Target audience: Beginner, Intermediate, Advanced

48: RF AND MIXED SIGNAL BOARD DESIGN

Rick Hartley, RHartley Enterprises

This session is intended to give PCB designers an understanding of the "things" RF engineers request during PCB layout. Due to sensitivity in analog circuits, the keys to full functionality (whether designing very high-frequency analog PCBs, mixing RF with digital or mixing low-frequency analog with digital) are signal integrity and noise control in the design of the PCB.

This course will cover impedance matching and balance, signal wavelength, propagation delay, critical trace length, noise, reflections, waveguides and other RF transmission lines, ¼ wavelength couplers and filters designed into board copper, RF/Analog layout techniques and strategies, plane structures, component placement, critical routing and circuit isolation, ground plane splitting (when to and when not to), mismatched loads and other discontinuities, signal splitters, tuning transmission lines, power bus decoupling for RF vs. digital circuits and PCB stackups for mixed RF and digital circuits. (Experienced RF engineers will likely not learn anything new from this course, as the material is mainly geared for PC board designers.)

Who should attend: PCB Designer

Target audience: Beginner, Intermediate

3:00 PM – 5:00 PM

49: PCB DESIGN TECHNIQUES TO IMPROVE ESD ROBUSTNESS

Daniel Beeker, NXP Semiconductor

This presentation will give some simple definitions for ESD/EOS, and describe the important differences in the energy involved and the type of damage that can result. PCB design techniques for improving system robustness will be presented. Some new research to present and some incredible design results to share using these techniques.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer, Test Engineer

Target audience: Beginner, Intermediate

MEHDI ABARHAM is a lead application engineer with a primary focus on electronics cooling applications. He has a doctorate in mechanical engineering from the University of Michigan. After graduation, he worked at Ford as a research engineer for two years before joining Ansys.

VIJAY ANANDAN is director for PCB engineering at Tessolve Semiconductor India. He has been with Tessolve for the past 10 years and has designed several complex test boards for top semiconductor companies for various ATE platforms and systems for digital, mixed, power management and RF applications. He has also worked with various PCB manufacturers in different regions and has thorough knowledge of PCB manufacturing. He has a bachelor's in electrical and electronics engineering from Anna University, Chennai, India.

CRAIG ARMENTI is a PCB marketing engineer for Mentor Graphics with a focus on the Xpedition tool suite. Over the past 25 years he has held marketing and application engineering positions with several major telecommunication and software companies. He holds a bachelor's in electrical engineering technology and an MBA in management. Prior to joining Mentor, he worked in PCB design, hardware management and application engineering at Blackberry, Foxconn, RadiSys and Nortel.

JAMES BARRY is has over 40 years in manufacturing, design, engineering and reliability experience. His background is completely in PCB technology, including assembly. He is trained in engineering, applications, materials and failure analysis. He has held various positions within the PCB industry, ranging from manufacturing, R&D, sales and marketing, engineering, and corporate and executive levels. Currently he is sales and marketing manager for PCB Technologies of Israel.

BILL CARDOSO, PH.D., started Creative Electron in his garage after 10 years with Fermilab. Creative Electron is now the largest US manufacturer of x-ray systems to the electronics industry. At Creative Electron, he leads the team of engineers that designs and manufactures x-ray systems. He received his associate's degree at 13 and went on to achieve a bachelor's, master's, and Ph.D. in electrical and computer engineering. He also has an MBA from the University of Chicago. Cardoso sits on the technical committees of SMTAI, SMTA Counterfeit Conference, SMTA LED Conference, Components for Military and Space Electronics Conference, SPIE Photonics, and the IEEE Nuclear Science Symposium. He has written two books and over 150 technical publications. He started his first company at 17 in Brazil, selling it a few years later to work for the Fermi National Accelerator Laboratory (Fermilab).

With more than 40 years of experience in electronic system design and EMC, **DANIEL BEEKER** provides applications support for NXP Automotive customers worldwide. He also supports NXP customers globally with special function development tools and instrumentation (almost all of the "LFxxx" tools on the NXP website). He also specializes in EMC and signal integrity design techniques for systems and PCBs, especially in low layer count designs. Beeker teaches field-based design techniques at NXP and industry conferences worldwide. Beeker is also involved with NXP IC package design and IC development tool teams to support improved EMC performance.

YIZHAK BOT has more than 25 years of experience in reliability and safety engineering for large projects, including electronic circuits and mechanical components for defense, aerospace, telecom, manufacturing, medical, etc. He was the program manager of many defense and commercial projects of more than $25 billion. He has written articles for leading magazines, conducts seminars and gives lectures worldwide. He is also the inventor of CARE, fiXtress and apmOptimizer technology, which help designers develop more robust products. Since 1989, he has been president and CTO of BQR, a professional testing and simulation service provider and software developing firm for the EDA market. Bot is a Certified Reliability Engineer from American Society for Quality Control (ASQC) and has a degree in electronic engineering from Tel-Aviv University.

RALF BRUENING is product manager and senior consultant at the Zuken EMC Technology Centre in Paderborn, Germany. He holds a degree in computer science, electrical engineering and economics from the University of Paderborn. He has 30 years of experience in electronics and EDA. He has longtime technical co-responsibility for Zuken's high-speed design, signal integrity, power integrity and EMI solutions. Part of his responsibility is to help customers with practical signal- and power-Integrity problems and in enhancing and optimizing their PCB design flow. He is an active member of the IBIS Open Forum and regular speaker at national and international conferences.

KEVEN COATES has been a development engineer at Geospace Technologies for five years, where he works designing low-noise seismic recording devices, industrial battery testers/chargers, and battery protection circuits. His work concentrates on embedded processors, low-noise circuits, medium-power circuits, battery safety, and battery management. He spent the previous 20 years working for Texas Instruments specializing in high-speed PCB layout/signal integrity, BGA layout, thermal issues, and PCB-friendly BGA packaging for consumer and automotive applications. He holds a bachelor's degree from Texas A&M University.

JOHN COONROD is technical marketing manager for Rogers Corp, Advanced Connectivity Solutions division. He has 30 years of experience in the PCB industry. About half of this time was spent in the flexible PCB industry on circuit design, applications, processing and materials engineering. The past 16 years have been spent supporting high-frequency circuit materials involving circuit fabrication, providing application support and conducting electrical characterization studies. He is chair for the IPC-D24C High Frequency Test Methods Task Group and holds a bachelor's in electrical engineering from Arizona State University.

PAUL COOKE has more than 30 years of experience in printed board (PWB) design and manufacturing. He has held senior positions in operations, quality, process engineering and field application engineering at some of the top North American PCB manufacturers. He has served on a number of IPC technical committees for standards development, and recently received an award for contribution to IPC-9121, "Troubleshooting for Printed Circuit Boards." He has coauthored numerous technical papers, and works with Tier 1 companies, focusing on PCB design and reliability. He has provided DfM consulting services to the industry, along with extensive training/educational presentations from PCB 101 through enhanced reliability. His current position is focused solely on working with designers in the avionics and space industry to design and develop products with extended life and long-term reliability in harsh environments.

VIJAYAKUMAR DAVID is senior manager, PCB design, in charge of library development at Tessolve Semiconductor. He has 27 years of industry experience, 17 in PCB design. He has been with Tessolve for the past 10 years in PCB design, heading QA and library development. He has bachelor's in electronics and communication engineering from NEC, M.K.University, India.

LAWRENCE DAVIS is president of Advanced Assembly.

JIM DELAP, ANSYS is an electronics product manager for Ansys, working with the company's customers and research team to provide the highest quality simulation workflow. He has a master's in electrical engineering from the University of Virginia, and has been working in the microwave and signal integrity field for over 20 years. He has designed products ranging in frequency from DC to mm-wave, and has several published trade journal and conference articles. His current interests include helping customers solve challenging electro-thermal problems.

VINCENT DI LELLO, CID+, has designed PCBs ranging from the Pebble Watch to boards that have gone into space and inside Las Vegas machines. A product engineer, he makes designers' lives easier by influencing Cadence software development.

A cofounder of Nano Dimension, **SIMON FRIED** leads its USA activities, overseeing business development, marketing, sales and product management for this revolutionary additive technology. With experience working in the US, Israel and throughout Europe, he has held senior and advisory roles in startups in the solar power, medical device and marketing sectors. Previously, he worked as consultant on projects covering sales, marketing and strategy across the automotive, financial, retail, FMCG, pharmaceutical and telecom industries. He also worked at Oxford University researching investor and consumer risk and decision-making.

GARY FERRARI is director of technical support, Firan Technology Group. He has more than 35 years' experience in electronics packaging and has held senior operations, quality and engineering positions, most recently as executive director and cofounder of the IPC Designers Council. He chaired the IPC Technical Activities Executive Committee, provided DfM consulting services, and spearheaded IPC's PWB Designer Certification Program. He was inducted into the IPC Hall of Fame in 2015.

RAY FUGITT has more than 30 years of printed circuit board experience. He spent 15 years in manufacturing, 11 with Hadco. Joining Advanced CAM Technologies as an application engineer, he supported the CAM350 product through PADS and later the Innoveda mergers. In 2002, he joined Downstream Technologies in technical marketing and later technical sales positions. He continues to support and train for both the BluePrint PCB and CAM350 products.

MARK FINSTAD is senior application engineer for Flexible Circuit Technologies. He has over 30 years of experience designing and manufacturing flexible circuits for commercial, medical, and military/avionics applications. He co-chairs the IPC-2223 Design Standard for Flexible Printed boards and coauthors the Ask the Flexperts column for *PCD&F* magazine. Finstad is also a regular columnist for several other industry publications.

XIAO MING GAO, PH.D., has been working at Intel for 20 years and has extensive experience in signal and system, I/O circuit design, signal and power integrity analysis, and high-speed platform design. He holds bachelor's, master's and Ph.D. degrees in electrical engineering. He has four patents and other pending applications.

JIM HALL is principal consultant and resident Lean Six Sigma Master Black Belt with ITM Consulting. His area of responsibility includes working with OEMs, contract assemblers, and equipment manufacturers to solve design and assembly problems, optimize facility operations, as well as teach basic and new technologies in private and public forums throughout the worldwide industry. Since joining ITM in 2000, he has helped clients in such areas as SMT implementation and assembly facility setup, manufacturing yield improvement, and process audits and improvement. He is coauthor of the SMTA Process Certification Course.

ROBERT HANSON, MSEE, has more than 40 years' experience in design, manufacturing and testing. He has bachelor's degrees in industrial engineering and business administration and a master's in electrical engineering. Hanson has been a digital design engineer at Boeing, Rockwell, Honeywell, and Loral. He teaches and consults internationally to corporations, conventions, universities, and other entities.

With 20 years of experience dealing with PCB signal integrity, **BILL HARGIN** served as product manager for Mentor Graphics' HyperLynx SI software. He currently serves as director of North American marketing for Nan Ya Plastic's PCB laminate division. More than 10,000 engineers and PCB designers worldwide have taken Hargin's workshops on high-speed PCB design, and he has spent much of the past five years focused on stackup design and PCB materials selection.

RICK HARTLEY is principal of RHartley Enterprises, resolving noise, signal integrity and EMI problems. Hartley has a degree in engineering from Ohio Technical Institute and 49 years of experience with companies such as L3 Avionics and BF Goodrich. He is a past member of the Editorial Review Board of *Printed Circuit Design* magazine and has written numerous technical papers and articles on methods to control noise, EMI and signal integrity.

GARY HINDE has been involved in PCB design since his apprenticeship started in 1975. While at Schlumberger Instruments he was involved in design and layout for a diverse range of products such as laboratory instrumentation (digital voltmeters, frequency response analysers, remote data logging and industrial transducers), aircraft flight control simulators, ground warfare simulation systems and security access systems. In 1991, he joined Cadence Design Systems as an application engineer, providing support for internal teams and customers. He has worked with a number of companies worldwide and is currently helping to develop electronic hardware system solutions for multi-fabric designs.

TAYLOR HOGAN has been working in electronic design automation for over 30 years. His research interests include genetic optimization, machine learning, and functional programming. He holds a bachelor's in computer science and a master's in electrical engineering. He holds several patents in the area of constraint-driven optimization of multi-substrate designs.

JEREMY HONG comes from a very hands-on and pragmatic hardware design background. He has dealt with complex mixed signal circuit board design and layout (40+ layer PCBs). Now he is a hardware reverse-engineer for Caesar Creek Software, but still does design work through a company he started in high school, Hong's Electronics. He lives in Dayton, Ohio.

DAVE HOOVER is a senior field application engineer at TTM Technologies, where he supports some of its top telecom customers. He has 40+ years' experience in PCB fabrication, and has been involved with the development of HDI, microvias and other leading high-speed technologies. His career includes PCB fabricators such as Hadco/Sanmina, Data Circuits, Litronic Industries, and Multek.

BEN JORDAN is a computer systems and PCB engineer with 25+ years of experience in PCB, embedded systems, and FPGA design. He started out at Altium as a senior applications engineer in 2004, traversing roles since as field applications engineer, tech support manager (USA), product marketing, and CircuitMaker evangelist before arriving at his current station as a senior member of Altium's product marketing team. He is an avid tinkerer and is passionate about the creation of electronic devices of all kinds. He holds a bachelor's of engineering (CompSysEng) with First Class Honors from the University of Southern Queensland.

SCOTT KOHNO is president of Royal Flex Circuits.

NICK KOOP is a senior field application engineer for TTM Technologies and has over 30 years of design, manufacturing and management experience in the flexible circuit industry. He developed and applied advanced PCB technologies to support a wide range medical, military, and global security applications. He is vice chairman of the IPC Flexible Circuits Committee, co-chair for the IPC-6013 Qualification and Performance Specification for Flexible Printed Boards Subcommittee, and coauthors the *Ask the Flexperts* column for *PCD&F* magazine.

RICHARD LEGASPINO is currently a senior PCB engineer at Analog Devices Inc. He graduated in 1994 from Cebu Institute of Technology, Cebu City with a bachelor's degree in electronic and communications engineering. He has three years' experience in hardware engineering at Acer Inc. Taiwan and five years' experience as test engineer at Teradyne Philippines LTD, Cebu. He joined Analog Devices Philippines on May, 16 2006 as test manufacturing engineer. He currently leads the simulation team at Analog Devices Philippines that supports signal and power integrity simulation requests across ADI sites.

MARK LAING has over 25 years' experience in PCB manufacturing, with particular strengths in test and inspection methodologies with three test companies: Marconi instruments, GenRad and Teradyne. He then moved into software solutions for Router Solutions. Since 2010, he has worked for Mentor's Valor division as a product marketing manager and business development manager. He has a bachelor's in electrical and electronic engineering from Loughborough University (UK). He has been granted two patents, one in the UK and one in the US, and recently filed a third one.

DENNIS NAGLE has been involved with high-speed PCB design for over 29 years. At Cadence Design Systems, he is a product engineering architect, responsible for driving the technical roadmap for the Allegro Sigrity SI product line and the High-Speed Constraint Driven Flow. Prior to that, he held technical marketing and applications roles in various capacities for Cadence's PCB design products. Before joining Cadence, he worked at Data General. He has a bachelor's in electrical engineering from Worcester Polytechnic Institute.

CHRIS NUTTAL joined NCAB in 2009 as UK operations director. In 2010, he became NCAB's quality and technical manager for the worldwide group. Prior to NCAB, he was quality manager and later supply chain director of the UK's largest independent PCB operation, with partners in China, Taiwan, Korea, Malaysia, India and UK. His responsibilities included purchasing, sourcing, logistics and warehousing. Previous to that, he was a quality engineer for tier 1/ tier 2 automotive customers at a PCB manufacturer in Scotland. He has a master's in quality management.

SEAN PRIDDY has a 20+ year diverse background in embedded electronics product development across consumer electronics, industrial, and DoD markets. As a senior design engineer, he has developed many wireless communications products spanning cellular, Bluetooth, 802.15.4, and other proprietary networking technologies. As a systems architect, he has created a software reconfigurable wireless sensor gateway and cloud-based management platform for IoT solutions. Now as the business development director for Creation Technologies, he provides guidance to customers developing novel IoT hardware solutions.

STEVEN G. PYTEL JR. is principal electronics product manager at Ansys. He has a Ph.D. in signal integrity from the University of South Carolina. He previously worked at Intel as a signal integrity and hardware design engineer where he helped design blade, telecom, and enterprise servers. He has over 50 publications, with an invited book chapter on signal integrity simulation within Maxwell's Equations: *The Foundations of Signal Integrity,* authored by Paul Huray. His current research interests focus on electro-thermal design challenges for digital and high power electronic devices.

NAVEID M. RAHMATULLAH has been working for Intel for 18 years, managing multiple hardware platform teams. He has been leading the board design process and methodologies within Intel to maximize efficiency and deliver high quality platforms for client, server, and IoT products and IP validations. He holds a bachelor's in electrical engineering, and has authored several technical papers.

WALDEN RHINES is president and chief executive of Mentor, a Siemens business. He was previously CEO of Mentor Graphics for 23 years and chairman for 17 years. Prior to joining Mentor, Rhines was executive vice president of Texas Instruments' Semiconductor Group. During his 21 years at TI, he was president of the Data Systems Group and held numerous other semiconductor executive management positions. He has a bachelor's in engineering from the University of Michigan, a master's and Ph.D. in materials science and engineering from Stanford, and an MBA from Southern Methodist University.

HEMANT SHAH has been with Cadence Design Systems, SPB division since 2000, most recently as product management group director – Allegro PCB & FPGA products. Previously, he was engineering director for advanced development at Xynetix Design Systems, where he also held a product marketing director role. He holds a bachelor's in electrical engineering and a master's in computer science.

MILAN SHAH is president of Royal Circuit Solutions, which he purchased in 2008. He began his technology career at Apple Computer. From there he moved to Sony as director of multimedia technologies and introduced leading-edge technologies to the North American markets. He has a bachelor's in computer information systems and business communications from Western Michigan University, and also an MBA.

VERN SOLBERG holds several patents for IC packaging innovations, including the folded-flex 3D package technology and is the author of *Design Guidelines for Surface Mount and Fine-Pitch Technology*. He is a speaker and instructor supporting several industry organization technical programs, including IPC and SMTA. He is currently an IPC Ambassador Council member, chairman of the task group that developed the IPC-7094, "Design and Assembly Process Implementation for Flip Chip and Die Size Components," and a certified IPC trainer for IPC-A-600, "Acceptability of Printed Boards."

KEN TAYLOR never designed a board in his life, nor did he build one, and he's too old to begin now. He began his career teaching high school and college, then returned to college, eventually becoming a physicist with a global chemical corporation before moving to exciting stuff like rocket propulsion and submarine acoustics. Next came 25 years of international sales and marketing with Tektronix before moving to Polar Instruments in 2001 to manage Polar's US operations. Notwithstanding, he understands the physics of PCB transmission line impedance and has worked with engineers, board designers and board manufacturers during his entire Polar career. His teaching experience helps him convey concepts in the least threatening way.

MARCUS MIGUEL V. VICEDO, CID, is a PCB design engineer at Analog Devices, where he currently supports a variety of PCB designs from high-speed applications to RF. He has a bachelor's in electronics engineering.

MARCO M. VILLAHERMOSA, CID, is a senior PCB design engineer at Analog Devices. He has a bachelor's in electronics and communications engineering from Ateneo de Naga University and a master's in ECE from Mapua Institute of Technology. Prior to joining ADI, he worked as PCB design engineer in Rohm LSI Design Philippines and line engineer at Ibiden Philippines.

KEVIN WEBB is a technical marketing engineer for the Valor Division of Mentor, with in-depth knowledge of Valor NPI, automation and PCB manufacturing processes.

SUSY WEBB, CID, is a senior PCB designer with 37 years of experience. Her career includes experience in coastal and oceanographic oil exploration and monitoring equipment, point-to-point microwave network systems, and CPCI and ATX computer motherboards. She is a regular speaker at PCB, IPC and international design conferences and consults for individual companies and Designers Council chapters. Her presentations discuss practical implementation of complex engineering concepts into board layout, and methods to improve the overall design and flow of printed circuit boards. She has set up company standards, documentation, procedures, and library conventions for several companies. She a former writer/columnist for *PCD&F* magazine, and a judge for Mentor's Technology Leadership Awards. Webb is also an active member of the IPC Designers Council Executive Board and education committees.

DAVID WIENS joined Mentor in 1999 through the acquisition of VeriBest. Over the past 30+ years, he has held various engineering, marketing and management positions within the EDA industry. His focus areas have included advanced packaging, high-speed design, routing technology and integrated systems design. He holds a bachelor's in computer science from the University of Kansas.

ALBERT YANEZ is executive vice president and president of the Americas of AsteelFlash Group. He served as general manager and executive vice president of WW operations at Serious Energy, where he was instrumental in building a leading company in green building materials. He has over 25 years of international business, operations, equipment engineering and manufacturing engineering experience. He has held several positions such as corporate director of program management for Monierlifetile (LaFarge). He also served as general manager of Southwall Technologies, and was on the core management team of Manufacturers Services Inc., where he streamlined operations for Hewlett Packard's laser jet and plotter manufacturing divisions. He also held senior management positions at Western Digital. He was part of the team that founded Trimedia, which became Hitachi Metals Trimedia.

PHIL ZARROW founded ITM Consulting in 1993, and has been involved with PCB fabrication and assembly for more than 35 years. His expertise includes the manufacture of equipment for PCB fabrication and assembly of through-hole and surface mount technologies. In addition to his background in automated assembly and cleaning, Zarrow is recognized for his expertise in SMT soldering and design and implementation of SMT placement equipment and reflow soldering systems. Having held key technical and management positions with Vitronics, Excellon-Micronetics and Universal Instruments, he has extensive hands-on experience with setup and troubleshooting through-hole and SMT processes throughout the world. During his tenure as director of technology development for GSS/Array Technology, he was responsible for specifying and setting up medium- and high-speed assembly lines, as well as investigating and implementing emerging and leading-edge technologies, equipment and processes. He is coauthor of the SMTA Process Certification Course.

THANK YOU

TO OUR SPONSORS

EMA Design Automation®

Mentor®
A Siemens Business

Polar

SIERRA CIRCUITS
QUALITY LEADER
SINCE 1986

STREAMLINE CIRCUITS
PCB EXPERTS

ZUKEN®

Ultra Librarian™

JULY 2018 • VOL. 35 • NO. 7

内容

PRINTED CIRCUIT DESIGN & FAB CIRCUITS ASSEMBLY

FIRST PERSON

MONEY MATTERS

TECH TALK

FEATURES

IN THE DIGITAL EDITION

DEPARTMENTS

POSTMASTER: Send address changes to PRINTED CIRCUIT DESIGN & FAB / CIRCUITS ASSEMBLY, PO Box 470 Canton, GA 30169

ENEPIG "2.0"

ENEPIG has *(at last!)* reached its ***ultimate*** performance potential!

- Uniquely flexible and stable electrolytes, with Talon electroless/alloyed palladium phos
- Lowest make-up and operating costs
- Pure palladium formulation available
- Reduction-assisted TWX-40 plates up to 8 µin of gold, with no nickel corrosion or deposit porosity

North America's Leading Experts in Final Finishes, including high frequency, harsh environment, and other applications, also Via Fills, Acid and Electroless Coppers, and Auruna Gold Electrolytes.

UYEMURA

Corporate Headquarters: 3990 Concours, #425 Ontario, CA 91764 • Ph: (909) 466-5635
Tech Center: 240 Town Line Road • Southington, CT 06489 • Ph: (860) 793-4011
Sales and Product Information: sales@uyemura.com • **uyemura.com**

PRINTED CIRCUIT DESIGN & FAB / CIRCUITS ASSEMBLY

pcdandf.com
circuitsassembly.com

EDITORIAL

EDITOR IN CHIEF: Mike Buetow, 617-327-4702, mbuetow@upmediagroup.com
SENIOR EDITOR: Chelsey Drysdale, 949-295-3109, cdrysdale@upmediagroup.com

DESIGN TECHNICAL EDITOR: Pete Waddell
EDITORIAL OFFICE: P.O. Box 470, Canton, GA 30169, 888-248-7020

PCD&F CONTRIBUTING EDITORS:
Akber Roy, Duane Benson, Peter Bigelow, Martin Cotton, Mark Finstad, Nick Koop

CIRCUITS ASSEMBLY CONTRIBUTING EDITORS AND ADVISORS:
Clive Ashmore, David Bernard, Robert Boguski, John D. Borneman, Joseph Fama, Susan Mucha, Chrys Shea, Jan Vardaman, Ranko Vujosevic

PRODUCTION

ART DIRECTOR AND PRODUCTION MANAGER:
Atomic Graphics, production@upmediagroup.com

SALES

SALES DIRECTOR:
Frances Stewart, 678-817-1286, fstewart@upmediagroup.com
SALES ASSISTANT:
Rebecca Handler, 770-617-7864, rhandler@upmediagroup.com
EXHIBIT SALES:
Frances Stewart, 678-817-1286, fstewart@upmediagroup.com
PRINT/ELECTRONIC REPRINTS: cdrysdale@upmediagroup.com

SUBSCRIPTIONS

Rebecca Handler, 770-617-7864, rhandler@upmediagroup.com

UP MEDIA GROUP, INC.

PRESIDENT: Pete Waddell
VICE PRESIDENT, SALES AND MARKETING:
Frances Stewart, fstewart@upmediagroup.com
VICE PRESIDENT, EDITORIAL AND PRODUCTION:
Mike Buetow, mbuetow@upmediagroup.com
DIRECTOR OF GROUP SHOWS
Alyson Corey, acorey@upmediagroup.com

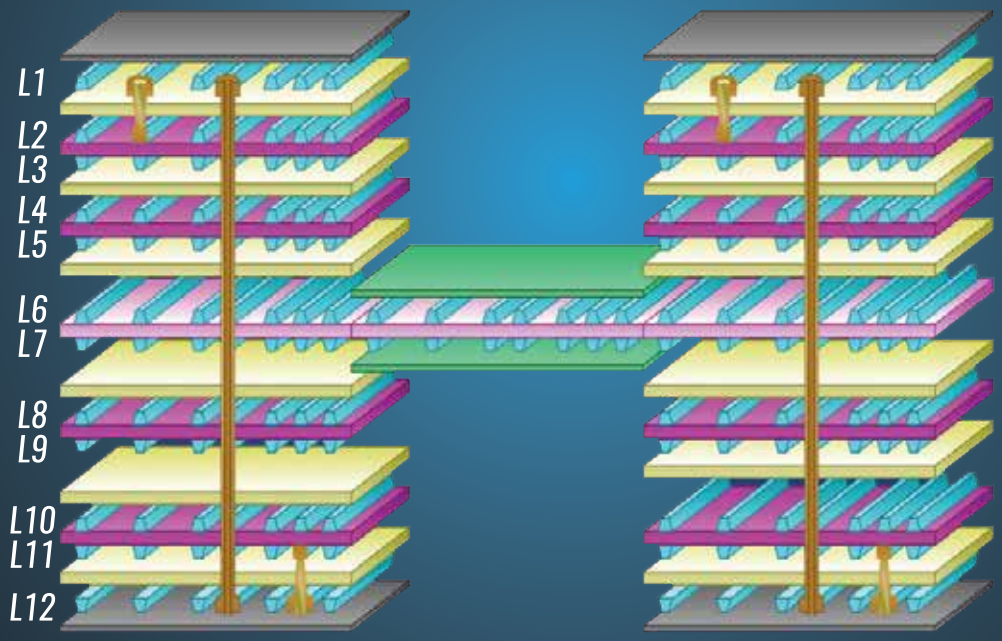
PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is distributed without charge to qualified subscribers. For others, annual Subscription Rates in U.S. funds are: $80 (U.S. and Canada), $145 (all other countries). Single copy price is $8.50. All subscription and single copy orders or inquiries should be directed to PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY, PO Box 470 Canton, GA 30169 rhandler@upmediagroup.com. Photocopies and issues on Micro-film/Microfiche (16mm, 33mm or 105mm) are available from University Microfilms International, 300 N. Zeeb Rd., Ann Arbor, MI 48106, Telephone 313-761-4600.

PRINTED CIRCUIT DESIGN & FAB/CIRCUITS ASSEMBLY is published monthly by UP Media Group Inc., PO Box 470 Canton, GA 30169. ISSN 1939-5442. GST 124513185/ Agreement #1419617.
Periodicals postage paid at Canton/Ball Ground, GA, and additional mailing offices.

Postmaster: Send address changes to Printed Circuit Design and Fab/Circuits Assembly, PO Box 470 Canton, GA 30169.

Multilayer PCB Stackup

12 Layer Flex Rigid, 0.030" Thick Rigid, 0.008" Thick Flex
Blind Via L1-L2 & L11-L12, 0.003" Hole, Resin Filled,
0.002"/0.002" Trace/Space, Controlled Impedance



Manufactured on August 2016

When you're in a rush call RUSH PCB

Affordable Pricing ⋆ Satisfaction Guarantee ⋆ Fast Response ⋆ Free Quote ⋆ Fast Shipping
HDI Boards ⋆ Stacked Micro Vias ⋆ 2 mil line & Space ⋆ Flex & Rigid Flex

Located in the Silicon Valley
PCB up to 12 Layers in 3 days
PCB Assembly Same Day Turn
Full Turnkey Service

Certified: ISO9001/ITAR/UL

www.rushpcb.com | Sales@rushpcb.com | 1 408 496 6013
Rush PCB Inc, 2149-20 O'Toole Ave, San Jose, CA 95131, U.S.A

MIKE BUETOW
EDITOR-IN-CHIEF

The Researcher's Playground

THE exploding maker market has brought thousands of new designers to the field. Many are learning printed circuit techniques on their own, through videos or books or other tutorials, rather than via the traditional mentor/trainer relationships. When you are a one-person operation, trial-and-error can be a painful process. Months of work can go down the drain in one fell swoop.

Amid all the maker noise, an entirely new generation of designers is being overlooked. These are the folks at colleges and universities who, like hobbyists, are learning board design as a means to develop new products and realize their ideas. But the scale can be several times greater; whereas a maker might design and re-spin a board a half-dozen times in a year, student teams might be producing three times that rate.

While their work may be under the radar, it can be highly significant. At the University of Sherbrooke in Quebec, for instance, graduate students in the Medical Equipment Research Group (GRAMS) are designing boards for imaging animal and human brains. Working with some of the top medical programs in the world, including Massachusetts General Hospital, engineers like Jonathan Bouchard are developing state-of-the-art brain scanners with exquisite spatial resolution.

Bouchard is a doctoral student in electrical engineering. He has been designing boards for nearly a decade, when he teamed up with other undergraduates to design unmanned aerial vehicles (UAVs). Necessity being the mother of invention, Bouchard recalls the lack of off-the-shelf parts for building drones led the team to use custom PCBs. "I first learned with teachers, then by myself. I worked a lot on this. I started to get interested in PCB and system design."

The team entered drone competitions, and board failures occasionally meant aircraft crashes. For Bouchard, it was part of the learning process. "You get experience from every single one you do," he notes. The board costs of failures can be self-limiting for many. Fortunately for Bouchard, he had a sponsor who was a fabricator in Montreal. "I designed 20 to 40 boards in a year, and they were producing them for free. Not everyone has the same chance to get experience in the field."

As part of his development as a designer, he reached out to a professor at Sherbrooke. He later joined that professor's group in graduate school. There, he is part of a team that uses professional CAD like Mentor Pads or Altium Designer. That team has two permanent technicians who do a lot of designs for a variety of projects, plus two interns and three others who work on PCB designs. Bouchard estimates there are maybe 300 to 400 workers at the research institute in Quebec, and many are designing electronics from chip-scale to PCB scale and building robots with them. Internally, they also design ASICs and make all the test boards themselves. The most complex board he produced was 16 layers, with microvias, buried vias and HDI. The group did a 32-layer-board. The lab goes far beyond the stereotypical mad scientist in the garage.

Like professional design groups, GRAMS has put in processes to reduce failures. "We have seen a lot of things that could have potentially failed," explains Bouchard, "but we can't afford to make more revisions, so we really have to be careful. We have a team that reviews all our designs and footprints."

With all the talk of the graying of the PCB design industry, especially in North America, I was interested getting Bouchard's take. "Do your colleagues ever discuss the relative age of PCB designers today?" I asked him. The response: "I wasn't really aware of that, but I kind of get (why), because it requires some experience. You have to start at the bottom and learn it."

I was surprised to hear graduate-level engineers were so entrenched in board design. But don't expect them to start seeking jobs with Intel and Apple. Bouchard says that when he completes his dissertation, he wants to stay on the academic side. "I like playing inside the research field. I really find it stimulating to build things that don't exist yet. Brand new competences give you opportunities to go further."

Just when you think you know the industry, you find new pockets doing great work, (mostly) sight unseen.

mbuetow@upmediagroup.com
@mikebuetow

P.S. Those interested in the future of the PCB profession, and the recruiting and management techniques needed to attract and keep millennials, are encouraged to attend Phil Marcoux's panel on The Future of PCB Engineers at PCB West in September. (pcbwest.com)

We Navigate EMS Supply Chain Challenges Every Day

At SigmaTron International, we recognize that our electronics contract manufacturing customers want superior quality product where they need it, when they need it. While production is part of that equation, visibility into the supply chain and the ability to react to changing availability has become an even more critical element. Our knowledgeable supply chain team, proprietary real-time systems and logistics partners help ensure that customer requirements are consistently met.

SigmaTron's advantages include:

- Agile PLM-driven project launch support
- Access to a global network of facilities in the U.S., Mexico, China and Vietnam
- 24/7 visibility into project status around the globe via our proprietary SCORE™ system
- A supply chain management strategy that supports material integrity while achieving competitive cost
- Robust systems for serialization, traceability and device history recordkeeping
- An experienced team capable of supporting your project's changing needs over time.

We've built our business around mid-to-high volume accounts who want Tier One caliber solutions, but truly customized service and responsiveness. All of our facilities are all registered to ISO 9001 and those building mission critical products are also registered to ISO 13485, ISO/TS16949 and/or AS9100C. You'll have access to global manufacturing options that support both nearshore and offshore strategies plus a trusted partner who truly values your business.

Call us today at **510-477-5004** or visit us on the web at: **www.sigmatronintl.com/ca** and download our new white paper: ***Supply Chain Disruption: How Well is Your Contract Manufacturer Prepared?***

Let us show you how our scalable options can help your company thrive in a changing world.

ONE SOURCE. GLOBAL OPTIONS.®

SIGMATRON INTERNATIONAL

PCD&F People

NCAB Group CEO **Hans Stahl** joins PCB Chat to offer background on the company's IPO and outline plans for acquisition targets and future expansion. (upmg.podbean.com)

Tech-Etch named **Richard Cammarano** president and CEO.

Siemens PLM Software promoted **Craig Armenti** to director of Electronics Solutions. He has been with Mentor since October 2016, and prior to that held executive and engineering roles with Zuken, BlackBerry and Motorola.

Charles Pfeil of Altium announced he retired on May 31. He spent 23 years as a PCB designer and another 26 in software development with VeriBest, Mentor and Altium.

TTM Technologies promoted **Nick Koop** to director, flex technology. He has been with TTM since 2013, and prior to that spent eight years at Minco.

PCD&F Briefs

Altix named **Artnet PRO** representative in North America and the Far East.

China has implemented another decree on emissions, with the provinces of Hebei, Shandong, Henan, and Shanxi releasing statements that they would employ stringent administration measures.

Taiwanese legislators are reviewing amendments to the national Toxic Chemical Substances Control Act following the deadly fire at **Chin Poon**.

Elite Material has begun expansion on a plant in Hubei Province set to come online by next August.

Fineline-Global named as sales representative **KTT Engineering and Manufacturing** in California and appointed **Hughes Cain and Associates** in the Southwest US and Mexico.

Two Chinese environmental organizations said they found that copper-laced acidic wastewater had been discharged from **Ichia Technologies** in Suzhou.

IPC awarded **Ventec** a second IPC-4101 Qualified Products Listing (QPL).

The deadline for comments to an amendment focusing on automotive requirements to IPC-6012, the industry standard for rigid PCBs, was Jun. 4, the chairman of the authoring task group said.

PCB West to Feature 15 Free Conference Presentations

ATLANTA, GA – PCB West announced this year's conference will feature two full tracks worth of free presentations on Sept. 12, with topics ranging from signal integrity to 3-D printing and common design errors.

A third track, the new CAD Tool Corner, will cover the design gamut, from component libraries to simulation and collaboration within the ECAD-MCAD software flow.

Rick Hartley, the most popular speaker in the history of PCB West, will kick off "Free Wednesday" with a two-hour talk on routing and termination for control of signal integrity. Other speakers are from Intel, AsteelFlash, TTM Technologies, Nano Dimension, Creation Technologies and other leading companies.

In all, the three tracks will include 15 free presentations. Among others, topics include:

- Prototype design
- HDI standards and design rules
- AI and machine learning
- 3D printed electronics
- Preventing the 10+ 21 most common design errors
- Data transfer within the Industry 4.0 environment
- PCB interposer design
- Optimizing hardware for IoT solutions

The CAD Tool Corner and Free Wednesday tracks take place Sept. 12, the same day as the sold-out exhibition. The trade show features more than 100 companies showing the latest in printed circuit design software, fabrication and assembly services.

"We are excited to offer more than two full days' worth of free sessions, with loads of valuable content for designers and all types of engineers," said UPMG vice president and conference chair Mike Buetow. "And where else could you come hear great instructors like Rick Hartley for free?"

To register for the exhibition, which includes access to these free sessions, visit pcbwest.com. – *MB*

NCAB Group Goes Public on Swedish Exchange

STOCKHOLM – PCB broker firm NCAB Group went public on June 5 with an offering on the Nasdaq Stockholm Exchange. The firm will use the funds to support its growth and operational strategy, among other things.

About 12.5 million shares were issued, and the company raised more than SEK 940 million ($108 million) in the sale.

"Being listed is a logical step for us now that we have reached sufficient size, profitability and maturity. I am proud of the team at NCAB, who has developed the company to a leading business with global reach. The listing is a quality mark, which will enable us to attract more and larger customers and make additional acquisitions," said Hans Stahl, CEO, NCAB.

"It has been great to be part of the growth and development of NCAB since 2007 and to work with the management team and many highly competent employees," said Christian Salamon, chairman, NCAB Group. "There is a culture of technical specialization, teamwork and dedication to customers. I am particularly proud of the high ratings NCAB has in the eyes of its customers, as well as from its employees. I also believe the work NCAB is doing in sustainability is an important part of its success."

NCAB is one of the largest PCB distributors worldwide, with operations in 15 countries and sales in 45 countries. In 2017 NCAB totaled revenue of $162 million (SEK 1.4 billion) and adjusted EBITA of $13 million. It had 1,650 customers in 2017, for which it produced 113 million PCBs. (Listen to Hans Stahl's interview on the PCB Chat podcast at upmg.podbean.com). – *MB*

YOUR EXPERT SERVICES PROVIDER

ONLINE PCBS

SPECIAL OFFER

15% OFF WHEN SELF ORDERING
YOUR PCBs AT ICAPE SHOP
ONLINE SIMPLE PCB QUOTES
PROTOTYPES & SMALL VOLUMES

LIMITED TIME ONLY
JULY OFFER
(from 07.01 till 07.31)

DISCOUNT CODE
4thJulyoffer

15% OFF

www.icapeshop.com

+ 1 765 431 1271 info@icape-group.com www.icape-group.com

Origalys Electrochem named **Technic** to distribute its electrochemistry instruments in the US.

Printed Circuits added an **Orbotech** Paragon LDI and a Fusion 22 AOI.

Prototron Circuits' PCB fabrication facility in Tucson, AZ, has achieved ISO 9001-2015 certification.

PCB West announced registration is open for the 2018 technical conference and exhibition at pcbwest.com.

Rogers filed a lawsuit in Germany against Korea-based **KCC** alleging infringement on a Rogers patent for direct bonded copper substrate master cards.

A new Pentagon report warns the supply chain for high-end electronics and rare materials is increasingly at risk, likely putting radar and electronic warfare capabilities in danger as the **US Department of Defense** relies more on these items.

CA People

Circuitronics appointed **Tim Harmon** vice president of operations. He has an MBA from Drexel and 18 years' experience in manufacturing engineering.

Horizon Sales promoted **Ken DeVries** to representative covering Eastern Michigan, Northern Ohio, Northwestern PA, and North Indiana US. He joined Horizon in 2018 as regional sales manager.

Koh Young America named **Jermaine Ducree** field engineer.

OEM Group named **Roberta Pino** senior buyer.

Ryder Industries appointed **Kingslea Chan** vice president of sales and marketing. He has 18 years' experience in operations, program management and business development with Flex, Season Group, and Hayco Group.

Sono-Tek appointed **Brian Booth** director of electronics & advanced energy. He joined Sono-Tek in 2007 as field service engineer and became regional sales manager in 2010.

Viscom named **Jesper Lykke** CEO and **Ed Moll** president of its US subsidiary. **Carsten Salewski** has been promoted to the executive board in charge of sales, marketing and international business. **Peter Krippner** will assume executive responsibility for operations.

Pending US Tariffs to Affect Host of PCB Equipment, Components

WASHINGTON – President Trump's decision to impose steep tariffs on Chinese imports will affect a number of products used in printed circuit board manufacturing and assembly.

The affected parts include common components such as connectors and passives, laser drills, dispensing machines, placement machines and reflow ovens, among other equipment.

The Trump administration this week announced a 25% tax on imports of more than 800 products made in China. The tariffs take effect Jul 6.

The tariffs come after a so-called Section 301 investigation by the office of the US Trade Representative, which determined China's policy of forcing foreign companies into partnerships with domestic firms had led to involuntary and illegal transfers of US corporate IP.

Among the products targeted for duty increases:

- Mechanical appliances for projecting, dispersing or spraying liquids or powders, used for making printed circuits or printed circuit assemblies (8424.89.10)
- Machine tools operated by laser, of a kind used solely or principally for manufacture of printed circuits (8456.11.70)
- Machine tools operated by light or photon beam processes, of a kind used solely or principally for the manufacture of printed circuits (8456.12.70)
- Parts & accessories for machines of heading 8456 to 8461 used to make printed circuits or PCAs, parts of heading 8517 or computers (8466.93.96)
- Parts and accessories of the ADP machines of heading 8471, not incorporating a CRT, parts and accessories of printed circuit assemblies (8473.30.20)
- Printed circuit assemblies for automatic teller machines of subheading (8472.90.10)
- Printed circuit assemblies of the goods of subheading 8504.40 or 8504.50 for telecommunication apparatus (8504.90.65)
- Printed circuit assemblies of electrical transformers, static converters and inductors (8504.90.75)
- Industrial furnaces and ovens for making printed circuits or printed circuit assemblies
- Printed circuit assemblies for television cameras (8529.90.09)
- Printed circuit assemblies which are subassemblies of radar, radio nav. aid or remote control apparatus, of 2 or more parts joined together (8529.90.19)
- Tantalum fixed capacitors (8532.21.00)
- Electrical fixed resistors, other than composition or film type carbon resistors, for a power handling capacity not exceeding 20W (8533.21.00)
- Electrical fixed resistors, other than composition or film type carbon resistors, for a power handling capacity exceeding 20W (8533.29.00)
- Connectors: coaxial, cylindrical multicontact, rack and panel, printed circuit, ribbon or flat cable, for a voltage not exceeding 1,000V (8536.69.40)

China is expected to respond in kind to the US tariffs.

IPC issued a note to its members reporting that discussions between US and Chinese trade officials are ongoing, and that the President could delay the duty increases up to 180 days. – MB

Power Design Services, Green Circuits Merge

SAN JOSE – Power Design Services (PDS) and Green Circuits announced a merger agreement, effective May 21. Financial and other terms were not disclosed.

Both EMS companies are based in San Jose and provide full-turnkey services, with Power Design Services focusing on prototypes and lower volumes and Green Circuits stretching into medium-volume assembly.

"This partnership presents an opportunity to extend the missions of both organizations to provide high-quality design, prototyping and full-scale production services to our customers," said Ted Park, president of Green Circuits. "With many

YXLON

A company of the Comet Group

Why compromise?

Choose a custom-built EVO solution for premium inspection

Join the Evolution: www.yxlon.com/evolution

Cheetah **EVO** PLUS | Cougar **EVO** SMT | Cheetah **EVO** SEMI | Cougar **EVO** PLUS | Cheetah **EVO** SMT | Cougar **EVO** SEMI

CA Briefs

Bowman appointed **SciMed** exclusive distributor for its XRF plating thickness measurement systems in the UK.

China has launched a probe into **Samsung, SK Hynix** and **Micron Technology**, the three semiconductor makers that control the market for DRAM memory chips.

Formosa Advanced Technologies (FATC) will expand production capacity for DDR4 burn-in and testing, according to the company.

Foxconn employees building products for **Amazon** at a factory in China were required to work at least 100 hours of overtime per month, well above the Chinese cap of 36 hours per month, a labor rights group says. Foxconn is denying the charges.

Foxconn said it remains committed to its $10 billion Wisconsin manufacturing facility, rejecting a report that it's considering reducing its initial investment by making display screens for smaller electronics, like phones.

Huawei is starting PCB assembly with **Flex** in Sriperumbudur, India.

IAC Electronic Manufacturing Services will relocate its plant in Newport, UK.

IPC said it welcomes the US Senate's version of the National Defense Authorization Act (NDAA), which could shore up the electronics manufacturing supply chain.

KUK Electronic could open an electronics assembly plant in Sri Lanka.

Naprotek installed a **Nordson Dage** Quadra 5 x-ray inspection system.

New-Heart Technology has purchased **Ucamco's** Integr8tor CAM for its plant in Taiwan.

Panasonic System Solutions named **Assembly Products** value-added sales representative in the New England US.

ProSMT installed an **ITW EAE** MPM printer at its manufacturer's rep site in Turkey.

Purdue researchers have discovered a new 2-D material, derived from the rare element tellurium, to make transistors that carry a current better throughout a computer chip.

Rutgers physicists have demonstrated a way to conduct electricity between transistors without energy loss, opening the door to low-power electronics.

Suzhou Victory Precision Manufacture has purchased the entire capital stock of **JOT Automation**.

TT Electronics has acquired **Precision Inc.**

Varitron has earned ISO 13485:2016 certification.

of our customers on aggressive development schedules, having all these capabilities within one organization reduces time to market, enabling a faster production ramp and reducing overall costs for our customers."

"Constantly striving for perfection and working toward aligned goals with like-minded individuals, complimentary skills and a customer-first attitude, this partnership will provide customers with the assurance that their projects will be completed to their specific design requirements, on-time and on-budget," said Joe O'Neil, president of Power Design Services. – *CD*

Mycronic Acquires MRSI for $41M in Cash

TABY, SWEDEN – Mycronic continued its acquisition push in June, purchasing 100% of MRSI Systems for $40.7 million in cash.

The acquisition was effective Jun. 1 and is expected to be accretive to underlying EBIT in 2018. Under certain performance targets, an earn-out of up to $20.2 million will be paid in 2020, which could bring the total purchase price to $60.9 million in today's currency. Mycronic is financing the acquisition through cash on hand and bank financing.

North Billerica, MA-based MRSI manufactures die bonders for optoelectronics and microelectronics assembly. Its largest customer segment is optical communications, and other market segments include defense and aerospace, life science and advanced manufacturing. It had net sales in 2017 of $31 million.

"MRSI is a perfect strategic match with Mycronic's goal of adding leading businesses in the area of high-precision and high-flexibility equipment manufacturers for electronics assembly. This acquisition is a further step in executing our strategy of growing with profitability in adjacent market segments," said Lena Olving, CEO and president, Mycronic.

"This acquisition will enable Mycronic to continue introducing exciting new products that address growing customer needs for increased precision, flexibility and speed. MRSI fits well with our growth strategy and is supported by several strong long-term trends in electronics assembly," added Thomas Stetter, senior VP and general manager, Assembly Solutions, Mycronic.

MRSI will be a part of the Assembly Automation division within the Assembly Solutions business area. The Assembly Automation division also comprises AEi (Automation Engineering Inc.), which is one of Mycronic's recent acquisitions. MRSI will, together with AEi, broaden Mycronic's product offering further, targeting additional electronics industry segments and strengthening the future offering to the automotive industry, for example in lidar and ADAS.

"From our customers' perspective, joining with Mycronic will enable MRSI to continue to deliver best-in-class automated die bonding and dispensing systems and to accelerate exciting innovations in our hardware and software," said Michael Chalsen, president of MRSI, in an email to customers. "With access to the significant resources and geographic reach of a larger group, we intend to invest even further in our global sales and customer support teams and to extend our global reach by entering targeted new markets."

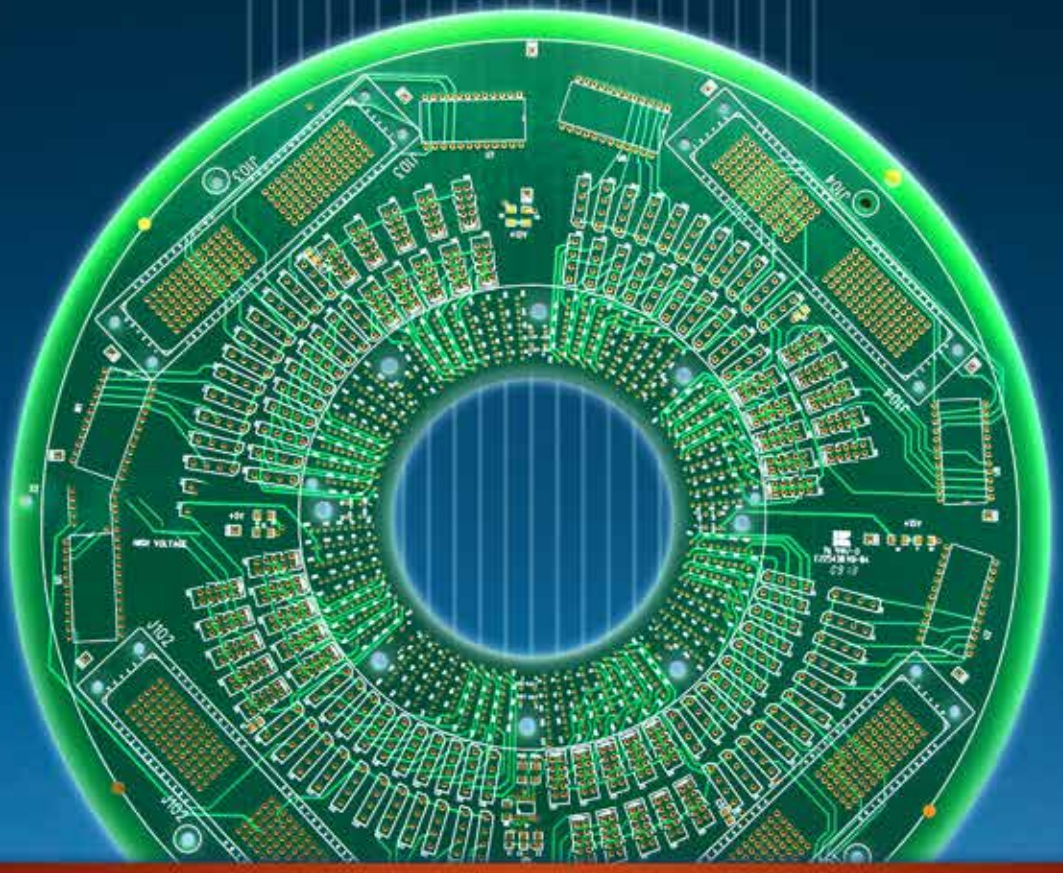
MRSI Systems will honor all existing agreements and outstanding purchase orders and quotations in accordance with their terms, and all key sales, customer service and technical points of contact will remain the same, Chalsen said. – *MB*

Yamaha Motor will open an Advanced Technology Center in Yokohama City, where it will study robotics, artificial intelligence, and promote open innovation.

Yekani Manufacturing opened a 301,000 sq. ft. "smart manufacturing" facility in the East London Industrial Development Zone in South Africa. The contract assembler invested $78 million in the new plant, which is equipped with 11 SMT lines and will ultimately employ up to 1,000 workers.

Zytek EMS, a contract electronics assembler in Milpitas, CA, is closing its factory and selling its assets at auction.

PCBCART



FREE BUT PRICELESS SERVICES FOR YOUR PCB FABRICATION

We are a China-based custom PCB fabrication service provider with over 10 years' experience. Except for full feature manufacturing capabilities, we also have multiple free but priceless services to ensure you get superior PCBs within budget!

- Free Panelization
- Custom Layer Stackup
- Valor DFM Check
- Advice on Cost Reduction
- Electrical Test & Flying Probe Test
- Parts Sourcing & Assembly Services Available

We Balance The "Iron Triangle" - Cost, Time & Quality Incredibly

SALES@PCBCART.COM WWW.PCBCART.COM

ISO TS 16949 RoHS UL Pb lead-free IPC

'UP-SIDE'

Trends in the electronics equipment market (shipments only).

	% CHANGE			
	FEB.	MAR.	APR.	YTD%
Computers and electronics products	-0.3	-0.8	1.2	5.4
Computers	1.3	-3.3	3.4	-15.9
Storage devices	-13.6	-12.2	10.3	-49.4
Other peripheral equipment	-9.6	-6.0	19.6	19.8
Nondefense communications equipment	-2.3	1.9	2.9	12.2
Defense communications equipment	0.0	1.1	0.4	8.2
A/V equipment	11.6	-1.7	-3.0	-13.2
Components[1]	-0.3	-1.9	0.2	6.7
Nondefense search and navigation equipment	-2.1	-0.9	3.2	7.8
Defense search and navigation equipment	-4.3	-0.9	1.0	5.1
Medical, measurement and control	0.9	1.7	0.3	12.1

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, June 4, 2018

Semi Industry Boom Still Has Life

MILPITAS, CA – The semiconductor industry is nearing a third consecutive year of record equipment spending, with projected growth of 14% year-over-year in 2018 and 9% in 2019, according to SEMI.

Over the semiconductor industry's 71-year history, only once before – in the mid '90s – has the industry logged four consecutive years of equipment spending growth, says the organization.

Korea and China are leading the growth, with Samsung dominating global spending and China on a steep rise, surging ahead of all other markets, says SEMI. Samsung accounts for 70% of all investment in Korea.

China's equipment spending is forecast to increase 65% in 2018 and 57% in 2019. Domestic, Chinese-owned companies – backed by large government initiatives – are building a considerable number of new fabs that will start equipping in 2018. The companies are expected to double their equipment investments in 2018 and again in 2019.

Other regions are also ramping investments. Japan is increasing equipment spending 60% in 2018, Europe and Middle East will boost investments 12%, and Southeast Asia will see investment jump more than 30% in 2018.

AR/VR Spending to Grow 72%

FRAMINGHAM, MA – Worldwide spending on augmented reality and virtual reality (AR/VR) is forecast to achieve a five-year CAGR of 71.6% over the 2017-2022 forecast period, according to IDC. Spending on AR/VR products and services is forecast to reach $27 billion in 2018, up 92% year-over-year.

The consumer industry maintains its position as the largest source of spending for AR/VR products and services over the course of the forecast period, reaching $53 billion by 2022. This is followed by spending in the retail, discrete manufacturing, and transportation industries, representing $56 billion collectively by 2022.

METALS INDEX

DATE	6/5/17	3/5/18	4/2/18	4/30/18	6/4/18
LME Cash Seller and Settlement for Tin	$9.28	$9.85	$9.53	$9.75	$9.38
LME Cash Seller and Settlement for Lead	$0.95	$1.15	$1.09	$1.06	$1.10
Handy and Harman Silver (COMEX Silver)	$253.07	$239.45	$240.01	$241.86	$240.38
LME Cash Seller and Settlement for Copper	$2.57	$3.13	$2.99	$3.11	$3.07

Global Shipments of PCDs to Decline 4% in 2018

FRAMINGHAM, MA – Global shipments of personal computing devices (PCDs) are expected to decline 3.5% year-over-year in 2018, says IDC. Looking ahead, PCDs are expected to drop at a five-year CAGR, down 1.8%.

PCDs are composed of traditional PCs (desktop, notebook, and workstation) and tablets (slate and detachable).

Desktop PCs are expected to see a five-year CAGR decline of 2.6%.

Hot Takes

- The global automotive cockpit electronics market will grow at a CAGR of 16.1% from 2017 to 2022. (ResearchAndMarkets)
- Year-over-year semiconductor growth was nearly 22%, and revenues climbed to more than $358 billion in 2017. (New Venture Research)
- April orders at PCB manufacturers in Germany, Austria and Switzerland rose 25% year-over-year. (ZVEI)

US MANUFACTURING INDICES

	JAN.	FEB.	MAR.	APR.	MAY
PMI	59.1	60.8	59.3	57.3	58.7
New orders	65.4	64.2	61.9	61.2	63.7
Production	64.5	62.0	61.0	57.2	61.5
Inventories	52.3	56.7	55.5	52.9	50.2
Customer inventories	45.6	43.7	42.0	44.3	39.6
Backlogs	56.2	59.8	59.8	62.0	63.5

Sources: Institute for Supply Management, June 1, 2018

KEY COMPONENTS

Book-to-bills of various components/equipment.

	DEC.	JAN.	FEB.	MAR.	APR.
Semiconductor equipment[1]	28.3%	27.5%	22.5%	16.9%[r]	26%[p]
Semiconductors[2]	22.5%	22.7%	21%	20.2%[r]	20.2%[p]
PCBs[3] (North America)	1.15	1.16	1.17	1.13	1.08
Computers/electronic products[4]	5.41	5.42	5.45	5.45[r]	5.40[p]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [p]preliminary, [r]revised

Available courses:

IPC Designer Certification
IPC Advanced Designer Certification

September 7-10th, 2018

Enroll today, space is limited.

1-800-64-EPTAC or visit eptac.com/pcbwest2018

$1,960 each plus shipping for prep materials prior to class

Innovation never gets old.

eptac
TRAIN. WORK SMARTER. SUCCEED.

PCB WEST 2018
Conference & Exhibition

EPTAC makes it easy. Complete the course, pass the exam, receive your certification.
Best of all, add credentials to your technical expertise with an industry recognized certification.

Call **1-800-64-EPTAC**, email **sales@eptac.com** or visit **eptac.com** to find a class near you!

Bound to Break?

Are otherwise global companies putting all their R&D eggs in one basket?

BUYING CARS IS not what it used to be. I was recently kicking the proverbial tires in search of a new automobile. This was the 18th time I underwent this process, one I approached with mixed emotions. It's always interesting to see what new technology, appearance and driving experience has been packed around an engine riding on four tires. Yet it's also concerning, as the cost always triggers a rethink of my priorities and change in my expectations.

This time around, the two biggest areas of technological interest also provided the greatest areas of concern. One was the lack of familiar knobs, dials and gauges. For the seasoned driver, this can cause initial, if not ongoing, confusion while navigating heat, air conditioning, music, and all the other things cars can do. The second was the lack of a spare tire. Many cars (or their manufacturers) are being touted as so reliable, spare tires are no longer necessary. Just deploy the tire repair/inflator (if you can find it on the knob-less dashboard) and away you go.

But concerns soon outweighed the wow of new technology. What if I cannot see an important piece of information because my electronic dashboard is in the wrong mode? What happens if I get a flat driving in a desolate place and the auto-repair option fails to inflate the tire?

Our industry has parallels to the state-of-the-art automobile. While we are familiar with what it does, we all must adapt to how it does it! In some cases that means learning new skills, such as how to program the dashboard, audio and climate control systems so they work as needed, when needed. The other is remembering some old skills, so if a system fails, you have a backup plan you know will work.

Our industry is one of the most innovative on earth. New technology, methods and processes are developed, refined and implemented at a pace simultaneously breakneck and yet accelerating. We should be duly proud. However, we should equally be aware that how we are going about these advances is also evolving, and may be creating risks that are not fully understood.

Recently, while reading a summary of activities taking place in our industry, it dawned on me that while the mix of companies initiating, sponsoring and developing new technologies was truly global insofar as the country of incorporation, the development work and innovation was being performed in a common place. All companies fully understood where they could get the best bang for the buck in R&D, and all agreed that was the place to base such activities. Have those companies thought through the potential concern of having too many eggs in one basket, especially when some global political leadership appears to not fully understand either the benefits or responsibilities of a truly global economy?

Deciphering the tea leaves of risk and reward requires a solid set of gauges and controls that are not just dependable, but consistent and easy to read. Problems rarely pop up when the operating environment is known and consistent. Disaster can occur, however, when an unexpected event takes place and either the controls cannot be operated quickly or are so difficult to understand, they get ignored. Such concerns need to be thought through when committing resources of a business, not just in what it hopes to accomplish but how it plans to do so. What you plan to do may be repetitive and well understood. Yet if the manner or the environment in which you are going to do those tasks begins to change, extra effort has to be invested to fully understand the changing gauges and controls and avert disaster.

In a car, the learning curve to operate the infotainment system is real, and concerted effort needs to be taken to competently operate the system. I know too many people who wait until they are almost in an accident before deciding to take such actions for their own safety, if not enjoyment. The lack of spare tire should make everyone think just a little about "what if" they get a flat. Will the new high-tech system work as planned, or should there be a Plan B just in case? And if so, what would that be?

My new car required my adjusting. I had to read what seemed like a zillion pages of instructions to be able to listen to local news, traffic reports and see how much gas was in the tank. A web video explained how the spare-less tire "safety" system works. It also made me realize that as neat as it is, I had better pay more attention to road conditions where I drive.

Those with corporate risk management responsibilities also need to be thinking about adjusting. And they need to determine if they have the tools to be able to see, and ultimately understand, in the most timely and accurate way, the new risks they may have while conducting their business. Most important, do they have the necessary protection – the "Plan B" – in place to avert disaster should they find their emergency systems either have been removed or replaced with complex controls that are not easily understood. Everyone must adapt and be aware of change, whether it comes as a new car or as an evolving business environment. PCD&F/CA

PETER BIGELOW
is president and CEO of IMI (imipcb.com); pbigelow@imipcb.com. His column appears monthly.

semi™

Connect · Collaborate · Innovate

SEMICON® TAIWAN

FUTURE STARTS HERE

SEPT 5-7, 2018

Taiwan Taipei Nangang Exhibition Center Hall 1, 1&4 F

Co-located with

I see the future

ISiP GLOBAL SUMMIT 2018

semicontaiwan.org

ECTC Boasts Record Crowds, FO-WLP Sessions Overflow

Whether round or rectangle, HDI will be required to meet the needs of next-generation semiconductor nodes.

THE IEEE ELECTRONICS Components and Technology Conference (ECTC) welcomed a record crowd of more than 1,700 attendees to San Diego to discuss the latest trends in packaging and assembly.

For the second consecutive year, fan-out wafer level (FO-WLP) packaging sessions reached overflow capacity as attendees streamed in to hear the latest developments. Regardless of format, round or rectangle, high-density interconnect will be required to meet the needs of next-generation semiconductor nodes – 7nm coming soon and 5nm to follow. Die-to-die and die-to-high bandwidth (HBM) memory stack (as described by Nvidia) requires high density interconnect. MediaTek announced its INFO (M-Link), a die-to-die networking solution using TSMC's InFO on substrate process, and provided reliability data and signal and power integrity analysis.

Many presentations described efforts to obtain finer feature sizes. TSMC discussed a new submicron polymer redistribution layer (RDL) technology for its InFO package. Atotech, Dow and others described plating developments, while equipment companies, including Applied Materials, Rudolph, SPTS, Suss Microtec, TEL NEXX, ULVAC, Yield Engineering Systems and Disco, introduced improved process solutions. Rudolph and Ultrasonic Systems discussed a new lithography system with a novel nozzleless spray coating technology. New material developments for FO-WLP from Brewer Science, FujiFilm, Hitachi Chemical, Lintec and Nagase ChemteX were also presented.

TSMC's expanded Integrated Fan-Out WLP (InFO-WLP) platform extends to more than application processors, with stacking options and a version that incorporates an antenna in the package called InFO_AiP. IME described research on an antenna in an FO-WLP. The antenna-in-package options are increasingly important for mmWave applications, including 5G, but FO is not the only option. ASE, SPIL, NCAP, Georgia Tech, IBM and Toshiba presented developments in other package options incorporating antennas.

Large-area panel processing attracted tremendous attention as a potential cost-reduction measure. Nepes presented its panel development, with a fingerprint sensor as the first product. Samsung Electro-Mechanics (SEMCO) detailed its chip-first FO panel with 2µm lines and spaces. Researchers found less warpage with a glass carrier than organic carriers. Panel yield will be critical to obtain the economic advantages. Researchers from Fraunhofer IZM and TU Berlin described the latest developments from their consortium and provided a realistic assessment of large-area processing issues and opportunities for research to move the technology forward. Several presentations from the consortium led by ASM Pacific Technology (with members Unimicron, JCAP, Dow, Huawei, Indium and Hong Kong S&T) described developments on panel processing.

Consortia such as ITRI, IME A*Star, Korea Advanced Institute of Science and Technology (KAIST), Ncap, Imec, along with companies including Amkor, ASE, Huatian, MediaTek, NANIUM, SPIL, and Stats ChipPac also discussed advances with FO-WLP. ASE compared electrical performance of eWLB, M-Series, and a chip-last approach.

New FO-WLP panel consortia launched. A new consortia organized by Hitachi Chemical called Jisso Open Innovation of Tops (JOINT) was unveiled for the first time at ECTC. Members include AGC Asahi Glass, Disco, JSR, Lintec, Namics, Mitsui Kinzoku, TOK, Toray Engineering, TOWA, Uyemura and Ulvac. Unimicron joined the consortia during the conference. The material and equipment vendors are coming together to advance the large area technology using an RDL-first fan-out test vehicle design by Hitachi Chemical. The 24 sq. mm package, fabricated on a 320mm square panel, features a four-layer RDL with 2µm minimum line and space. Eight chips are mounted with a minimum bump pitch of 40µm. Development will use Canon's stepper, with a large-area flip-chip bonder from Toray Engineering used to bond the chips. TOK will provide photoresist, and Uyemura will provide the copper electroplating solution. Ulvac's sputtering system, Shikoku's OSP, and Mitsui Kinzoku's glass carrier will be used. Hitachi Chemical will provide dielectric, mold compound and underfill for the first test vehicle.

Artificial intelligence. AI and its impact on system design was the subject of a plenary session that featured presentations from GlobalFoundries, IBM, Microsoft, Georgia Tech and Samsung. A keynote lunch speaker from Broadcom described packaging advancements to enable AI, with applications ranging from autonomous cars to wearables.

In an evening session on high-density packaging technologies in the era of big data, speakers from Fujitsu, IBM Research, JCET, Stats ChipPac, Shinko Electric, and Hitachi Chemical discussed some of the packages required.

Silicon interposers with through-silicon via (TSV) are now mature products for high-performance applications, as indicated in several presentations. Xilinx provided a comprehensive study on package design for board-level reliability in thermal cycling and power cycling for its silicon interposer with package. Nvidia described a micro-bump system for its second-generation GPU and HBM on a silicon interposer.

E. JAN VARDAMAN
is president of TechSearch International (techsearchinc.com); jan@techsearchinc.com.

Wafer-to-wafer bonding. Wafer-to-wafer (W2W) bonding is a hot topic, especially with TSMC's announcement of its W2W bonding this spring. IMEC presented its failure analysis for 1.8µm pitch wafer-to-wafer bonding. The Institute of Microelectronics and Tsinghua University discussed a low-temperature fine-pitch wafer-level Cu-Cu bonding using PVD fabricated nanoparticles. National Taiwan University and the Joining and Welding Institute at Osaka University described a low-temperature Cu-Cu bonding using a microfluidic electroless interconnect process. Xperi described a low-temperature hybrid bonding process to bond interconnect at <20µm.

Automotive reliability and power devices. Automotive electronics also remains a hot topic. Reliability requirements are especially important. A presentation from Texas Instruments described corrosion prevention for Cu-wire bonded devices to improve bonding reliability. Intel discussed underfill degradation in packages for ADAS. A presentation from researchers at Georgia Tech focused on high temperature and moisture aging for power packages. A joint presentation from Keio University, Alpha Assembly Solutions/MacDermid clarified the warpage and thermal stress for SiC and Si power devices using a direct Ag sintering clip-attachment on a Cu plate.

Emerging technology. A special session on emerging technologies for medicine, healthcare and human-machine interfaces opened the pre-conference special sessions on Tuesday morning. The focus was on soft materials, processing, and manufacturing methods, and the utilization of flexible hybrid electronics for these applications. Speakers from University of Minnesota, University of California, Psyonic and Microtek described the latest developments.

A special session on novel assembly methods to manipulate ultra-thin, small chips with high throughput covered a range of topics from microLED displays to advanced memories. Speakers from Darpa, PlayNitride, Besi, X-Celeprint and Uniqarta provided insight into some of these methods. PlayNitride and X-Celeprint highlighted the potential for microLED assembly.

Additive manufacturing featured a presentation from Texas Instruments that discussed additive printing technology for IoT, 5G and automotive radar applications. CEA-LETI researchers described the use of a 3-D printing encapsulation process. Researchers at Georgia Tech discussed printed electronics for wearable RF antennas, and researchers at ASU discussed printed electrochromic films for wearable electronics.

The importance of co-design. One night session focused on IC and package co-design for heterogeneous integrated systems. Avi-Bar Cohen from Raytheon, the current IEEE EPS president, and Chris Bailey of University of Greenwich led the discussion. Representatives from ASE, Mentor, ON Semiconductor, Lamar University, Georgia Tech and University of California, San Diego highlighted the importance of co-design.

Reliability, sintering pastes, power electronics, nanotechnology, biochemical, optoelectronics with a focus on silicon photonics, advances in wire bonding, materials, flip-chip manufacturing challenges, RF modules, through-silicon via (TSV), and thermal characterization sessions rounded out the program. Several sessions discussed the issue of warpage with wafers, silicon interposers, fan-out WLP, package-on-package (PoP), panel-level fan-out, and laminate substrates, including PBGA.

A special session was devoted to emerging packaging technologies for 5G and advanced computing. Several presentations at the conference discussed new material developments for 5G.

Interactive poster sessions allowed in-depth, one-on-one discussions with the authors. Many new exciting developments are often presented in these sessions. These included a 3-D-printed liquid jet impingement cooler from IMEC and KU Leuven, and Smoltek's integrated fully solid-state capacitor based on carbon nanofibers and dielectrics.

The Heterogeneous Integration Roadmap also held a meeting to continue its roadmap development activities. A special session discussed how to enhance women's participation in engineering around the globe. Funding for the IEEE Foundation Frances B. Hugle Memorial Scholarship was announced with contributions from 100 individuals and corporations. Bill Chen's contribution to the scholarship from his IEEE Electronics Packaging Field Award honoring his wife allows the application process for young women in engineering to begin.

Next year, ECTC will be held in Las Vegas May 28-31. The Electronics Packaging Society (EPS) expects another record attendance. **CA**

Engineering Multi-GHz Systems is Driving Design to Deeper Levels

How smoother surfaces and rounder edges help keep us all safer and more connected.

MAKING THE IMPOSSIBLE possible with advanced technology is a frequently recurring theme in advertising today. It seems the wider world has finally "got" science; well-known high-tech brands are comfortable explaining how their technologies are enabling new and fantastic smartphone features, more immersive gaming and TV viewing experiences, safer more relaxing travel in our increasingly autonomous vehicles, among others.

Of course, we in the electronics industry are intimately familiar with the underlying innovations enabling these previously unimaginable new experiences. As digital computing capabilities advance at the speed of Moore's Law – or, in some cases, even faster – system capabilities are making incredible gains, while at the same time physical size, power consumption and cost are reduced, resulting in new generations of products at once more user-friendly and affordable.

Automotive autonomous-driving systems provide a great example. Advanced safety features in particular have a habit of quickly transitioning from high-end options to mandatory fitments, as governments pursue the vision of zero road fatalities. Autonomous driving modes like pedestrian detection, collision avoidance, lane assist and adaptive cruise control can significantly reduce accident rates, and will be more in demand. Automotive radar will be critical for many of these systems, providing one of the most important senses alongside modes like visual sensing and lidar.

Once a high-end option, operating in the 24GHz band and supporting limited functionality, the latest 77GHz technology permits greater distance, speed and angular resolution suitable for mandatory safety systems within the tight space and power constraints of today's vehicles.

There are already moves to use even higher frequency bands, such as 120GHz, in the future. The higher-frequency systems can also handle close-up work like parking assist or even monitoring passengers inside the vehicle to support features like gesture control. On the other hand, moving and manipulating the data from high-frequency radar, at multi-Gb/s rates, requires serious attention to engineering details all the way down to the physical properties of cables, interconnects and circuit boards.

The cellular world is facing similar challenges, as 4G-LTE and 5G standards evolve to meet ever-growing bandwidth demands from increasing numbers of subscribers. And, of course, the impact of communications with the tens of billions of smart "things" we expect to see connected to the Internet is yet to be fully felt. 5G is expected to take off in the US and China this year, although economic factors will likely dampen European operators' enthusiasm for a while yet.

These advanced cellular technologies, based on dual frequency-division multiplexing and operating at 6GHz antenna frequency to support the channel density and data rates demanded by modern digital lifestyles, can be highly vulnerable to background noise and distortion caused by unwanted effects such as passive intermodulation (PIM).

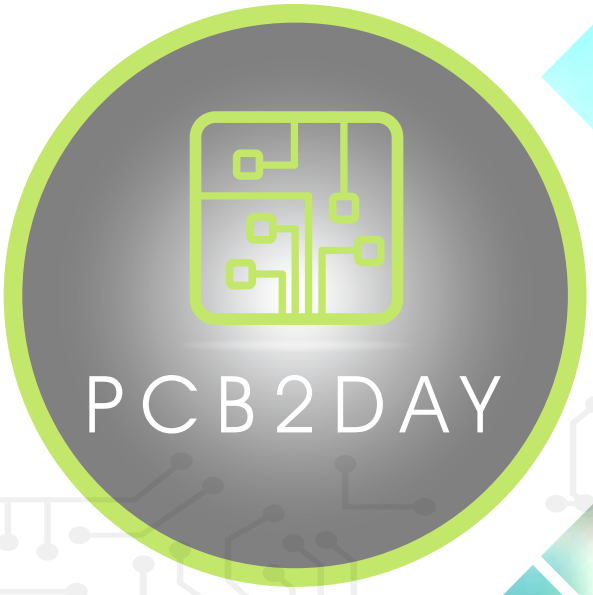
PIM is a key concern for network operators, infrastructure suppliers, installers and test-equipment manufacturers. The causes can be minute factors, such as unbalanced concentrations of electrons at sharp edges, or magnetic hysteresis in materials near the signal path. Even a rusty metal structure in the vicinity of an LTE mast is a potential cause of PIM distortion that can result in dropped connections, missed calls, or bit errors that waste data bandwidth – ultimately translating into lost revenue for operators.

Overcoming the challenges to signal integrity in the multi-GHz world demands minute attention to detail, including aspects such as the properties of materials that make up connectors and cables, and even the surface finish of conductors. It's an environment plagued by anomalous effects, like skin effect and transverse electromagnetic mode (TEM), that have a profound effect on signal propagation. Above a few GHz, the skin depth for copper is significantly less than one micron, so a poor or inconsistent surface finish can cause disruptive losses and reflections. The resistivity and magnetic permeability of conductors also have an important effect on signal transmission, as do the effects of dielectric materials associated with the transmission lines.

The challenges to signal integrity are intensifying, but are not entirely unforeseen. It's been heading this way for some time, and countermeasures like low-PIM cables and connectors are already in the market. As far as printed circuit materials and processes are concerned, standard substrates are known to be unsuitable at signal frequencies above about 500MHz. Low dissipation factor (Df), low dielectric constant (Dk) laminates and prepregs have evolved with moves toward generally higher signal frequencies throughout electronics applications. Low Df and Dk give designers more freedom to optimize copper trace widths, spacing, and PCB thickness to maintain signal integrity and meet other design constraints such as size and cost.

continued on pg. 48

MARTIN COTTON
is director OEM projects at Ventec International Group (ventec-group.com); martin.cotton@ventec-europe.com.



Control of Noise, EMI and Signal Integrity in
High Speed Circuits and PCBs

A two-day workshop featuring

RICK HARTLEY

CHICAGO - ILLINOIS

OCTOBER 25 & 26

$595

through

Sept. 24th

pcb2day.com

Maximizing High-Speed Performance in Flex Boards

Flex circuits can run 10+Gb/s signals, but many factors need to be met.

CAN FLEX CIRCUIT boards run 10+Gb/s signals? Answer: Multiple factors must be juggled to successfully run signals that are 1Gb/s and above on flexible circuitry. I will address each of them individually.

Controlled impedance. Just like any high-speed rigid PCB, a successful high-speed flex design will have to incorporate a target characteristic impedance. To do so, match the characteristic impedance of the flex to the rest of the system to ensure minimal reflections and crosstalk. This can have negative consequences for mechanical performance, however. Elevated impedance requirements typically equate to thicker dielectrics, thereby making the circuit much less flexible.

The impedance value of a circuit is driven primarily by the signal trace width, the layer-to-layer spacing between signal trace and reference plane, and the dielectric constant (Dk) of the insulating material between the signal and plane. For most flexible-circuit manufacturers, yields start to drop when trace widths fall much below 0.003" (0.0762mm), so any significant trace width reduction beyond that can have a hefty cost impact. Also, traces under 0.005" are fragile and may develop cracks in tight bend-radius applications.

If flexibility is a concern, raising the dielectric thickness between signal and plane layers is not a great option because of the additional stiffness it will create. The Dk of standard polyimide with thermosetting epoxy or acrylic adhesive ranges between 3.2 and 3.5, which is not great if the goal is elevated impedance combined with a circuit that will bend without breaking.

Many flex designers use a cross-hatch pattern for the reference plane(s) rather than solid copper (**FIGURES 1-3**). This trick will bump up impedance without the need to decrease signal trace width or increase dielectric thickness. The downside to using cross-hatched shields is increased insertion loss. Depending on how much loss the system can tolerate, this may or may not be feasible. If all the limits have already been pushed and higher impedance is still needed, consider some less-common insulating materials that have a lower Dk. Most of these materials also have lower insertion loss, which is a perfect segue to the next topic.

Insertion loss. Most high-speed signals are very small and cannot afford to lose any amplitude on the way to their termination. And just like impedance mismatches can cause reflections that degrade small signals, high insertion loss materials surrounding the signal traces can eat up a lot of signal strength. Several available materials offer lower insertion loss, and at the same time lower Dk. Everyone wins, right? Well, sort of, but at a cost. Most of these materials are thermoplastics like Teflon and LCP (liquid crystal polymer), which are very expensive and not particularly easy to work with. Processing temperatures for laminating LCP and Teflon are upwards of 300°C. Since processing temperatures for laminating standard epoxy or acrylic adhesive are under 200°C, many flex manufacturers lack proper high-temperature lamination equipment required to run LCP or Teflon. This will reduce the potential vendor base.

Additionally, most high-speed materials have a propensity to be considerably more difficult to work with than standard epoxy- or acrylic-based flex materials. Unlike standard thermosetting adhesives, which cure and then stay put in subsequent laminations, thermoplastic high-speed adhesives can re-melt and permit features to move and shift if extreme care is not taken during additional lamination cycles. It's easy to divine that the increased raw material cost, limited vendor base, and complicated processing will have a significant impact on final circuit cost. Some newer materials combine low Dk values and low insertion loss with lower lamination processing temperatures (very similar to epoxy and acrylic). While the newer raw materials are still more expensive than standard flex materials, the relative ease-of-processing can soften the blow on cost with improved yields and also a larger vendor base.

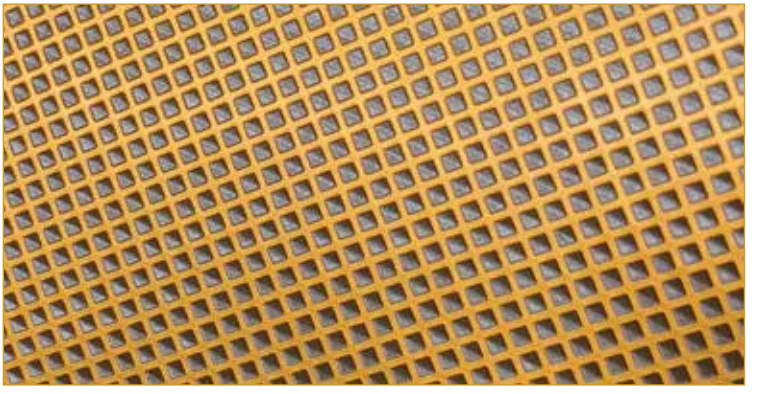


FIGURE 1. The most common cross-hatch pattern is a series of perpendicular traces forming a "screen" image. This pattern runs at 45° to the signal traces.

MARK FINSTAD is senior application engineer at Flexible Circuit Technologies (flexiblecircuit.com); mark.finstad@flexiblecircuit.com. He and co-"Flexpert" **NICK KOOP** (nick.koop@ttmtech.com) welcome your suggestions. The authors will speak on flex design and manufacture at PCB West in September (pcbwest.com).

Rigid-flex considerations. Rigid-flex circuitry has additional concerns to be dealt with since any signal running from a rigid area, across a flex section, and back into a rigid area will travel through very different materials. Sensitive signals should be kept within individual rigid areas whenever possible. If signals must bridge a flex section, perform impedance calculations for both the flex and rigid areas, and adjust trace widths to provide matching values.

Ensure any conductor width changes occur on the rigid side of the flex-rigid transition, *not* on the flex side! A conductor width change on the flex side of the flex-rigid transition could result in a stress concentration point, which in turn could cause the trace to crack when the circuit is flexed. Discuss with your fabricator high-speed materials used in the rigid sections of the circuit. Not all high-speed rigid materials have a matching *no-flow* prepreg adhesive.

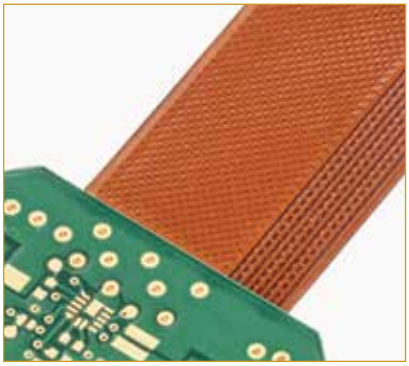


FIGURE 2. This image is a solid plane with round dots removed to provide a cross-hatch pattern.

FIGURE 3. Honeycomb cross-hatch pattern.

No-flow prepregs are required in the construction of rigid-flex designs to ensure the prepreg does not flow into flex areas during lamination.

Terminations. At some point high-speed flex must be terminated with compatible connectors that can maintain an uninterrupted signal return path and also offer matched impedance. While most connectors designed to be mounted to rigid PCBs can also be mounted to flex, it is important to ensure any connector selected is compatible with flexible circuitry. And as always, it is wise to enlist input from the flex-circuit manufacturer on all these attributes early in the design process to ensure the final high-speed flex is both cost-effective and will perform as expected. PCD&F

7 Habits of Highly Efficient PCB DESIGNERS

Flexibility, preparation and passion are an effective combination. **by JOHN MCMILLAN**

Every step taken during the printed circuit board (PCB) design process is taken purposefully. This article describes seven habits that highly efficient PCB designers take as they study, prepare, visualize, strategize and complete PCB designs.

1. Pay attention to details. From creating the schematic symbols to polishing the layout for fabrication, assembly and test, even the smallest missed detail can make or break a PCB design. Efficient designers make it a point to understand every aspect of the design flow, and when in doubt, they check things out. Preparation is key. It starts long before the PCB layout tool is launched. From building symbols and component land patterns from scratch, to obtaining them from tool libraries or online resources, designers check them out. Why? Because they can't afford for them to be incorrect, no matter the source, since a single incorrect symbol or land pattern alone can result in a costly board re-spin.

Reviewing the design's bill-of-materials (BoM) and component datasheets to verify the component dimensions and pin-out is time well spent. Whether it's adding stitching vias to connect power or ground fills and planes or additional silkscreen notations, effective PCB designers understand all the electrical design aspects and requirements necessary for an optimal design.

2. Study, plan, strategize, execute and be prepared to regroup quickly. Efficient PCB designers must become familiar with the schematic and think multiple steps ahead. Understanding the design's schematic enables the designer to expedite placement. For example, defining groups or rooms of associated components helps expedite component placement. Designers should understand the applications for discrete components like decoupling capacitors and bypass resistors, why and where they are needed, their proximity to the component leads and even when necessary on unused pins.

Efficient PCB designers also know the value of setting up the layout session properly and are resourceful. They know

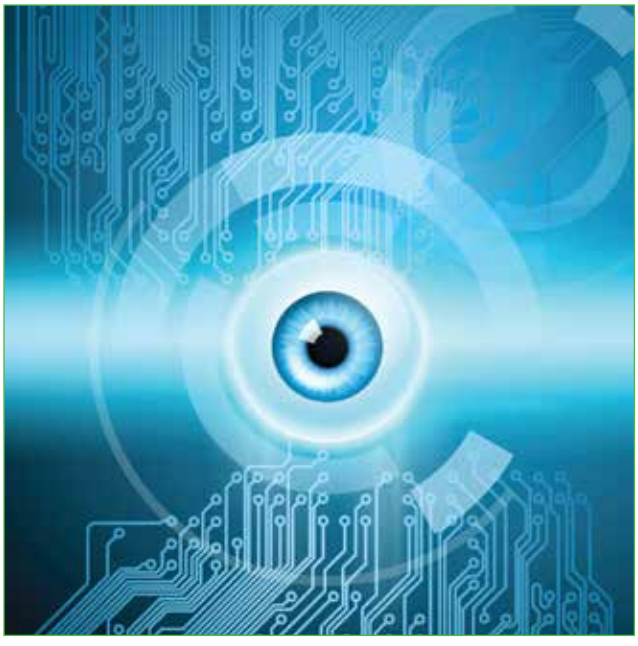


FIGURE 1. "Creativity is intelligence having fun!" – Albert Einstein

FIGURE 2. "None of us is as smart as all of us." – Ken Blanchard

how to apply design constraints and rules that ensure they are followed during placement and interactive and autorouting phases. They may develop route studies and strategies that prioritize nets to ensure that even the most extensive rules-driven designs are accomplished. Let's face it, changes happen. There can be a variety of reasons for design updates: perhaps a part is no longer available, or a component like an FPGA requires a new pin-out. It is not uncommon for a designer to get an updated netlist, or perhaps several updates, during layout. The ability to regroup and adjust quickly is critical for PCB designer efficiency, especially if the design's release schedule is time-sensitive.

3. Visualization. Component placement is a critical step and sets the stage for successful layout. Component orientation, top or solder placement, spacing that avoids shadowing and ensures optimal solderability, and testing are just a few of the details designers are aware of, plan for and visualize. Factors such as aligning components and breakout vias help ensure routing lanes are not blocked. Efficient PCB designers can study a ratsnest of connections and begin to visualize and plan a routing strategy before the first trace is connected. They know what should be routed manually and what can be autorouted. Efficient PCB designers may even use specific techniques to steer routing by placing route boundaries or temporary fences and keep-out areas.

Efficient PCB designers visualize the design not only from a layout perspective but also from a manufacturing perspective. They are aware fabricators have their own internal processes and design rule checks. Details such as knowing which components require additional placement room during layout, perhaps driven with placement boundaries, for example, can minimize or totally eliminate rework time after boards are fabricated.

4. Value working with and consulting with peers. As singer Vanilla Ice raps in "Ice Ice Baby," "stop, collaborate and listen." Efficient PCB designers don't work in a vacuum. They understand the value of collaboration. Early on, for example, they work closely with mechanical design teams to ensure the design's board outline, mounting holes and the locations of all physical interfaces, such as connectors, LEDs, displays, etc., are adhered to. And when identified, they provide valuable feedback to mechanical teams that can improve the design. They embrace ECAD-MCAD collaboration and keep the end-product in mind throughout the PCB layout phase.

Understanding the design requirements such as design rules and signal integrity constraints that drive connectivity is a must. The design process may include specific SI engineers that use models, run simulations and apply strict routing and timing rules, such as defining net topologies and differential pairs with minimum and maximum trace lengths, matched lengths, maximum separation, etc.

Collaborating is essential to PCB design success. Depending on the size of the business and complexity of design, collaborating can include component and model librarians, EMC, thermal, QC and NPI engineers, even board fabricators. Even the best PCB designers understand the value of peer reviews. Some designers can be so involved, they may overlook something as simple as a missing or misplaced reference designator, or nonfunctional pads on internal layers were not removed.

FIGURE 3. "Pleasure in the job puts perfection in the work." – Aristotle

5. Strive for perfection. Do you remember a class in school where a score of 95% was an "A" grade? Well, that's certainly not "passing" in PCB design. In fact, even the smallest error such as an incorrect pad size or a single trace too close to a mounting hole can result in a respin. Efficient PCB designers do everything they can to achieve design perfection. From online design rule checks (DRC) and designing for manufacturing and assembly (DfMA) checks, every effort is made to ensure the design work is accurate.

Design reviews are critical to eliminate ambiguity between design stakeholders. Effective PCB designers often use specific post-design programs that combine capabilities of design for manufacture (DfM) and new product introduction (NPI). These tools ensure a smooth transition to fabrication, assembly and test from the PCB design environment.

6. Continue to learn. All PCB design steps, processes and procedures referenced here are derived from education, training and hands-on experience. First and foremost, a strong foundation is absolutely essential to being a PCB designer, especially with the pace with which new components, technologies and processes are evolving. Continuing education is a must in electronic product design. Continuing education includes keeping up with the latest industry standards, including ones from IPC, ANSI, the military, etc., as well as PCB fabrication and assembly processes. PCB designers contend with a constant stream of new and improved components, packages, fabrication and manufacturing, pre- and post-test and assembly processes as well.

Effective PCB designers understand they are not an island, but rather are part of a greater community of designers with a common goal. They subscribe to publications like PCD&F and Circuits Assembly, are either members of or regularly attend IPC Designers Council chapter meetings and conferences, and may even present papers to peers at PCB conferences like PCB West. Many designers even seek industry credentials or certifications through training and testing, like IPC's Certified Interconnect Designer (CID) programs.

7. Their designs reflect their passion. Insomuch as canvas is the medium of an artist, PC monitors are the virtual canvas for PCB designers. In fact, give an identical design database to 10 different PCB designers, and the finished result can look quite different. Said differences may be subtle or visibly noticeable, as each PCB designer has their own unique design style in which items that aren't immutable or fixed can be tailored and custom.

Rarely, for example, does a PCB designer kick-off an autorouter and is 100% percent satisfied with the finished result. Typically, designers will choose to hand-route physical interface connections or sections of highly constrained busses like DDR. Nets with T-points, clocks, TX and RX traces, RF circuitry, etc., are also considered for partial or complete pre-routing. Trace characteristics such as corner chamfers and tuning (rule-based) are just some of the other design elements that may vary from designer to designer.

Conclusion

I referred to PCB design as a complex puzzle. It starts with a design envelope that provides the frame, a set of components to be logically and strategically placed, and a schematic diagram with guides and rules that represent how components are interconnected. There is, however, no picture on the top of a box of the finished product, since every placed component, trace, pad and other feature is by design. Developing design habits that expedite design completion, improve design quality and enhance productivity are instrumental to highly efficient PCB design. PCD&F

JOHN MCMILLAN is product marketing manager at Mentor Graphics (mentor.com); john_mcmillan@mentor.com.

PCB WEST 2018

Conference & Exhibition

Conference:
September 11 – 13
Exhibition:
Wednesday, September 12

Widely recognized as the best training for PCB design and engineering

- **Nearly 70 sessions; hot topics include:**
  - **Reverse engineering, and how to stop it**
  - **Fine-pitch BGA design**
  - **Noise control in high-speed electronics**
  - **And much more!**
  - **Plus, Mentor CEO Wally Rhines addresses the future of the PCB design industry**
- **All-day tutorials on transmission lines, DfM, and assembly process troubleshooting**
- **Speakers from TTM Technologies, NXP Semiconductor and more top companies**
- **One-day exhibition with 100+ leading suppliers and services**
- **15 FREE technical sessions ranging from design to fab to assembly**

REGISTER NOW

CONNECTING
DESIGN
TO FAB
TO ASSEMBLY

Santa Clara Convention Center, CA

pcbwest.com

Register by August 13 and save!

TUESDAY, SEPTEMBER 11

TIME	TITLE	SPEAKER	CATEGORY
8:00am CONFERENCE COFFEE BREAK, *Sponsored by Sierra Circuits*			
8:30am - 12:00pm	1: PCB Design Strategy for High Density BGA and CSP Components	Vern Solberg, Solberg Technical Consulting	DfF/DfM/DfA/DfT
9:00am - 11:00am	2: Layout of Switch Mode Power Supplies	Rick Hartley, RHartley Enterprises	EMI/EMC/PCB Design
	3: Power Distribution Made Easy	Daniel Beeker, NXP Semiconductor	PCB Design/Layout/ Placement
9:00am - 5:00pm	4: The Basics of PCB Design	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
	5: What's New in the IPC Design Standards, and How to Use Them	Gary Ferrari, FTG Circuits	PCB Design/Layout/ Placement/Standards
	6: PCB Stackup Design and Materials Selection	Bill Hargin, Z-zero	PCB Design
	7: Troubleshooting and Defect Resolution of SMT Assembly Processes	Jim Hall and Phil Zarrow, ITM Consulting	SMT/Electronics Assembly
11:00am - 12:00pm	8: Managing Your Impedance, Coupling and Return Paths in Design and Avoid Unnecessary Iterations with SI/PI Engineers	Dennis Nagle, Cadence Design Systems	High Speed
	9: Evaluating an Appropriate Power Plane through Power Integrity Simulation	Richard Villamor Legaspino, Analog Devices	Power Integrity
	10: PCB Library Development and Management – A Treatise	Vijayakumar David, Tessolve Semiconductor	Libraries
12:00pm – 1:00pm LUNCH-N-LEARN, *Sponsored by Streamline Circuits (Tuesday conference attendees only)*			
1:00pm - 3:00pm	11: Power Integrity & Decoupling Primer for PCB Designers	Ralf Bruening, Zuken	SI/PI
	12: Laying Out Analog/Digital Planes	Robert Hanson, Americom	SI/PI
1:00pm - 4:30pm	13: Effective PCB Design: Techniques to Improve Performance	Daniel Beeker, NXP Semiconductor	PCB Design/Layout/ Placement
	14: Circuit Grounding to Control Noise and EMI	Rick Hartley, RHartley Enterprises	EMI/EMC & PCB Design
3:00pm - 5:00pm	15: Thermal Integrity within an Electrical Design Flow	Jim DeLap, Ansys	PCB Design/Layout/ Placement
	16: How to Fight Magnetic Noise Gremlins	Keven Coates, Geospace	EMI/EMC

WEDNESDAY, SEPTEMBER 12

8:00am CONFERENCE COFFEE BREAK, *Sponsored by Sierra Circuits*			
8:30am - 12:00pm	17: The Complexities of Fine Pitch BGA Design	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
9:00am - 10:00am	18: PCB Reverse Engineering Countermeasures	Jeremy Hong, Hong's Electronics	PCB Design/Layout/ Placement
9:00am - 11:00am	19: Multi-Board Design: Castellation, Connection, SI, Alignment	Ben Jordan, Altium	PCB Design/Layout/ Placement
	20: An Intuitive Approach to Understanding Basic High-speed Layout	Keven Coates, Geospace	SI/PI
	21: A Beginner's Introduction to PCB Trace Impedance	Ken Taylor, Polar Instruments	PCB Design
9:00am - 5:00pm	22: Cost Reduction through Design for Manufacturing and Assembly	Gary Ferrari, FTG Circuits	DfF/DfM/DfA/DfT
	23: The Complete Guide to Understanding Transmission Lines	Robert Hanson, Americom	High Speed
10:00am – 6:00pm EXHIBITION FLOOR OPEN			
10:00am – 2:00pm EXHIBIT HALL BOOTH BARISTA, *Sponsored by Zuken*			
10:00am - 12:00pm	24: iPhone X – Steve Jobs' iPhone	Bill Cardoso, Creative Electron	PCB Design/Layout/ Placement
11:00am - 12:00pm	25: Continuing Test Point Management throughout a PCB Design Flow	Mark Laing, Mentor	PCB Design/Layout/ Placement
	26: Clock Jitter Behavior on Different PCB Layout Approach	Marcus Miguel Villaflores Vicedo, Analog Devices	PCB Design/Layout/ Placement
	27: ECAD-MCAD Co-design for a Competitive Advantage	John McMillan, Mentor	PCB Design/Layout/ Placement
12:00pm – 1:00pm LUNCH ON EXHIBIT FLOOR, *Sponsored by Sierra Circuits*			
1:00pm - 3:00pm	28: Thermal Design Considerations for SMD PCBs	Keven Coates, Geospace	PCB Design/Layout/ Placement
	29: Signal Attenuation in Very High Speed Circuits	Rick Hartley, RHartley Enterprises	High Speed/PCB Design
1:00pm - 4:30pm	30: HDI Routing Solutions	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
	31: The Basics of PCB Fabrication (101)	Paul Cooke, FTG Circuits	Fabrication
3:00pm - 5:00pm	32: Differential Pair Routing for SI Control	Rick Hartley, RHartley Enterprises	High Speed/PCB Design
	33: Evaluating the VIA Transition through TDR Simulation	Richard Villamor Legaspino, Analog Devices	RF/Microwave/PCB Design

PCB WEST Schedule-at-a-Glance

TIME	TITLE	SPEAKER	CATAGORY
FREE WEDNESDAY, SEPTEMBER 12			
9:00am - 11:00am	F1: Routing & Termination for Control of Signal Integrity	Rick Hartley, RHartley Enterprises	High Speed/PCB Design
9:00am - 10:00am	F2: HDI: High Density Interconnect	Chris Nuttall, NCAB Group	PCB Design/ Fabrication
10:00am - 11:00am	F3: AI and Machine Learning Disrupting the Manufacturing of Your Products	Albert Yanez, AsteelFlash	Automation/Process Improvement
11:00am - 12:00pm	**KEYNOTE: Is Past Prologue? The Future of the PCB Design Industry - Walden Rhines, CEO, Mentor**		
	F4: Designing in the Age of Prototypes	Milan Shah, Royal Circuits	PCB Design
1:00pm - 2:00pm	F5: Industry 4.0 and IPC-2581	Hemant Shah, IPC-2581 Consortium	Electronics Data Transfer/Standards
1:00pm - 3:00pm	F6: The 10+ 21 Most Common Design Errors Caught by Fabrication (and How to Prevent Them)	David Hoover, TTM Technologies and Ray Fugitt, DownStream Technologies	DfF/DfM/DfA/DfT
2:00pm - 3:00pm	F7: Efficient PCB Interposer Design Using a Novel Smart Router Based on Neural Networks and Genetic Algorithms	Xiao Ming Gao, Intel	PCB Design
3:00pm - 4:00pm	F8: Optimizing Hardware for Your IoT Solution	Sean Priddy, Creation Technologies	Business/Markets
	F9: PANEL: The Future of PCB Engineers	Phil Marcoux, PPM, Moderator	3D Printing/ Fabrication
4:00pm - 5:00pm	F10: 3D Printed Electronics: A New Dimension in Prototyping & Manufacturing	Simon Fried, Nano Dimension	Printed Electronics
	F11: PANEL: Understanding the AS9100D Standard	Peter Bigelow, IMI, Moderator	Standards
CAD TOOL CORNER – FREE – WEDNESDAY, SEPTEMBER 12			
1:00pm - 2:00pm	C1: Ensure Your Electronic Design is Reliable and Robust by Simulation – During Schematic, Before Manufacturing and Testing	Yizhak Bot, BQR	PCB Design
2:00pm - 3:00pm	C2: Retargeting Your Libraries for Newer, Better Processes without Breaking Your Bank	Vince Di Lello, Cadence Design Systems	PCB Design/Layout/ Placement
3:00pm - 4:00pm	C3: Designing PCBs in the Context of a System	Gary Hinde, Cadence Design Systems	PCB Design
4:00pm - 5:00pm	C4: Multi-Domain Collaboration for Electronics Systems Design	David Wiens, Mentor	PCB Design
5:00 pm – 6:00 pm EVENING RECEPTION, *Sponsored by Ultra Librarian*			
THURSDAY, SEPTEMBER 13			
8:00am CONFERENCE COFFEE BREAK, *Sponsored by Sierra Circuits*			
8:30am - 12:00pm	34: Design of Power Distribution and Decoupling	Rick Hartley, RHartley Enterprises	EMI/EMC & SI/PI & PCB Design
	35: Part Placement Choices and Consequences	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
9:00am - 10:00am	36: Intelligent DfM for Assembly	Kevin Webb, Mentor	PCB Design/Layout/ Placement
	37: Providing Solutions for Thermal Management within RF Designs	James Barry, PCB Technologies	RF/Microwave/ Thermal Management
9:00am - 11:00am	38: The Mystery of Bypass Capacitors	Keven Coates, Geospace	SI/PI
	39: Ask the Flexperts – Flexible Circuit Design through Test with Lessons Learned	Mark Finstad, Flex Circuit Technologies, and Nick Koop, TTM Technologies	PCB Design & Fabrication Processes
9:00am - 12:00pm	40: Designing Embedded Passives and Related Technologies	Gary Ferrari, FTG Circuits	Embedded Passives/ Fabrication/ Components
10:00am - 11:00pm	41: DfM: Getting It Right from the Start	Chris Nuttall, NCAB Group	DfF/DfM/DfA/DfT
	42: Arriving at an Optimal Stackup for Printed Circuit Boards Used in Silicon Validation	Vijay Nanjai Anandan, Tessolve Semiconductor	Fabrication
11:00am - 12:00pm	43: Leveraging 3-D Layout to Optimize Rigid-Flex Designs	John McMillan, Mentor	PCB Design/Layout/ Placement
	44: Overview of Several RF Structures and How They Work	John Coonrod, Rogers	RF/Microwave/PCB Design
12:00 pm – 1:00 pm LUNCH-N-LEARN, *Sponsored by Polar Instruments (Thursday conference attendees only)*			
1:00pm - 3:00pm	45: Electromagnetic Fields for Normal Folks: Show Me the Pictures and Hold the Equations, Please!	Daniel Beeker, NXP Semiconductor	EMI/EMC
1:00pm - 4:30pm	46: Flexible and Rigid-Flex Circuit Design and Assembly Process Principles	Vern Solberg, Solberg Technical Consulting	DfF/DfM/DfA/DfT
	47: Best DfM Practices for Board Engineers	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
	48: RF and Mixed Signal Board Design	Rick Hartley, RHartley Enterprises	RF/Microwave/PCB Design
3:00pm - 5:00pm	49: PCB Design Techniques to Improve ESD Robustness	Daniel Beeker, NXP Semiconductor	EMI/EMC

PCB WEST 2018
Conference & Exhibition

WHO'S EXHIBITING

Accurate Circuit Engineering
Accutrace, Inc.
Aculon, Inc.
Advanced Circuits
Akrometrix, LLC
All Flex Flexible Circuits & Heaters
ALL-4 PCB (North America) Inc.
American Standard Circuits, Inc.
APCT
Asteelflash
Autodesk EAGLE
Bay Area Circuits, Inc.
Beta LAYOUT
Bittele Electronics Inc.
Bowman XRF
Cadence Design Systems
Cicor Group
CML USA Corp.
CMR Summit Technologies
Cofan USA Inc.
Creation Technologies
dalTools
Dino-Lite Scopes (Big C)
Dow Electronic Materials
DownStream Technologies, Inc.
DYCONEX AG
Dynamic Electronics Co., Ltd.
EM Solutions Inc.
EMA Design Automation
Firan Technology Group – FTG Circuits
Fischer Technology, Inc.
Flex Interconnect Technologies
Freedom CAD Services, Inc.
Frontline PCB Solutions
GreenSource Fabrication LLC
GS Swiss PCB AG
Han's Laser Corp.
Hawk Ridge Systems
Henkel Electronic Materials
HSIO Technologies
ICAPE Group
Insulectro
Integrated Packaging Films, Inc.
IPC-2581 Consortium
Javad EMS Inc.
JetPCB Web LLC
Kyocera International, Inc.
Leader Tech, Inc.
Mentor, A Siemens Business
MFS Technology (S) Pte Ltd
MicroConnex
Milestone Technology
Mitsui Chemicals America, Inc.
Multek Interconnect Solutions
MVINIX Corporation
NCAB Group USA
NexLogic Tech., Inc.
Numerical Innovations
Oak-Mitsui Technologies
Ohmega Technologies, Inc.
One Diamond Electronics Inc.
Optimum Design Associates
PackageWright
Panasonic Electronic Materials
Park Electrochemical Corp.
Polar Instruments, Inc.
Polliwog Corporation
Printed Circuits
Pulsonix PCB Design Software
Q & D Circuits Co. Ltd.
Qdos Technology Sdn Bhd
Quadcept
Risho
Rogers Corporation
Royal Circuits
San Diego PCB Design
San-ei Kagaku Co., Ltd.
Sanmina Corporation
Screaming Circuits
Shenzhen Danyu Electronics Co. Ltd.
Shenzhen Huixin Circuit Technology Co., Ltd.
Shenzhen Kinwong Electronic Co., Ltd.
Sierra Circuits, Inc.
SOMACIS
Streamline Circuits
Summit Interconnect
Sunshine Global Circuits
Sunstone Circuits
SVTronics, Inc.
Taconic
Tempo Automation
Tessolve
Ticer Technologies
TopLine
TTM Technologies, Inc.
Ultra Librarian
Varioprint AG
Ventec International Group
Victory Giant Technology (Huizhou) Co., Ltd.
Wurth Electronics
Zero Defects International
Zuken USA Inc.

Manage HIGH-CURRENT TRACES by Thinking Outside the Box

Stop thinking such traces must be a certain width!

by DOUGLAS BROOKS, PH.D., DR. JOHANNES ADAM and NITIN BHAGWATH

Au: The general ideas and concepts presented in this paper were first suggested by Nitin Bhagwath in 2017 and presented in a paper at DesignCon in 2018.[1]

When we start a new board design, we need to meet several objectives. Some of the most obvious are:

- Certain physical constraints must be met (board outline, certain component locations, etc.)
- Point-to-point connection requirements specified in the netlist must be met.

When we start actually routing traces, in broad general terms we work within two paradigms. For now, we will call them "signal" (or i*R), and "power" (or i^2*R). The first probably applies to more than 99% of traces. This paradigm relates to how we maintain a clean enough signal so that the system will operate. At a minimum we want to ensure there is not so much voltage drop along the net to cause signal loss and system instability.

We do this by ensuring the resistance of the trace is low enough, and we do that by ensuring the cross-sectional area of the trace is large enough to meet our needs. In the vast majority of cases, the manufacturing limitations are such that the trace is almost always large enough, meeting this requirement inherently. But as systems get more sophisticated, we need to worry about other things:

1. Controlling the loop area to control EMI and crosstalk.
2. Controlling trace impedance to control reflections.
3. Placement of components like bypass caps, and
4. Minimizing pad inductance for good power distribution control.
5. Dealing with the skin effect and dielectric losses.

Sometimes we even need to worry about via location, impedance and length. As an industry, we now have a lot of information and guidelines regarding how to work within this paradigm.[2]

Things are a little different when we start dealing with the second paradigm. Here we worry about whether the current level in the trace generates enough power along the trace, and therefore enough heat along the trace, and therefore enough of a rise in temperature, to cause a thermal issue on the board. The power comes from the i^2R drop along the trace. Most designers, if working within this paradigm, have one solution: make the cross-sectional area of the trace big enough to lower the resistance low enough to handle the current. And the only place they know to get the answer to how large the trace should be is in the data summarized in IPC-2152.[3]

This is unfortunate. As Brooks and Adam have shown,[4] the IPC data are almost always worst case. That is, almost anything we do to a trace from a practical standpoint lowers the temperature of the trace. This area is very complex, and it is very hard to make generalizations because almost all examples are case-specific. But in the examples Brooks and Adam look at in their book[5]:

1. Reducing the length of a trace can lower the change in temperature by perhaps 20%.
2. Adding a parallel trace can lower the change in temperature by perhaps 14%.
3. Placing a plane on the opposite side of the board can lower the change in temperature by perhaps 30%.
4. And placing a plane on the layer directly under the trace can lower the change in temperature by up to 50%.

As a result, many designers use larger traces than required, using up valuable real estate. But the examples above only touch a fraction of the opportunities that might be available to designers. In this article we will suggest that thinking outside the box may allow many designers to achieve their thermal objectives much more efficiently than ever before. We may be able to add non-current-carrying copper areas and trace segments, not for signal reasons, but for thermal reasons.

Caution: Some designers, in initial discussions about this topic, immediately dismiss the concepts presented herein as being impractical because a) the designers think they don't have enough real estate on the board to implement them, or b) they think the ideas are inconsistent with their perceived signal integrity needs. This is a mistake! It is very rare for the same trace to be subject to both paradigms (signal and thermal) suggested above at the same time. And thermal issues can often be confined to areas of a board where real estate requirements can be a little more flexible.

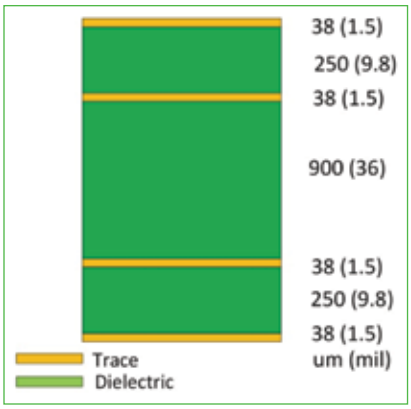


FIGURE 1. Stackup of test board (not to scale).

A trace heats by i^2R. The primary cooling mechanism for a trace is conduction (heat spreading) into and through the board material (dielectric) before heat ejection from the board through convection and radiation. Anything that increases the efficiency of the thermal conduction lowers the temperature. That is why, for two traces with the same cross-sectional area carrying the same current, the thinner, wider trace will have a lower temperature. That is why a copper plane directly under the trace lowers the trace temperature.

What we are advocating here is that, first of all, designers stop thinking about high-current-carrying traces as being a certain width. We tend to look at the IPC-2152 tables and think, "Okay, my trace needs to be x mils wide." No, it can vary in width. And if we vary the width, then the wider sections can draw heat away from the narrower sections. Second, we advocate that designers consider various ways to add copper surface area to their designs in such a way as to conduct heat away from traces. Adding a plane under the trace is one obvious way to do that. There may be other ways we can approach this.

In the rest of this article, we will offer suggestions of ways to think about these options. But, there is an infinite number of ways we can do this. Every example here can be implemented any number of ways, with any number of shapes and dimensions. There is no one answer. In fact, it is really hard to even make generalizations, although we will try to offer some insights. At the end of the article we will offer suggestions on how a designer can proceed.

Test Board

In the examples below, we will assume a standard test board 220mm long by 20mm wide (8.7" x 0.8"). Its thickness will be 1.55mm (approx. 61 mils), including 38µm (1.0 oz.) trace layers top and bottom. A stackup is provided in **FIGURE 1**. The standard (reference) trace on the board's top layer will be approximately 150mm (6.0") long by 1.0mm (40 mils) wide. The board dielectric material will be polyimide. We will apply 4A of current through the trace. We will simulate our examples and calculate temperatures using a simulation program called Thermal Risk Management (TRM).[6] The temperature of the simple trace, with no adjacent traces or planes and with no supplemental cooling, rose from an ambient of 20°C to 53.2°C, or a change of 33.2°C.

Example 1: Copper under the trace.

Adding copper under the trace will help conduct heat away from the trace, lowering the trace temperature. We looked at five configurations, summarized in **TABLE 1** and in **FIGURE 2**. These included:

- The trace with no supplemental cooling.
- Placing a trace the same width on the trace layer under the trace.
- Placing a trace three times wider than the trace (120 mils) on the trace layer under the trace.

TABLE 1. Basic Data

	CASE	TEMPERATURE	DELTA T	% DELTA T IMPROVEMENT
A	Simple trace	53.2	33.2	0
B	Narrow trace under	52.95	32.95	0.8
C	Wider trace under	49.2	29.2	12
D	Full plane, bottom	44.8	24.8	25.3
E	Full plane, under	39.5	19.5	41.3

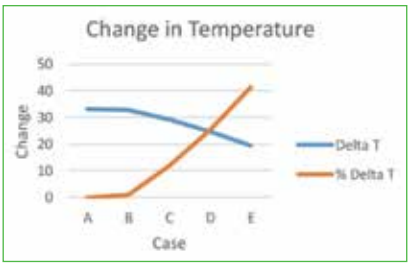


FIGURE 2. Change in temperature data from Table 1.

- Placing a full copper plane on the bottom trace layer.
- Placing a full plane on the trace layer under the trace.

Discussion. Two conclusions are intuitive. The more copper we can place under a trace, the more heat is conducted away from the trace, and the cooler the trace temperature will be. The closer the copper is to the trace, the more heat is conducted away from the trace, and the cooler the trace temperature will be. The more heat that is conducted away from the trace, the smaller the trace can be and still carry the target amount of current. So, look for ways to add copper underneath the trace.

It should be noted a copper area used specifically for cooling carries no current whatsoever. And even if there is some small amount of noise signal coupled to it from the power trace, that coupled current should be harmless. If there is any concern at all about a coupled current, simply tie the copper area to the system reference (ground) with a *single* via.

From a thermal standpoint, any underlying plane works like any other plane. The underlying plane does not have to be a "continuous and related" plane in the sense we need that for the signal paradigm (signal integrity.) However, a systems engineer needs to determine whether any noise on the high-current-carrying trace might couple into any underlying, unrelated (and sensitive) plane.

Adding vias (i.e., "thermal" via) connecting traces to planes in any of these configurations resulted in trivial (if any) improvement. As we have shown in our book, traces can cool vias, but not the other way around. Vias do not cool traces.[7] On the other hand, any vias that might be penetrating the planes

from other nets are inconsequential. They have a minimal impact on the cooling area of the total plane.

Example 2: Adding additional copper to traces. It is not necessary for a high-current-carrying trace to be constant width. There may be opportunities to change the width as the trace routes across the board. For this example we added nine "stubs" or pads, equally spaced along the trace. The stubs increased the width of the trace from 1.0mm to 5.0mm at each point. They were spaced 15mm apart. FIGURE 3 is an illustration from the simulation output showing the configuration.

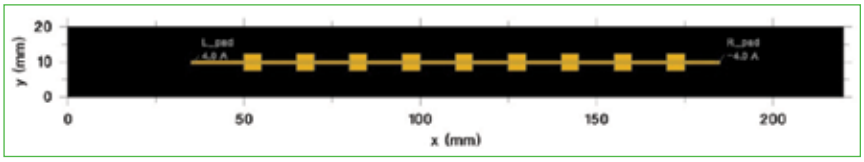


FIGURE 3. Trace with distributed "stubs" along its length.

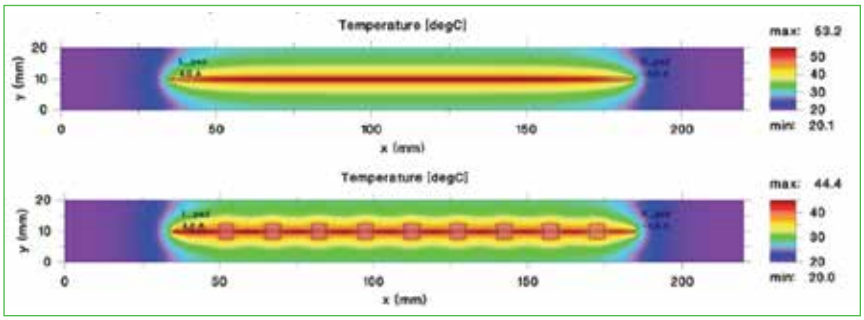


FIGURE 4. Thermal profiles showing the simple trace and a trace with numerous stubs along its length.

With just a simple trace, the maximum trace temperature was 53.2°C. Adding the distributed stubs lowered the peak temperature to 44.4°C. The corresponding changes in temperature were 33.2°C and 24.4°C, respectively, an improvement of 26.5%. This means we could, for example, decrease the width of the standard trace without exceeding our maximum allowable trace temperature. The thermal profiles of the two cases are shown in FIGURE 4.

Discussion. If we do not constrain ourselves thinking that high-current-carrying traces should be a constant width, we open up all kinds of opportunities to change the width to help conduct away heat. So if, for example, we calculate a trace 40 mils wide is needed to carry the current, we may be able to reduce that width in some areas of the board, while increasing it in others without increasing the maximum tolerable trace temperature.

The largest part of the current is carried along the line of the trace. There is a little current fringing into the stub, but not very much. FIGURE 5 shows the current density along a portion of the trace.

Example 3: Dealing with connecting links. In a recent article, we discussed how short, narrow connecting links along high-current-carrying traces are not as troublesome as some might think.[8] The main trace acts as a heatsink for the link, conducting a significant part of the heat away from the link, helping to lower the temperature of the link. In this example we will look at three link configurations (FIGURE 6):

A. A single, short, 3-mils long, 11-mils wide connecting link between two sections of the test trace. Such a link may be required if we have to bring the primary trace near some components that restrict the area around the trace. This link looks a lot like a fuse!
B. The addition of a second link using a nearby path.
C. The addition of a small, supplemental area of copper (partial plane) directly underneath a single link. This copper area is 40mm long by 6mm wide (1.6" x 0.25").

The results of these simulations are shown in TABLE 2. A single, 11-mils wide trace, by itself, carrying 4.0A would heat to well over 150°C. But because of the heat-sinking influence of the basic trace, the trace temperature doesn't rise nearly that much. But it does increase, perhaps to intolerable levels. If we put a small plane under it, the temperature only increases about 13%. Adding a parallel second link, the

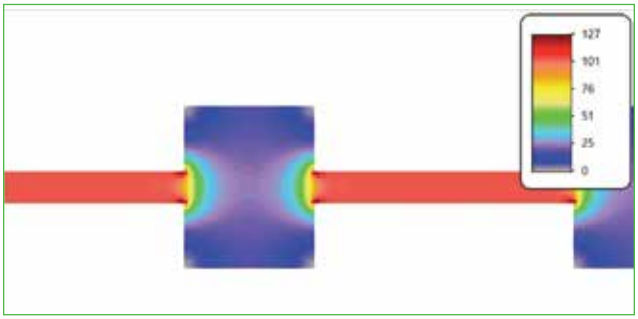


FIGURE 5. Current density along trace (units are A/mm^2).

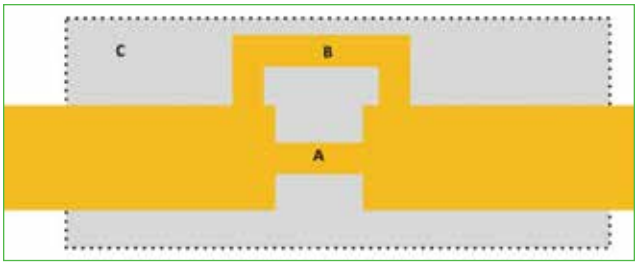


FIGURE 6. Three link configurations (not to scale).

TABLE 2. Example 3 Data

CASE	TEMPERATURE	DELTA T
Basic trace	53.2	33.2
Single link, A	74.6	54.6
Single link + Plane C	60	40
Second link B	59.3	39.3

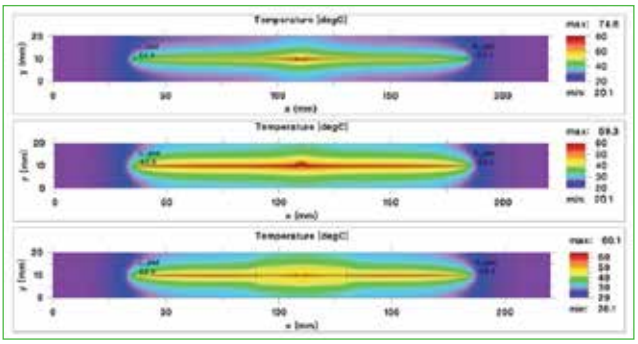


FIGURE 7. Thermal profiles of the three cases.

benefit is about the same as adding an underlying plane. The thermal profiles of the three cases are shown in FIGURE 7.

Discussion. If we are constrained in our thinking that high-current-carrying traces must be a certain width, and then we run into a constricted area on the board, it would seem we had few, if any, options. But if we relax that restriction, several opportunities may present themselves. It certainly may be possible that a second (albeit narrow) adjacent path (or even more) might be available. This would allow spreading out the heat-generating area of the trace over a wider area, helping to control the trace temperature.

The "plane" area under the link area doesn't necessarily need to be continuous. In fact, it need not even be a single area. There might be an opportunity to spread copper around the layer between other traces. And any via paths that might exist through the "plane" are almost inconsequential as far as the heat-spreading ability of the copper is concerned.

Conclusions

When we start worrying about signal integrity issues in PCB design, we start worrying about *rules*: loop area must be minimized; trace impedance must be constant; pad impedance must be minimized, etc. We are now advocating that when designing high-current-carrying traces we forget the rules (i.e., the trace must be a minimum size). Instead, start thinking outside the box. Think how can I lower the trace temperature in ways other than just increasing its cross-sectional area? As a start, we can add (non-current-carrying) copper areas near and under the trace to help conduct heat away. We can design traces with wider widths where there's room and narrower widths where there's not. The wider areas will help sink some of the heat away from the narrower areas. In this way we will achieve much more flexibility in our layouts, especially in tight areas.

How to evaluate design alternatives. The good news from all this is there may be some really significant options available if we look. The bad news is it is really difficult to evaluate them! In the mid '90s our industry first began looking at controlled impedance traces in a significant number of designs. We needed to know how to calculate trace impedance and how to calculate trace parameters to meet a target impedance. Back then we had formulas published by various trade associations and manufacturers. Today we know these formulas are not accurate enough. We now say we need "field effect" solutions to meet our requirements, computer programs that use matrix algebra to solve a large number of simultaneous equations, resulting in the solutions we need.

When it comes to thermal design, we have relied on the charts published by IPC for a long time. But the problem is much more complicated than simply adding the thermal resistance and local heating of individual traces. We now need the same types of computer programs as needed for impedance: programs that use matrix algebra to solve a large number of simultaneous equations, resulting in the solutions we need. The equations are different, but the process is the same. In general, this category of program is called "thermal simulation." And as systems get more complex, we will need these programs at both the board level and the systems level. PCD&F

NOTES

1. Nitin Bhagwath, Doug Brooks, Robin Bornoff, Praveen Anmula, Joseph Aday, Robert Carter, and Patrick Carrier, "Non-Conventional Approaches for Maximizing Current Capacity of a PDN," DesignCon, January 2018.
2. Douglas G. Brooks, Ph.D., *PCB Currents; How They Flow, How They React*, Prentice Hall, 2017.
3. IPC-2152, "Standard for Determining Current Carrying Capacity in Printed Board Design," August, 2009, IPC. This is an update of the charts that appeared in IPC-2221, which themselves traced back to National Bureau of Standards Report #4283, published in 1956.
4. Douglas G. Brooks, Ph.D., and Dr. Johannes Adam, *PCB Trace and Via Temperatures: The Complete Analysis*, 2nd Edition. See also Johannes Adam's earlier paper, "New Correlations Between Electrical Current and Temperature Rise in PCB Traces," Proc. 20th IEEE SEMI-THERM Symposium, 2004.
5. Brooks and Adam, Section 6.3 and especially Table 6.5, p. 70.
6. TRM (Thermal Risk Management) is designed to analyze temperatures across a circuit board, taking into consideration the complete trace layout with optional Joule heating, as well as various components and their own contributions to heat generation. Learn more about TRM at www.adam-research.com. Examples of how to use TRM are in Brooks and Adam, Chapter 6.
7. Brooks and Adam, Chapters 7 and 8.
8. Douglas Brooks, Ph.D. and Dr. Johannes Adam, "More on Via Temperatures," PCD&F, June 2018.

DOUGLAS BROOKS, PH.D., is president of UltraCAD Design, a PCB design service bureau and author of three books, including *PCB Trace and Via Currents and Temperatures: The Complete Analysis,* 2nd edition (with **JOHANNES ADAM**) and *PCB Currents: How They Flow, How They React*; doug@ultracad.com. **NITIN BHAGWATH** is a product architect at Mentor (mentor.com); nitin.bhagwath@mentor.com.

Why Zestron Wants to 'CLEAN UP' in Asia

With its new technical centers in Taiwan and Japan, the electronics cleaning company is going local and changing cultures. by CHELSEY DRYSDALE

Asia knows how to throw a party.

Upon exiting the bus at Zestron's inauguration ceremony for its first ever technical center in Taiwan last month, we were met with multiple cameras. Hsinchu employees, local press and native dancers flanked a red carpet leading into the sleek building. They'd been eagerly awaiting the company's management team. For Zestron's customers, however, the ceremony is secondary to what comes next.

In mid-May, Zestron inaugurated two new technical centers: one in Hsinchu, Taiwan, and the other in Samukawa, Kanagawa, Japan. That brings the number of technical centers the company now boasts to eight, including labs in Germany, Malaysia, the US, Korea, and two in China. Zestron's technical centers correspond with each of its headquarter hubs.

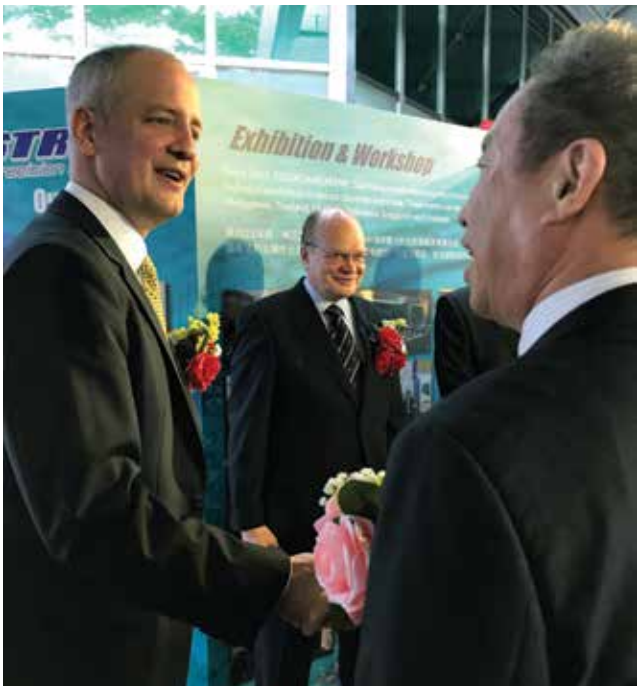


FIGURE 1. Zestron president Harald Wack greets Jack Ma, president of Everteam, at the opening of the Taiwan site, as John Zarno, Zestron's chairman of the board, looks on.

Harald Wack, Ph.D., president of Zestron, called Taiwan a "flourishing business environment" in his opening remarks, part of which he gave in Chinese, a language he says he's been diligently learning over the past two years. His personal efforts are a microcosm of the company's commitment to winning over customers in South Asia.

"This is an important company milestone," he said. He promised the Hsinchu community Zestron would go "beyond expectations," with a "commitment to personalized, professional customer service (and the) highest product quality."

Wack said the opening is the culmination of a decade-long presence in Taiwan. He thanked James Yeoh, the firm's executive director of South Asia, saying, "You've provided the reason we're here today."

The initial scale is small, with three staff members currently working in Hsinchu. Nevertheless, the company expects the local team to "multiply," and is banking on its growth. Asia is the "future leader" for company growth, Wack said, adding, "We would like to become more Asian every day."

FIGURE 2. The Taiwan tech center is outfitted with cleaners that are typical of the local market.

Listening to Locals

Zestron is putting its money where its mouth is. Some 70% of its current global investment is in Asia. Recently, it started R&D in Malaysia, with two Ph.D. chemists there who work directly with customers. "We are automatically learning more about Asian requirements" and are open and adapting to it, Wack said.

While Zestron is "listening to more local customers," Wack is quick to note the company is "not *only* Asian." The Ingolstadt, Germany-based firm is well-established in the US, and "that won't go away. It's a good mix of everything."

Zestron prides itself on being a leader in research and development in electronics assembly process cleaning. Spreading itself across a wider breadth of the globe brings unique challenges for its lab workers. Because its customers are multi-regional, Zestron conducts multi-regional studies, including a current semiconductor study to prepare substrates. One of the firm's customers is the leading semiconductor company in Asia, among other giant global names in the electronics industry with whom it works. Zestron conducts multiple engineering meetings each year, and task groups are formed across global campuses to perform studies for certain accounts.

While standard products work with the majority of customers," when necessary, Zestron formulates special products, especially for large customers.

"R&D is everywhere for us," Wack said. R&D "regularly communicates as much as the engineers do," he added, citing a video conferencing system where as many six people communicate face-to-face. "We are very well connected.

"The tech centers come across problems," he explained. "The next step is the engineer engages with R&D. It becomes a multi-departmental effort to satisfy the customer."

At a press conference inside the Hsinchu lab, Wack provided the impetus for the facility, which is contained on one level of the building. He stressed the importance of being local, which gives engineers the chance to see the effects of flux residue and other contaminants for themselves up close. "It allows local customers to come here to see our products are better." The site "shows how clean an assembly has to be."

The goal is to show customers the advantage of automation. "Results are becoming a lot more consistent," he said. "We recommend automated cleaning" because it provides more long-term reliability.

The newly inaugurated sites contain inline and spray-in-air machines from local manufacturers. Both Hsinchu and Japan feature the Kedtech S300 and include office space and an analytics lab, where they've integrated the Zestron Eye digital monitoring system for measuring and controlling cleaning bath concentration.

New Markets

"One of the reasons we are in Taiwan and Korea is the semi markets," Wack said. "Taiwan, Korea and Japan are very semiconductor heavy. We don't have those kinds of ovens everywhere."

Currently, about 30% of Zestron's business is semiconductor, with 70% SMT, but in the next five to 10 years Wack expects that number to be closer to 50/50. "It will be harder to differentiate between the two at some point," he said.

He emphasized the environmentally friendly nature of Zestron's water-based products, as the industry's traditional use of solvents is outdated.

"Solvents are difficult to remove and dispose [of]. In the last 25 years, part of our success has been in R&D. We have been able to change to a water-based product. Our products are pH neutral and fully biodegradable. A little concentrate. The rest is water."

Wack called the formula the "closest we can come to pure water. We are about 10 years ahead of the competition. No one else comes close."

That said, the decision to clean remains a hurdle for many. Generally, it is driven by quality issues, especially as boards get smaller and more prone to failures due to residues. "Not every customer wants to clean, so companies that decide to clean have to do so because of product quality," Wack added. "If they don't clean, they'll have product failures in the field. Once you have rejects, it creates more work than you can imagine.

"Miniaturization gets more important. It is becoming more difficult to clean under components." This is a trend "every cleaning company is facing." It is "probably one of the biggest challenges."

Wack and his staff welcome the opportunity to sit down with customers to determine their challenges and how to solve them. "Being physically present is important. We see infrastructure as a unique advantage."

He said the Hsinchu tech center will grow, and will eventually need a bigger space, like with locations opened earlier.

A New Culture in Japan

In a more formal, equally impressive setting, Japan brought out the white gloves for the Samukawa event.

FIGURE 3. Outside the new 10,000 sq. ft. center in Samukawa, Japan, about 54km from Tokyo.

FIGURE 4. The Zestron Eye tool for measuring contamination is a big piece of the company's analytics assessments.

The day included a ribbon-cutting, another press conference, a customary sake barrel breaking, a tour of the immaculate two-story building – not counting rooftop access – and drum lessons by native talent.

The ground floor houses analytical and cleaning labs, including a large, conveyorized inline cleaning machine for water-based products that is said to be atypical for Japan. Manufacturers in Japan typically prefer ultrasonic and solvent cleaning. But according to Wack, Zestron has begun to convince customers to switch.

"We are changing the culture," Wack said. "You can only go to Japan if you have a better mouse trap." The key, he shared, is to be patient and build trust.

In addition to the S-300 inline machine like the one in Taiwan, the site has Fourier-transform infrared spectroscopy (FTIR) to characterize organic residue (Lumos and Alpha II); ion chromatography capabilities, and a Sawa Ecrobid ultrasonic machine that cleans stencils.

Zestron previously rented a facility in Japan for five years. The firm's growing success led to the decision to choose the new location.

Zestron Japan is a 10,000 sq. ft. site, including a warehouse and a large empty space for growth. That compares favorably with the Ingolstadt technical center, which is more than 8,600 sq. ft, with over 30 cleaning machines. In all, Zestron has a total of more than 70 cleaning machines globally. "The new sites are at the same (capability) level as Germany," Wack said.

In Taiwan and Japan, as with their other technical centers, Zestron will use a scanning electron microscope (SEM) and energy dispersive x-ray (EDX) microscope, currently on order. Analytic testing is for inorganic and organic residues.

In a speech to local press, Wack commended Zestron Japan's general manager, Daido Sawairi, whom he met with five years ago to discuss a Japanese presence. "We both felt it was a unique and great time to start in Japan to replace old technology.

"Today is a good beginning to build trust as a new company to Japan. We have invested a lot of money and are confident one day it will be returned," Wack said. "What Daido and team have accomplished in a few years is truly remarkable."

When asked later, Sawairi said the Japan technical center was completed just two days prior to the inauguration. "We made it," he said. The 20-year-old building was overhauled, starting last October.

To the best of Zestron's knowledge, their new Japan home is the biggest industry cleaning center in the country. Within a few years, they expect the staff to grow from five, with up to 10 employees expected soon.

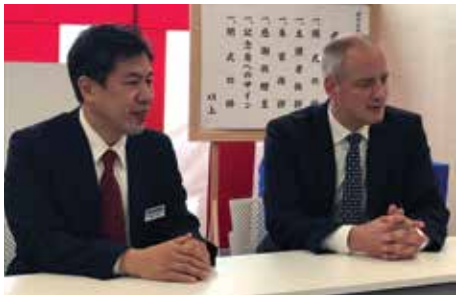


FIGURE 5. Zestron Japan general manager Daido Sawairi and Wack discuss plans for the Japan center.

continued on pg. 39

Stereo with LINE SCAN CAMERAS for High-Resolution 3-D Applications

With passive stereo, there are no limitations in resolution or in the type of illumination. by KLAUS RIEMER, PH.D.

New technologies in production lines bring new requirements for inspection systems. One example for coming 3-D applications in semiconductor industries is inspection of small solder balls or pins used to connect wafers and dies. These components must be inspected with 3-D methods to measure the precise height of the conducting elements.

In general, the objects to be inspected are getting smaller with new technologies. At this time the typical dimensions of such components are around 5µm. Such sizes require high optical resolution of the inspection system, in the range of at least 5µm. Such small metallic objects often have partially reflective surfaces and come with the demand for high-processing speed.

Well-known 3-D approaches with resolutions in that range are triangulation methods and interferometry. There is a tradeoff between resolution and accuracy, on one hand, and processing speed on the other. Interferometry methods provide high resolution and can handle partly specular reflecting surfaces, but are relatively slow. Triangulation methods are quite fast, but slower with higher resolutions, and work best if surface reflectivity is almost diffuse.

Moving in stereo. Stereo is a common approach and widely used in combination with area cameras, e.g., for high-precision object measurements based on special markers. Stereo in combination with line scan cameras is a novel approach providing high speed and very high optical resolution, which opens new possibilities in 3-D inspection. The basic principle is the same as for area cameras: two line sensors in a stereo configuration combined in one camera.

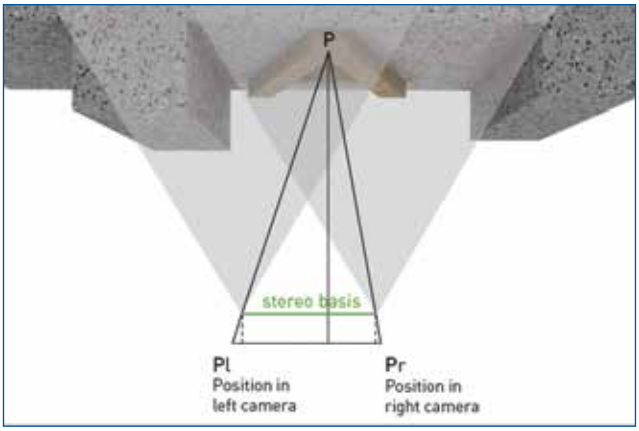


FIGURE 1. The stereo principle: The object point P is projected in both stereo images, denoted as Pr in the right and Pl in the left image. A triangle can be spanned including those three points, which is used for calculate the distance of point P. The stereo basis is the distance of the two optical centers of the stereo cameras.

The stereo concept is to capture two images in a so-called stereo configuration from the same object. Thus, the two stereo images show the same scene from slightly different perspectives and are the basis for triangulation: a triangle can be spanned including the object point and the two corresponding image points. If the positions of the two image points and the camera parameters are known, the distance from the camera to the object point can be calculated from this triangle (**FIGURE 1**).

The preconditions for stereo are:

- Only points of the object surface that are visible in both stereo images can be measured. If an object point is only visible in one image, it can be inspected in 2-D but not in 3-D.
- Finding the corresponding points. The stereo algorithm has to find the right match of the two image points that correspond to the same point on the object surface.

Active illuminations with fringe patterns or random patterns help identify corresponding image points by bringing known texture on even untextured surfaces and enhance the stability of the algorithm. With passive stereo the structure of the object surface itself is used to find the matching points. The latter approach has the advantage that there are no limitations in resolution or in the type of illumination involved by the active illumination.

The precondition for this approach is structures on the surface of the object can be resolved in the image. Two important parameters influence that: the type of illumination and the optical resolution. The

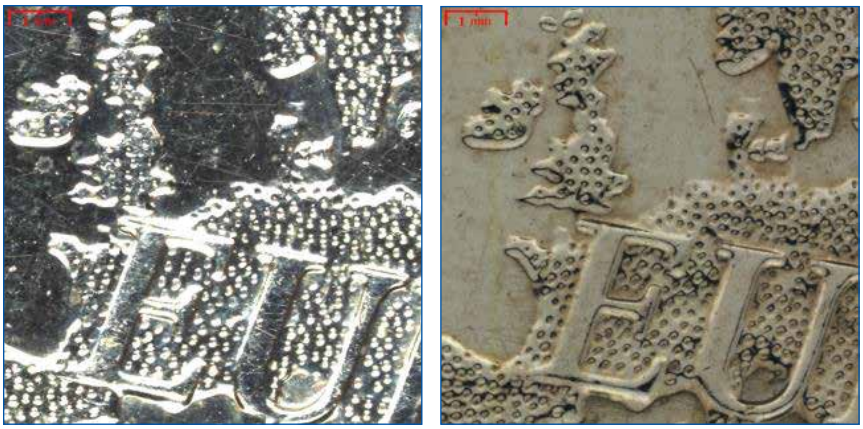


FIGURE 2. The type of illumination is important to reduce shadows and emphasize small surface structures. A Euro coin is shown with dark field (left) and diffuse illumination (right).

illumination can be chosen in a way that fine structures show up with high contrast. The right optical resolution ensures those structures are resolved in the image.

For stereo, a standard approach to find the corresponding image points is based on pattern matching. In doing so, a small area around each point in one image is used as a pattern to be matched with the corresponding stereo image. The best match of the pattern in the corresponding image is defined as the corresponding image point. Doing this for all points (pixels) in the image results in dense 3-D data.

Unique Features of Stereo with Line Scan

The first stereo line scan cameras had optical resolutions of about 50µm, like other well-known 3-D cameras. The typical dark field line scan illumination has been used to provide high-intensity light for high speed. The advantages of those stereo cameras are speed and getting color images in combination with 3-D. Demand for higher optical resolution came next. It turned out that almost all applications requiring high resolution have partly reflective surfaces as well. To provide the right technology for those new requirements, camera makers developed high-resolution stereo cameras and bright diffuse line illuminations. Combining both – the high-resolution stereo cameras and the diffuse tube light – provides a solution for those applications. Those applications clearly show additional unique advantages of stereo cameras based on line scan:

- High resolution: Line sensors provide a large number of pixels; sensors with 7,000 to 16,000 pixels are available. This provides a large field of view (FoV) in combination with a high optical resolution. As an example, with an optical resolution of 5µm, the field of view with 7,000 pixels is 35mm.
- Flexible illumination: With passive stereo, all kinds of illuminations can be used: dark field, bright field, diffuse and co-axial light. The light conditions can be evaluated and optimized for each application. This opens up stereo for partially specular surfaces as is often not feasible with other triangulation methods. For example, FIGURE 2 shows a metal surface illuminated with dark field and with diffuse illumination. The diffuse light reduces shadows and specular reflexes and enhances the fine structures, making it possible to find corresponding points in almost every image area.
- High speed: Depending on the sensor and interface line, frequencies up to 60kHz are available. In the future even faster line sensors with higher speeds will be available. Line sensors with a large FoV and high line frequency allow inspection of a large area in a short time. For example, with 20kHz line frequency and 7,000 pixels, an area of 3,000 mm² can be inspected in one second with a resolution of 5µm. The high-speed acquisition demands for high-speed image processing requiring a lot of processing power. GPUs are primarily used now to achieve the required computational power for stereo processing.
- Fewer occlusions: If the stereo line scan camera is oriented perpendicular to the object surface, there are no occlusions in transport direction. Therefore, the occlusions are reduced in comparison to other stereo or triangulation methods with typical viewing angles of 20° or 30° with respect to the object surface.
- 2-D images in combination with 3-D: Stereo provides two gray or color images from the object, which are available for 2-D image analysis. This is a benefit if, in addition to 3-D, relevant features have to be inspected in 2-D or in color.

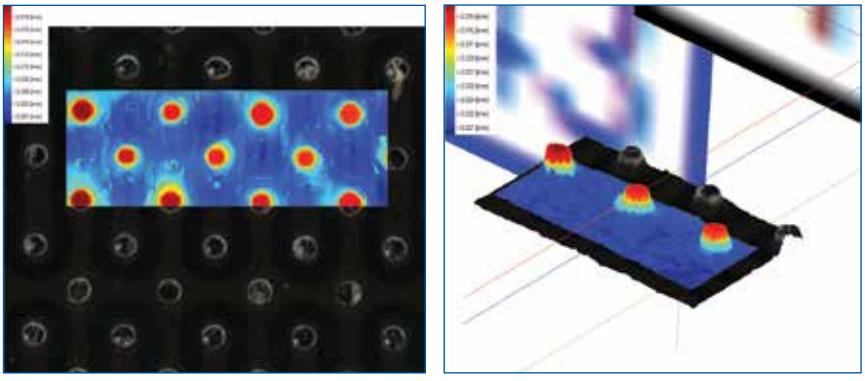


FIGURE 3. At left, a color image with pseudo-color overlay showing small pillars. The diameter of the pillars is 70µm. The pseudo-colors denote the height. Red is closer to the camera. The images are made with a 3-D stereo camera with 2.5µm optical resolution. At right, pseudo 3-D view of a part of the left image.

Application Examples

Typical applications for high-resolution stereo cameras are small objects with metallic surfaces that have to be measured precisely in height.

One application example is to measure the height and shape of small pillars used as connecting elements in semiconductor components (FIGURE 3). By using diffuse illumination, specular reflexes are avoided, and the underlying structure on the surface shows up. The images and height map are shown in Figure 3. Here, a 3-D stereo camera with 2.5µm resolution is used.

Another example is small solder joints on PCBs with partly specular reflecting surfaces (FIGURE 4). (Images are made with the novel 3-DPIXA stereo camera.)

Inspection of wire bonds requires high resolution as well. Even with the reflective surface on the thin wires, the passive stereo approach shows the relevant details in 3-D. The right curvature is important for the functionality and reliability of the product and can be verified with this approach.

Future Challenges

For most applications the stereo algorithms are running on GPUs in the PC. This requires a high-speed data interface to transfer image data from the camera to the PC, making the system quite complex. Running intelligent stereo algorithms fast on embedded hardware will permit calculations to be performed in the camera, which will make the stereo systems smaller, easier to use, and will reduce total system cost. This is an important development step toward wider use of stereo in industrial machine vision.

On the other hand, still-higher optical resolution is necessary as objects get smaller. At higher resolution, the height range becomes limited, since the depth of field is reduced with higher optical magnification. The extension of the height range of line scan stereo with new optical and camera designs will be another challenge for the future. CA

KLAUS RIEMER, PH.D., is 3D product manager at Chromasen's GmbH (chromasens.de); klaus.riemer@chromasens.de.

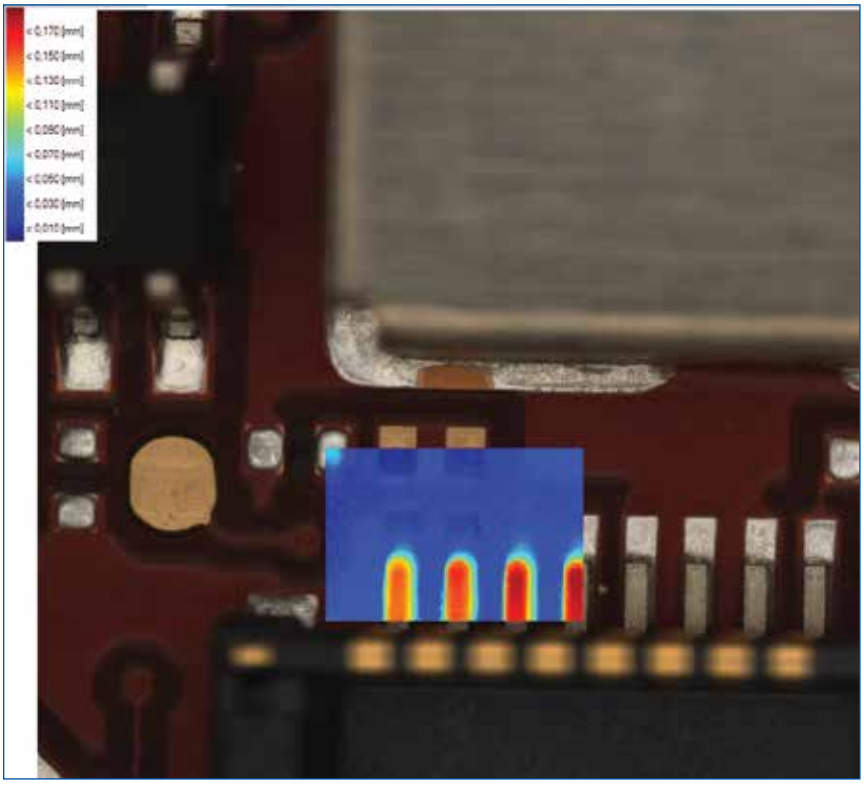


FIGURE 4. Color image with pseudo-color overlay showing solder joints on a PCB. The width of the solder joints is about 50µm. The pseudo-colors denote the height. Red is closer to the camera. The images are made with a 3-D stereo camera with 2.5µm optical resolution.

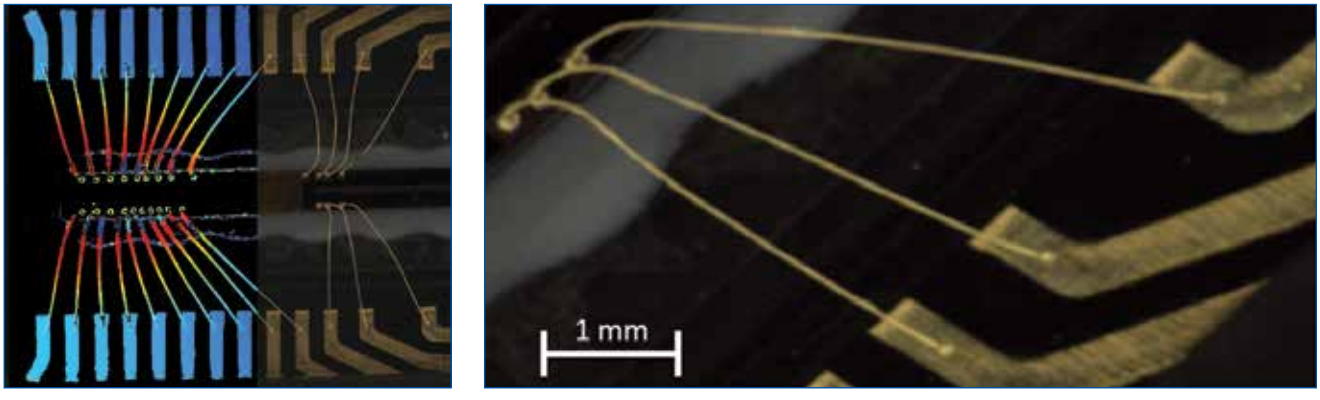


FIGURE 5. At left, a color image with pseudo-color overlay showing wire bonds of an imaging sensor. The width of the wires is about 3µm. The pseudo-colors denote the height. Red is closer to the camera. At right, pseudo 3-D view of a part of the left image.

Gold Peeling

Is it the mask, or is it the gold-plating underneath?

PEELABLE MASKING HAS been used in the past to protect gold key pads during soldering or from solder spitting during reflow, which leads to solder wetting spots on some terminals. This, in turn, may be a cosmetic issue, but also may affect the operation of the contacts.

In FIGURE 1, the peelable coating reflects poor adhesion of the gold to the surface of the pads. This problem is related to the preparation of the contact pads prior to gold or nickel plating and was not related to the assembly process or mask. Testing for gold adhesion using IPC methods showed a total lack of adhesion of the plating.

These are typical defects shown in the National Physical Laboratory's interactive assembly and soldering defects database. The database (http://defectsdatabase.npl.co.uk), available to all this publication's readers, allows engineers to search and view countless defects and solutions, or to submit defects online. To complement the defect of the month, NPL features the Defect Video of the Month, presented online by Bob Willis. This describes over 20 different failure modes, many with video examples of the defect occurring in real time. CA

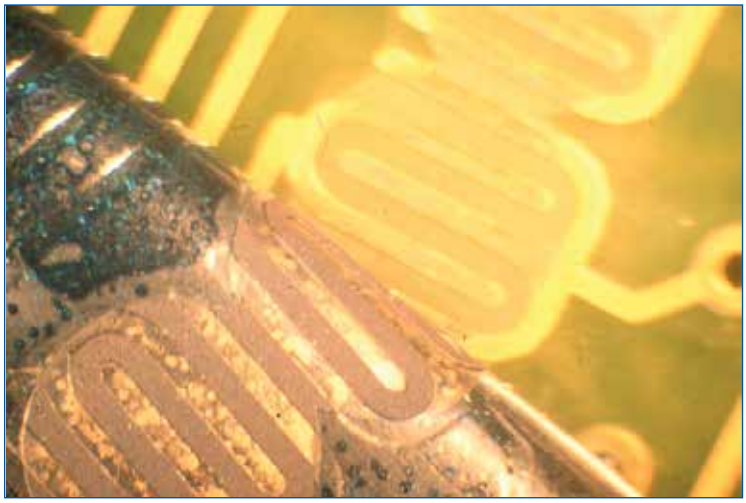


FIGURE 1. Lack of adhesion of gold to solder pads.

MARTIN WICKHAM is a consultant at the National Physical Laboratory (npl.co.uk); martin.wickham@npl.co.uk. His column appears monthly.

When Trade Shows are Worse than Speed Dating

Can our columnist outlast a shy customer in the ritualistic convention dance?

TRADE SHOW TIME in the beautiful Pacific Northwest. One of those one-day, tabletop affairs. Cheap to exhibit. Easy logistics. No extortionate setup fees from the event promoters, like you see at the really big shows with the four-letter acronyms and the five-figure expense, just looking out for the betterment of our industry. (You know who you are.) Pristine setting a bonus. (Who doesn't like traveling to the Pacific Northwest?!) Those who fancy salmon are rewarded.

Ten-minute teardown at show close at 3 pm, leaving time for beerful reflection at day's end. Good risk/reward ratio if you snag one new customer; life is really good if you land two. A high incidence of engineers and technicians in attendance, our target crowd. An infrequent opportunity to reconnect with existing customers, too, in a relaxed setting. Comfortable surroundings afford productive time to share gossip, spread rumors, and hatch conspiracies with friends and colleagues, both esteemed and otherwise.

In the midst of these festivities, he makes his entrance. He will not tell you his name. Paradoxically, he wants you to know who he is, but you must work for that knowledge. His show badge is discreetly, deliberately tucked into his shirt, away from inquisitorial, peddling eyes. Not unlike a Catholic bishop who hides his pectoral cross. A techie bishop. No business card, its absence connoting importance. No eye contact either. He mumbles, deliberately. He deflects questions. Clearly he's had some coaching, or peer influence has rubbed off. He won't tell you where he works at first. No way, no how. Then he gushes about his employer anyway, in a sort of Ivy League-ish boastfulness, daring you to ask, dropping large enough hints that you grab the bait. He wants you to grab the bait, while preserving his aura of exclusivity. It's in the culture. One of the cool kids. Because he exudes awesomeness simply because of where he works, and he sends enough signals that he wants you to know that. Can barely contain it. He can't resist. He desperately wants you to know, but he won't tell you, craving the attention. Like a Cheshire Cat without the self-satisfying grin. It's Seattle, after all, serious business, and the field of usual suspects narrows with a few pointed questions. He really does want you to know, but you have to solve his riddles to recognize his employer. He craves the attention these riddles provide. Like it or not, he is the New Generation, and he has married privilege, to which we are expected to genuflect. He is the Reality We Must Deal With. Greetings, earthlings.

Call him Amazon Guy.

He works the room, gliding from table to table in splendid anonymity, not lingering at any too long, lest some eager salesperson engage him in unwelcome, intrusive and all-too-revealing conversation. He keeps moving. He asks limited, general questions, not wanting to disclose much, keeping it all at a need-to-know level. Nothing sticks; he is Teflon. He is their advance scout, and today is Reconnaissance Day on somebody else's dime. The mothership awaits his report.

He could be Facebook Guy, or Netflix Guy, or Apple Guy or Google Guy. Or even Startup Guy. It's not the company. It's the attitude. And it's almost always guys. They all went to the same school: Plain Vanilla Institute of Technology. Double major in engineering and obfuscation. With honors.

On his second orbit of the room he lands back at our table, and starts entertaining himself by leafing through a stack of 3-D CT scanning images provocatively arranged in our display. He seems interested; maybe the images have their own unique gravitational pull. Anyway, they pull him. He looks away, then looks back, several times. Like he's satisfying a guilty pleasure. There is interest. Time for dialogue. Countering his habits, we do our best to make eye contact and extend pleasantries.

"Can we explain those images to you?"

"I know what they are."

Of course he does. He says this while directing his speech at an oblique angle from where you sit, no doubt capitalizing on the acoustics.

"In that case, can we help you with similar services? It appears you are interested in our CT scanning capabilities. Is there a specific problem we may assist you in resolving? Do one or more of these CT scans resemble a problem you're dealing with now? Give us some details and we'll see if there's a match."

No answer. Not even so much as an acknowledgment. That rigorous cultural immersion training again. Admit nothing. He continues to sift through the assorted images without comment. Like a detective. Or a spy. Maybe he is a spy. Matching things scrupulously. Assessing what his own operation lacks, and what his superiors need.

"May we take down your contact information so we might send you some literature about our services?"

Again, no answer at first. Then mumbling, directed at no one in particular. Then a hastily averted gaze. Then departure, doubtless to forestall further engagement. He leaves the room, maintaining the mystery.

But then he comes back 30 minutes later, following the conclusion of a stemwinder about thermosetting adhesives. Fifty-seven utterly captivating PowerPoint slides in 4K vision and surround sound. He looks somewhat reduced from the edge-of-your-seat

ROBERT BOGUSKI is president of Datest Corp. (datest.com); rboguski@datest.com. His column runs bimonthly.

excitement, like part of him sweated itself away, leaving fatigue. Thermosetting adhesives will do that to you.

The ritual of engagement renews. Haley's Comet on fast-forward. Further detached scrutiny of our x-ray and CT scanning images. He has a problem and he wants something. The truth is out there. Despite the odds, time to attempt contact with intelligent civilization, using better means.

"Can we interest you in some of our other testing services?"

Once again, it's Sphinx 3.0. No verbal acknowledgment whatsoever. He pivots away and saunters down our row of display tables, stopping at one or two of them to stare at the wares on display, always careful to keep that name badge safely tucked away and not prone to gravity-induced revelation. Preserving precious anonymity, but only just. So goes the act.

He leaves the room yet again. This time it's to answer the universal call for sustenance. Lunch, made more agreeable by being free for all attendees and exhibitors alike, whether with exposed badges or not. No discrimination here. The hotel has set up warming trays directly outside of our ballroom. A queue of hungry attendees and exhibitors forms in two orderly rows, flanking the table, clutching their cheesy trade show swag bags and balancing them on one hand while manipulating plates of food on the other.

Duly provisioned, he returns to the hall yet again. The sponsors of the show have positioned several large, round tables in the center of the hall. We exhibitors have our tables situated around the perimeter of the room, creating a deliberate bullpen effect, thus enabling us to size up the occupants of the large round tables while they consume their free lunch. Evidently somebody did market research that food choice predicts sales prospects. You are what you eat.

He eats alone.

We scrutinize him for 20 minutes. We eat, too, at our display table. Thus energized, both him and, hopefully, us, we hope for better prospects. There are challenges. It is well-known that the afternoon portion of a one-day show is often the Dead Zone, when interest lags and attendance drops because locals lose the excuse to skip out for lunch and need to return to work. Afternoon speakers can sap attendance too. Nonetheless, his trajectory brings him to our table a fourth time, not talking with his mouth full and not yet nodding off from milk and cookies.

We politely resume the sales ritual. It is why we're here in this ballroom, after all. Something keeps drawing him back. What is it that interests him: The cool pictures? The holographic images of CT scans we're displaying? Why does he refuse to articulate what he wants? How is it that we are we not clicking with this guy? His body language screams we are not fulfilling expectations. Our body language retorts that we are tired of faking sincerity. Get to the point.

He doesn't get to the point. He drifts off yet again. Maybe he's composing his RFQ in his mind, with the meticulousness of a Shakespearean soliloquy. Maybe he's under orders to commit to nothing, like a North Korean diplomat. Or perhaps he's just really shy. Then again, maybe he really is a spy.

This is worse than speed dating.

The hall is, predictably, thinly populated. Mostly salespersons standing or wandering around, telling tales. We have entered the Boredom Phase, between last speaker and the blessed relief of cocktail hour. It can't come soon enough.

Salesman's self-reinforcing lies are interrupted by a fifth apparition. He's back. Still no words are exchanged. This gentleman needs elocution lessons. I'm tempted to recommend a good book he can get on Amazon.

This time, however, he gathers remembrances. We have pens. He scoops up pens from our table. We have brochures. He covetously grabs a bunch and stuffs them into his solder paste company bag. We have flash drives, emblazoned with our logo, for his precious memories. He greedily takes one of those, too. He looks fulfilled. He grins for the first time. Mission accomplished. He takes his leave, secure as a man can be, holding a Day-Glo green shopping bag. The mothership awaits.

Beam him up. **CA**

Zestron, continued from pg. 37

"Many customers stay longer than a day because of challenges they are having," Sawairi said. "It's not uncommon [for them] to stay a week. We want to accommodate them."

"But generally, within a day, we can solve a problem, and we've never *not* been able to solve a problem," Wack added. "If you don't have local tech centers and engineers, it won't happen."

Customers go home with a comprehensive report detailing the cleanliness and surface quality achieved and recommended implications.

No set arrangements are in place for Zestron to open more technical centers, although Wack says there have been talks about Brazil or India. With its current eight sites, Zestron has come a long way since CIRCUITS ASSEMBLY covered the company's Manassas, VA, inauguration 11 years ago, when the firm's other operations were limited to Ingolstadt and Shanghai.

After spending several days alongside members of Zestron's team, including Wack and his father, founder Oskar Wack, Ph.D.; Ralph Hoeckle, managing director, Zestron Europe/North Asia; John Shen, general manager, Shanghai; Doris Lam, sales manager, Zestron South Asia; John Zarno, chairman of the board of directors; Yeoh; Sawairi, and several others, it's clear an age-old saying we're all familiar with is true: "If you put your mind to something, anything is possible," Wack said.

Not unlike a global, multilingual family, the talented minds of Zestron will have "favorable wind pushing (from) the back," according to the mayor of Samukawa.

"We can't wait to establish market leadership (in Japan)," the firm's president said. It took them 25 years to establish market leadership in Asia, and the high-precision electronics cleaning specialists show no sign of stopping. The party, it appears, has a lot of life in it yet. **CA**

CHELSEY DRYSDALE is senior editor at CIRCUITS ASSEMBLY; cdrysdale@upmediagroup.com.

X-ray Magnification – Transmissive and Reflective Targets

At the highest magnifications, the differences between the two types of targets become clear.

IN THESE COLUMNS, I have often mentioned the term geometric magnification (GM) and how this value defines the available magnification for x-ray imaging. GM is the ratio of the distance between the x-ray source and the detector and the distance between the x-ray source and the sample. Therefore, the closer the x-ray source can get to the sample for a fixed detector distance, the greater the available imaging magnification. However, these GM distance measurements are defined from the point of origin of the x-rays within the x-ray tube, called the focal spot, and not the point from which the x-rays physically exit the tube housing. This distinction is important to understand, as the configuration of the x-ray tube in a particular x-ray system will have an in-built separation distance between the location of the focal spot and the point of exit of the x-rays through what is called the tube x-ray window. Depending on the x-ray tube used, this in-built separation distance may be a much greater limiting factor to the available image magnification that an x-ray system can provide compared to how close the x-ray window can be placed relative to the sample. As such, x-ray tube choice may impact the capability of an x-ray system to see to a magnification adequate to permit sufficient analytical quality of the smaller, and continually shrinking, features within electronics boards and components.

To understand why this is the case, it is necessary to appreciate how x-rays are produced within the tube. In simple terms, the x-ray tube generates electrons that are then accelerated toward a metal target through an applied voltage. The high energy impact of the electrons on the metal produces the x-rays. During x-ray tube operation, the accelerating voltage is known as the "kV." In principle, any metal could generate x-rays, but for electronic applications tungsten (W) is most common. Operationally, all this takes place within an evacuated environment to ensure the electrons can travel toward the target without being stopped by intervening air molecules and potentially damaging the electron-generating component. Once the x-rays have been created, they need to exit the tube housing. This is where the type of x-ray tube target impacts the available magnification. X-ray targets can either be transmissive or reflective in their style (FIGURE 1).

Transmissive targets have a very thin layer of target material (< 10µm thick) directly bonded to the x-ray window (typically around 500µm or 0.5mm thick). The window material could be diamond, beryllium or aluminium. Diamond and beryllium are transparent to x-rays, hence the term window. Aluminium is not transparent to x-rays, but as it is a light element and the thickness used is small, its effect on x-rays passing through is relatively minimal for electronics applications. Once the incoming electrons hit the front side of the target material, x-rays are produced and transmit through the target material thickness into the window material before exiting the tube, hence the transmissive name. Some self-absorption of the produced x-rays does occur as they pass through the target material, and that is why the target material is so thin. Typical total target plus window thickness is 0.5mm or less. Therefore, this is physically the closest a sample can be placed to the focal spot. In contrast, reflective targets, as their name suggests, have the produced x-rays reflecting

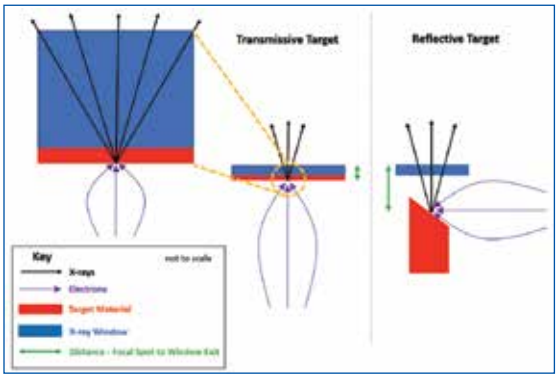


FIGURE 1. Schematic of transmissive and reflective target type x-ray tubes indicating the substantial difference in the distance of their focal spots to the exit of their x-ray windows.

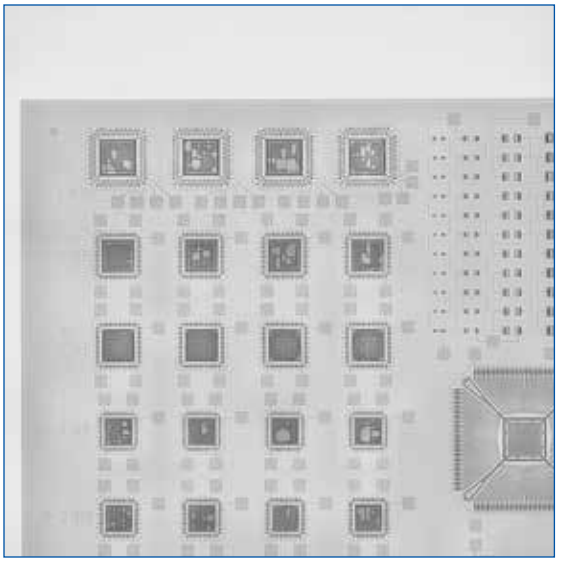


FIGURE 2. Low-magnification x-ray image example, achievable with x-ray tubes containing either a transmissive or reflective target.

DAVID BERNARD, Ph.D., is an expert in use and analysis of 2D and 3D (CT) x-ray inspection techniques for electronics; dbc@bernard.abel.co.uk.

off the front surface of the target before exiting the tube through the window. As the x-rays do not need to pass through the target, the target material can be of any thickness. A typical minimum distance from focal spot to window exit for a reflective target x-ray tube is ~8mm, which is 16x the distance of the typical transmissive target x-ray tube described above.

Different x-ray tubes from various manufacturers will vary slightly from these values, of course, but based on these numbers, what does this mean for the geometric magnification of an x-ray system where the detector is 300mm from the focal spot of both tube types? For a very thin sample placed outside on the window, the transmissive tube would give a maximum available GM of 300/0.5 = 600x. The reflective tube would give a maximum available magnification of 300/8 = 37.5x. If we then consider a more real world application where a BGA sits atop a 2mm thick board, in these respective system configurations the transmissive tube provides maximum magnification of 300/(0.5 + 2) = 120x, and the reflective tube gives 300/(8 + 2) = 30x. In both situations, the maximum available magnification will continue to reduce as the sample moves farther away from the tube.

What does this difference in available magnification mean in imaging terms? As an example, **FIGURE 2** shows a low-magnification image of QFNs on a test board. In this image, the sample is substantially farther from the tube compared with any in-built focal spot to window exit distance. Therefore, in magnification terms, x-ray tubes with either target type are acceptable to provide a suitable image for analysis. The differences between transmissive and reflective targets become more apparent at the highest available magnifications (**FIGURES 3** and **4**). Figure 3 shows an x-ray image of a section of the same sample where the focal spot to sample distance is 8mm, as for a reflective target. Figure 4 has the focal spot to sample distance set at ~ 0.5mm, as for the transmissive target. The difference in available analytical detail between the two images is clear. As samples become thinner and contain smaller features, the difference in what can be seen in the images available at maximum magnification becomes greater.

In this column I have concentrated on the impact to image magnification caused by transmissive and reflective targets. There are other issues/differences these target types have in relation to image quality caused by x-ray focus (resolution) and power; these will be discussed in a future column. For now, when considering a new x-ray system, ensure there is sufficient available magnification to see the features you must inspect, both now and for tomorrow's applications. **CA**

Au.: Images courtesy Peter Koch, Yxlon International.

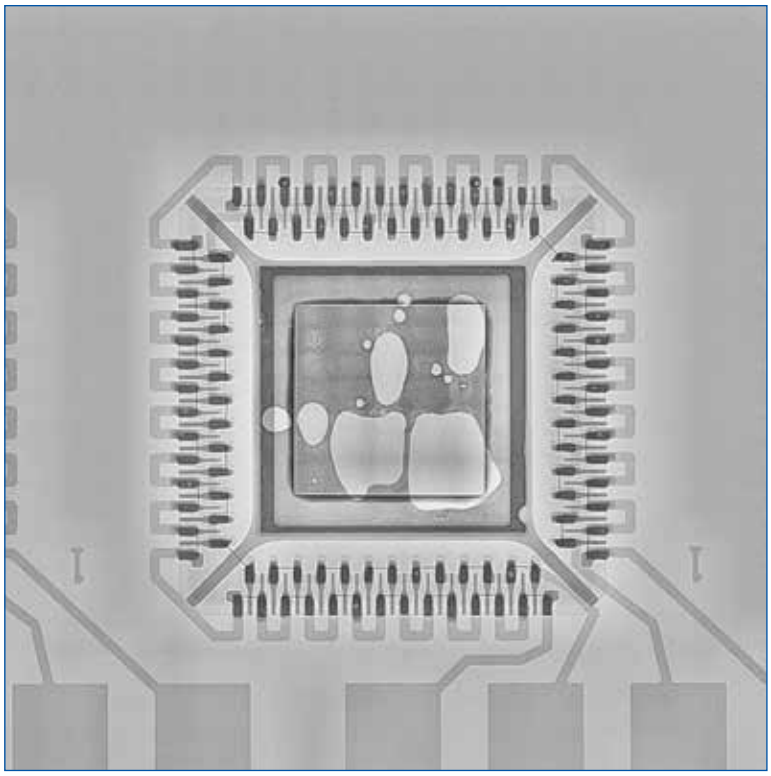


FIGURE 3. X-ray image showing the maximum available magnification for the same sample placed ~10mm from the tube focal spot, representing a reflective target x-ray tube.

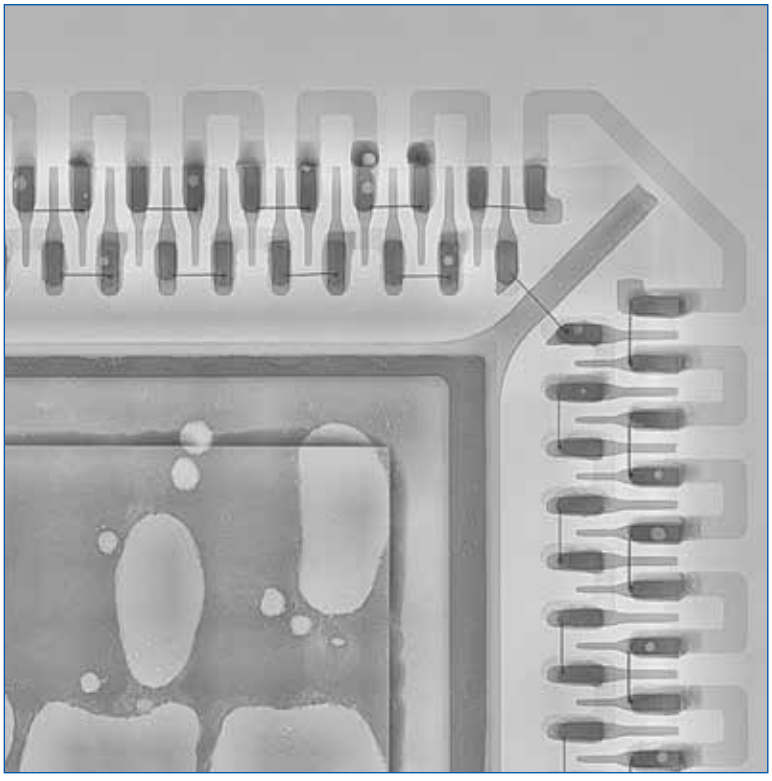


FIGURE 4. X-ray image showing the maximum available magnification for the same sample placed ~0.5mm from the tube focal spot, representing a transmissive target x-ray tube.

To Fixture or Not?

A PCB carrier can reduce variations on solder joint geometries.

ELIMINATING DEFECT OPPORTUNITIES by minimizing process variation is a key concept of Lean manufacturing. Fixturing is often a key ingredient in that. However, many contract manufacturing customers see fixturing as an unnecessary nonrecurring engineering (NRE) expense. The reality is fixturing does add cost, but it can also save money in production. More important, printed circuit board (PCB) technology is driving the need for greater use of fixturing. Consequently, the decision on whether to fixture or not is being made more frequently.

Use of a printed circuit board assembly (PCBA) carrier for fixturing has several benefits, including:

- Support for the PCBA and larger components.
- Elimination of PCB "rails," which could reduce PCB cost.
- Repeatable and time-efficient setup.
- Minimization of mechanical stress.
- Minimization of thermally induced stress.

Support for PCBA and larger components. PCB fabrication technology is enabling the design and fabrication of high density interconnect (HDI) and thinner PCBs, as well as much thicker high-layer count, larger PCBs with complex internal interconnections. Assembly and test process tooling and flow should be designed to minimize mechanical and thermally induced stress on these PCBAs.

Larger components such as high-pin-count BGAs, multichip modules (MCMs) or larger SMT connectors could potentially get warped during soldering processes. Proper fixturing can provide a stable surface to support the PCBA throughout the manufacturing process from screen printing through reflow, or as needed through wave soldering, subsequent cleaning processes and test.

Elimination of PCB rails. Breakaway rails are typically used as part of multi-up PCB panels for smaller PCBs, and even as a single-up PCB panel if the board isn't a standard rectangular shape or has components that are too close to its edges for automated handling. Depending on the board shape and size, a panel that is designed to be transported by itself during assembly processes, with no additional carrier, could end up with excessive "breakaway areas" that increase PCB area and cost. Depending on the bare board and assembly details, upfront planning to use a fixture as part of the assembly flow may enable use of more area-efficient multi-up PCB panels or eliminate the addition of breakaway rails entirely.

Repeatable and time-efficient setup. Use of dedicated carriers to host a PCB or multi-up panel during assembly processes can improve setup repeatability and time. Ensuring a repeatable mechanical setup to support the PCB reduces assembly process variation.

Minimization of mechanical stress. Proper fixture design to support PCBA during assembly processes minimizes the *in situ* mechanical stress on the board, components and their internal interconnections as well as stresses to the existing soldered joints on a typical densely populated PCBA with components on both sides.

PCBs assembled in panel form, either in single or multi-up, require an additional depaneling operation to separate the board into its final form. Fixturing provides an opportunity to eliminate or reduce the extent of this depaneling operation.

Minimization of thermally induced stress. Thermally induced stresses on PCBAs, both *in situ* during soldering processes, as well as after the soldered interconnections, can be minimized by utilizing a carrier during the soldering operation. When a PCB and components warp during reflow or wave soldering, it increases the number of soldering defects and the stress in soldered interconnections. Reducing variation on the effective relative positions of surfaces to be interconnected during soldering is important to reducing soldering defects. Use of a PCB carrier to achieve this mechanical constraint during solder joint formation will in turn reduce variations on the final solder joint geometries.

On the other hand, as with other alternative engineering solutions, there are perceived disadvantages of using dedicated carriers to load and unload the PCBAs, manage their storage, usage and procurement costs. Viewed from the perspective of technological changes that are resulting in far more delicate PCBAs, fixturing represents a relatively low-cost solution compared with the costs associated with handling or thermally induced defects. And when the total amount of savings in terms of reduced substrate material use, processing time and improved first-pass yield are considered, fixturing often pays for itself. CA

YOUSEF HEIDARI is vice president of engineering at Sigmatron International (sigmatronintl.com); yousef.heidari@sigmatronintl.com.

SMTA International

2018

The Industry's Strongest Technical Conference

Electronics Manufacturing Conference & Expo

Save the Date

October 14-18, 2018

Donald E. Stephens Convention Center

Rosemont, IL, USA

Electronics Exhibition
October 16-17, 2018

Technical Conference
October 14-18, 2018

www.smta.org/smtai

Premium Sponsor:

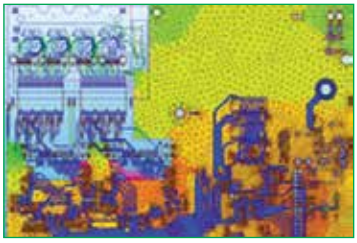
Panasonic

total solutions for any mix any volume

Co- located with:

IPC

sensors MIDWEST



PCB DESIGN SIMULATION

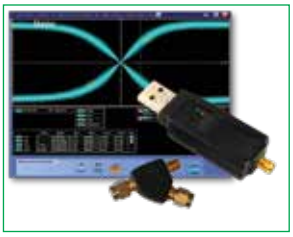
Ansys 19.1 delivers new analysis capabilities in the electromagnetics suite for designing wireless communication, autonomous and electrification technologies. New features include ADAS and autonomous radar analysis and new hybrid simulation techniques for PCB analysis. Comprehensive system modeling functionality is included with the electromagnetic field simulation products, delivering advanced analysis capability for power electronics systems.

Ansys
ansys.com/19-1

DOUBLE CIRCULAR BLADE DEPANELIZER

K4000 M24 singulates pre-scored metal core panels. Two blades are set to shear pre-scored aluminum or copper panels. Optional light beam safety curtain and ESD-safe belt conveyor. IR sensor stops belt for PCBs.

FKN Systek
fknsystek.com



FAST-EDGE SIGNAL GENERATOR

PerfectPulse provides square 32ps edge pulse. -500mV, 50Ω output signal is square, without overshoot or undershoot. For verifying instrument and probe rise/fall times, verifying signal path rise/fall time and undershoot/overshoot, and as high-performance TDR for measuring PCB coupons, cable and PCB trace impedance, verifying cable crimps, measuring trace and cable lengths, Dk, and other applications. Pocket-sized.

Picotest
picotest.com

OTHERS OF NOTE

COF IMMERSION SN FINAL FINISH

Stanna-COF immersion tin enables chip-on-film technology. Bonds chips straight onto traces, for a smooth and even finish. Enhances yields and functionality and permits high-volume reel-to-reel production. May enhance fine-line capability and provides a protective and functional final finish.

Atotech
atotech.com

HIGH-IMPEDANCE LAMINATE

Magtrex 555 features high permeability and permittivity. Expands trade-space of antenna design, enabling size reductions up to a factor of six with minimal impact on bandwidth, up to a factor of six increase in bandwidth with similar size, or a design optimum in between. Can miniaturize VHF and UHF antennas, while maintaining bandwidth achieved in a larger design. Based on ceramic/PTFE composite system.

Rogers Corp.
rogerscorp.com

RF-READY LAMINATE

Meteorwave 8000 is high-speed, low-loss digital and RF electronics material for high-layer-count PCBs in 56Gbs to 112Gbs applications. Typical loss (Df) of 0.0016 at 10GHz. Comes in thicknesses 0.0012" and up.

Park Electrochemical Corp.
parkelectro.com

LOW-LOSS BONDING MATERIALS

RO4450T are 3.2-3.3Dk, spread-glass reinforced, and ceramic-filled. Come in 3 mil, 4 mil or 5 mil thicknesses. Exhibit excellent Dk control for repeatable electrical performance and a low z-axis expansion for PTH reliability. Are compatible with standard FR-4 processes. For multilayer designs requiring sequential lamination. UL 94 V-0 flame retardant rating. Compatible with Pb-free processes. Complement RO4835T and RO4000 laminate family.

Rogers Corp.
rogerscorp.com

PCB CURING OVEN

No. 813 is a gas-heated 500°F(~260°C) walk-in oven. 350,000 BTU/HR is installed in a modulating natural gas burner. Workspace dimensions are 48" x 48" x 72". Has 4" insulated walls and an aluminized stainless steel interior and exterior.

The Grieve Corp.
grievecorp.com

TEST WORKFLOW SOFTWARE

LabVIEW 2018 includes new tools that reportedly simplify system integration and grant more control through hardware accessibility. Integrates third-party IP from tools like Python. Can strengthen code reliability by automating building and execution of software through integration with open interface tools like Jenkins for continuous delivery. Includes improved learning functions and floating-point operations.

National Instruments
ni.com/labview

INTELLIGENT PARTS STORAGE

YST15 SMD storage system interlinks with component mounting lines to automatically store and manage supply of SMDs. Stores up to 1,500 reels (for the 7" 8mm format). Can also load or unload a maximum of 27 reels in one batch. Interlinks with mounters controlled by Intelligent Factory IoT/M2M integration system supply. Optional humidity management.

Yamaha Motor
yamaha-motor-im.com/en/

AUTO-PROFILER WITH TRACEABILITY

RPI i4.0 comes with network software for real-time dashboard, data sharing and traceability storage. Automatically acquires profile data from each product soldered in reflow oven in real-time. Is said to offer full thermal process traceability, reduce scrap and rework, improve production line utilization and fast defect troubleshooting.

KIC
kicthermal.com

COATING THICKNESS ANALYSIS

W Series uses poly-capillary optics to focus x-ray beam to 7µm FWHM. A 150x magnification camera measures features on that scale; is accompanied by secondary, low-magnification camera for live-viewing samples and birds-eye macro-view imaging. Dual-camera system shows entire part, zooms with high-mag camera, and pinpoints features to be programmed and measured. Programmable x-y stage (less than +/-1µm for each axis).

Bowman
bowmanxrf.com

OTHERS OF NOTE

'ALL PARTS' SOLDER TEST KIT

Solder paste analysis toolkit integrates market requirements and offers turnkey solder evaluation tool. Includes PCB design, BoM, full programming documentation, setup, test methods, and step-by-step directions for a designed experiment. Integrates area arrays down to 0.3mm pitch; 0.4mm pitch BTCs; 1206s to 008004s. Assesses 22 material properties, plus BoM and labor costs. User-defined scorecard indicates best solder paste for a specific operation.

Henkel
henkel-northamerica.com

QFN INSPECTION

Quadra 3 features novel QuadraNT sealed x-ray tube, said to require no regular maintenance. Reportedly performs uninterrupted operation at 0.95µm. Detects defects on BGAs, QFNs and IGBT attachment, PTH filling, interfacial voiding, component cracking and counterfeit devices. Can be used with X-Plane software option to look at individual image planes, for examining complex PCBA arrangements such as double-sided boards and PoP structures.

Nordson Dage
nordsondage.com

BENCHTOP FLUID DISPENSER

Performus X is air-powered (or pneumatic). X100 features 0-100psi (0-7 bar) pressure regulator for applying low- to high-viscosity fluids such as glue, silicone, UV-cure adhesives, and solder paste. X15 features a 0-15psi (0-1 bar) pressure regulator for greater control when dispensing low-viscosity or thin fluids such as solvents. Housing acts as a Faraday cage for improved EMI/RFI protection.

Nordson EFD
nordsonefd.com/performusx

300X DIGITAL MICROSCOPE

EVO Cam II digital microscope offers up to 300x optical magnification, 12x digital zoom (combined magnification up to 3600x), customizable overlays to aid inspection, and up to 10 preset settings. Comes equipped with dimensioning capabilities using a grid overlay in x and y axes. Large zoom range measures different size components. Saves different calibrations at set zoom positions. Captures live video streaming and images at HD 1080p/60fps. Eight-point LED ring light. Optional sub-stage lighting.

Vision Engineering
visioneng.com

LOW-TEMP SOLDER PASTE

PQ10 is made with Sn42Bi58 alloy and has melting point of 138°C. Compared to SAC, it reportedly reduces peak reflow temperature; energy consumption; and warpage of PCB and components. Is paired with PF735 and PF743 alloys. Fine bismuth phase; good drop test performance; good thermal cycle test performance.

Shenmao
shenmao.com

HIGH-TEMP EPOXY

Supreme 62-1 is a solvent-free, two-component, toughened epoxy system. Is serviceable from -60° to +450°F (-51° to +232°C). Chemically resistant to a range of acids, bases, fuels and solvents, even at elevated temperatures. Can be used as adhesive/sealant for aerospace, electronic, optical and specialty OEM applications. Tensile strength of 8,000-9,000psi and tensile modulus of 450,000-500,000psi.

Master Bond
masterbond.com

In Case You Missed It

This column provides abstracts from recent industry conferences and company white papers. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

Electrical Transmission

"Momentum-Space Indirect Interlayer Excitons in Transition-Metal Dichalcogenide van der Waals Heterostructures"

Authors: Jens Kunstmann *et al;* jens.kunstmann@tu-dresden.de.

Abstract: Monolayers of transition-metal dichalcogenides feature exceptional optical properties that are dominated by tightly bound electron-hole pairs, called excitons. Creating van der Waals heterostructures by deterministically stacking individual monolayers can tune various properties via the choice of materials and the relative orientation of the layers. In these structures, a new type of exciton emerges where the electron and hole are spatially separated into different layers. These interlayer excitons allow exploration of many-body quantum phenomena and are ideally suited for valleytronic applications. A basic model of a fully spatially separated electron and hole stemming from the K valleys of the monolayer Brillouin zones is usually applied to describe such excitons. Here, the authors combine photoluminescence spectroscopy and first-principles calculations to expand the concept of interlayer excitons. The authors identify a partially charge-separated electron-hole pair in MoS_2/WSe_2 heterostructures, where the hole resides at the Γ point and the electron is located in a K valley. The authors control the emission energy of this new type of momentum-space indirect, yet strongly bound exciton by variation of the relative orientation of the layers. These findings represent a crucial step toward the understanding and control of excitonic effects in van der Waals heterostructures and devices. In the future, this research could contribute to electronics with more controlled properties. (*Nature Physics*, April 2018)

"Direct Evidence of Ferromagnetism in a Quantum Anomalous Hall System"

Authors: Wenbo Wang, Weida Wu, *et al*; wdwu@physics.rutgers.edu.

Abstract: Quantum anomalous Hall (QAH) systems are of great fundamental interest and potential application because of their dissipationless conduction without the need for an external magnetic field. The QAH effect has been realized in magnetically doped topological insulator thin films. However, full quantization requires extremely low temperature (T<50 mK) in the earliest works, although it has been significantly improved by modulation doping or co-doping of magnetic elements. Improved ferromagnetism has been shown in these thin films, yet direct evidence of long-range ferromagnetic order is lacking. Herein, the authors present direct visualization of long-range ferromagnetic order in thin films of Cr and V co-doped $(Bi,Sb)_2Te_3$ using low-temperature magnetic force microscopy with in situ transport. The magnetization reversal process reveals typical ferromagnetic domain behavior – that is, domain nucleation and possibly domain wall propagation – in contrast to much weaker magnetic signals observed in the endmembers, possibly due to superparamagnetic behavior. The observed long-range ferromagnetic order resolves one of the major challenges in QAH systems, and paves the way toward high-temperature dissipationless conduction by exploring magnetic topological insulators. (*Nature Physics*, May 2018)

Reliability

"Reliability Assessment of Electronic Assemblies under Vibration by Statistical Factorial Analysis Approach"

Author: Mohammad Gharaibeh; mohammada_fa@hu.edu.jo.

Abstract: This paper aims to present a reliability performance assessment of electronic packages subjected to harmonic vibration loadings by using a statistical factorial analysis technique. The effects of various geometric parameters, the size and thickness of the printed circuit board and component and solder interconnect dimensions on the fundamental resonant frequency of the assembly and the axial strain of the most critical solder joint were thoroughly investigated. A previously published analytical solution for the problem of electronic assembly vibration was adopted. This solution was modified and used to generate the natural frequency and solder axial strains data for various package geometries. Statistical factorial analysis was used to analyze these data. The results of the present study showed the reliability of electronic packages under vibration could be significantly enhanced by selecting larger and thicker PCBs and thinner and smaller electrical components. Additionally, taller and thinner solders might also produce better reliability behavior. (*Soldering & Surface Mount Technology,* vol. 30 no. 3, 2018)

Material Gains, continued from pg. 20

The stability of substrate parameters over time and temperature is extremely important to ensure repeatable performance. In addition to setting new benchmarks for Dk and Df, further innovations such as Hyper Very Low Profile (HVLP) copper give conductors a consistent surface finish for near-perfect PIM performance compared with standard HTE copper foils.

As our industry continues to redefine the limits of possibility, we can expect to face even more exacting engineering challenges – wherever in the signal chain our expertise may lie. These challenges will likely demand even more inventive and thoughtful solutions. But we are consumers, as well as inventors, and we all share the desire to discover what comes next. **PCD&F**

REL61™ Lead-Free Alloy

WAVE & SMT : ONE ALLOY THAT DOES IT ALL

☑ HOLE-FILL

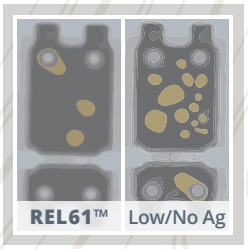
- **SUPERIOR WETTING & HOLE-FILL** VS LOW/NO SILVER ALLOYS

☑ LOW COST

- **LOWER COST** VS SAC (SN-AG-CU) ALLOYS

☑ REDUCES VOIDS

- **LOWER VOIDING** VS ALL LOW/NO SILVER ALLOYS



☑ RELIABILITY

- **ENHANCED RELIABILITY** VS ALL COMMON LEAD-FREE ALLOYS

ALSO AVAILABLE : AIM's ***award winning*** **REL22™ Lead-Free Solder Alloy** for extremely harsh environments

AIM Global Solder Solutions

www.aimsolder.com | info@aimsolder.com