11. Packaging Dimensions

This section illustrates the package specification for the CY8C24x94 PSoC devices, along with the thermal impedance for the package and solder reflow peak temperatures.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip’s footprint. For a detailed description of the emulation tools’ dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

*Figure 11-1. 56-Pin (8x8 mm) QFN*

**NOTES:**
1. **HATCH AREA IS SOLDERABLE EXPOSED METAL.**
2. **REFERENCE JEDECH: MO-220**
3. **PACKAGE WEIGHT: 0.162g**
4. **ALL DIMENSIONS ARE IN MM [MIN/MAX]**
5. **PACKAGE CODE**

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<th>DESCRIPTION</th>
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