National Aeronautics and Space Administration

Body of Knowledge (BOK) for Leadless Quad Flat No-Lead/Bottom Termination Components (QFN/BTC) Package Trends and Reliability

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NASA Electronic Parts and Packaging (NEPP) Program
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OBJECTIVES AND PRODUCTS

Bottom terminated components and quad flat no-lead (BTC/QFN) packages have been extensively used by commercial industry for more than a decade. Cost and performance advantages and the closeness of the packages to the boards make them especially unique for radio frequency (RF) applications. A number of high-reliability parts are now available in this style of package configuration.

This report presents a summary of literature surveyed and provides a body of knowledge (BOK) gathered on the status of BTC/QFN and their advanced versions of multi-row QFN (MRQFN) packaging technologies. The report provides a comprehensive review of packaging trends and specifications on design, assembly, and reliability. Emphasis is placed on assembly reliability and associated key design and process parameters because they show lower life than standard leaded package assembly under thermal cycling exposures. Inspection of hidden solder joints for assuring quality is challenging and is similar to ball grid arrays (BGAs). Understanding the key BTC/QFN technology trends, applications, processing parameters, workmanship defects, and reliability behavior is important when judicially selecting and narrowing the follow-on packages for evaluation and testing, as well as for the low risk insertion in high-reliability applications.

Key Words: bottom termination component, BTC, quad flat no-lead, QFN, MLF, IPC 7093, solder joint reliability

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1. EXECUTIVE SUMMARY

As with many advancements in the electronics industry, consumer electronics is driving the trends for electronic packaging technologies toward reducing size and increasing functionality. Microelectronics meeting the technology needs for higher performance, reduced power consumption and size, and off-the-shelf availability. Due to the breadth of work being performed in the area of microelectronics packaging/components, this report limits it presentation to board design, manufacturing, and processing parameters on assembly reliability for leadless (e.g., quad flat no-lead (QFN) or a generic term of bottom termination component (BTC)) packages. This style of package was selected for investigation because of its significant growth, lower cost, and improved functionality, especially for use in an RF application.

The 2013 report of the international manufacturing initiative (iNEMI) roadmap shows component (package) trends—their decline and growth. Table 1-1 shows the component trends to smaller surface mount components and flip chip (versus wire bonded) using the relative growth rate of different single chip package types as baseline. It clearly shows that some single-chip packages, such as dual-in-line package (DiP) and wire-bond ball grid array (BGA), are projected to have negative growth while flip chip, DCA/WLCSP (direct chip attach/wafer level chip scale package) and QFN components are projected to grow at a 15% compounded average annual growth rate (CAAGR).

Table 1-1. World Wide Semiconductor Package Volume (billions of units) (iNEMI/Prismark [1]).

Package Style (Bn Units)	2010	2011	2016	CAAGR 2016/2011	% of IC 2016
DIP/SOT	5.3	4.3	3.9	-1.9%	1.4%
SO/TSOP/SOT	83.0	80.8	108.4	6.0%	37.8%
QFP/LCC	19.0	18.3	24.5	6.0%	8.6%
QFN	19.6	20.5	46.0	17.0%	16.1%
Wire Bond FBGA	8.0	8.2	12.6	8.9%	4.4%
Stacked FBGA	6.2	6.8	10.9	9.8%	3.8%
BOC	12.0	12.5	15.5	4.4%	5.4%
Wire Bond BGA	1.4	1.3	0.8	-7.9%	0.3%
COB (Wire Bond)	7.2	7.7	11.3	8.0%	3.9%
Flip Chip FBGA	0.8	1.6	8.1	39%	2.8%
Flip Chip BGA/PGA/LGA	1.1	1.1	1.6	7.1%	0.6%
DCA/WLCSP	12.9	14.5	29.2	15.0%	10.2%
COG/COF	8.6	9.2	13.7	8.3%	4.8%
Total Wire Bond	161.7	160.3	233.8	7.8%	81.6%
Total Flip Chip	23.4	26.4	52.6	14.8%	18.4%
IC TOTAL	**185.1**	**186.7**	**286.4**	**8.9%**	**100%**

The literature survey indicates the following:

- The BTC/QFN packaging size and I/O have significantly increased. Now, packages comparable to fine pitch BGA (FPBGA) are being evaluated.
- Significant design, process, and reliability data are available for conventional QFN components, but data are lacking for multi-row QFNs. Recently released specifications such as IPC 7093, have helped to ease wider use of BTC/QFN packages.
- IPC 7093 committee identifies two key issues in BTC: (1) providing the appropriate amount of solder paste and (2) ensuring solder-joint reliability is met.
- Reliability data is lacking, it is recommended to test evaluate of BTC packaging technologies to characterize behavior for insertion in low-volume and high-reliability applications.

2. SINGLE CHIP PACKAGING TRENDS

2.1 Key Microelectronics Roadmap Organizations

Industry roadmap organizations have been created to address trends in numerous technologies including microelectronic, optics, and printed electronics. The International Technology Roadmap for Semiconductors (ITRS) is the key industry roadmap provider for the conventional microelectronics field, and it is sponsored by the world's five leading chip manufacturers. The objective of the ITRS is to ensure cost-effective advancements in the performance of integrated circuits and the products that employ such devices, thereby supporting the health and success of this industry.

iNEMI (a consortium of approximately 100 leading electronics manufacturers, suppliers, associations, government agencies and universities) is another industry roadmap provider. The iNEMI roadmaps cover the future technology requirements of the global electronics industry by identifying and prioritizing gaps in technology and infrastructure. With the support of participant companies, iNEMI generates timely, high-impact deployment projects to address or eliminate those gaps.

The Association Connecting Electronics Industries (IPC) electronic interconnection roadmaps cover three basic elements: (1) the design and fabrication of semiconductors and their associated packaging; (2) the fabrication of the interconnecting substrate for both the semiconductor package and the product printed board; and (3) multiple levels of assembly and test. Figure 2-1 compares key attributes and the overlap areas of ITRS, iNEMI, and IPC. The IPC roadmap encounters challenges in covering increasingly fluid business relationship for the OEM and EMS that may be anywhere on the planet rather than previously a predominantly simple model of vertically integrated the OEM markets. Teams of experts from many organizations around the world have cooperated to ensure that the IPC roadmap presents the recommendations based on original equipment manufacturer (OEM), original design manufacturer (ODM), and electronics manufacturing services (EMS) companies' vision and needs assessment.

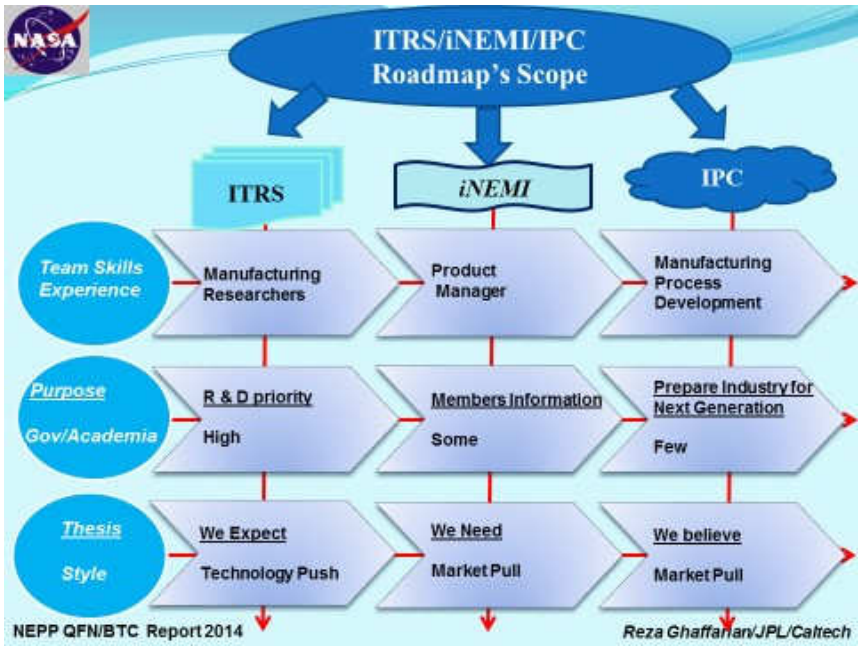

Figure 2-1. Comparison of key attributes of three industry roadmap societies for microelectronic device (ITRS), packaging (iNEMI), and assembly (IPC) technology applications.

For example, The ITRS projects that by 2020–2025, many physical dimensions are expected to be crossing the 10-nm threshold (limitation of Moore's Law). By fully utilizing the vertical dimension, it is possible to stack layers of transistors on the top of each other. This 3D approach will continue to increase the number of components per square millimeter even when horizontal physical dimensions become unable to meet demands for further reduction. Therefore, it is recognized that the semiconductor community needs to depart from the traditional scaling "technology push" approach and involve new categories in its activities. ITRS materialized this new approach in 2011, when it added a micro-electro-mechanical systems (MEMS) chapter to the roadmap, and also aligned it with the iNEMI roadmap. In addition, the two roadmap societies collaborated in summarizing key industry packaging gap and technology needs (see Table 2-1).

Table 2-1. Packaging gap and technology needs, a joint effort between ITRS and iNEMI (ITRS [2]).

Less Than 5 Years (Tactical) Gaps/Needs	Category	Comments
Need lower cost multi-layer RDL interposers (silicon or glass) and integrated passive devices	O	These technologies are very critical to support ITRS roadmap, but they are not cost effective nor available in high volume today; they need step function cost reduction
Package warpage at elevated temperature (surface mount technology [SMT] reflow) will drive the need for metrology and database and will drive new materials and new packaging structures.	R/S/O	Warpage is becoming the primary limiting factor to support further package miniaturization, particularly for larger die and TSV package on package SMT
Need for optimized, lower cost of ownership and high throughput equipment for wafer level packaging, fanout, 3D, in interposer assembly and system in Package (SiP)	O	Current equipment is mostly modified wafer fab equipment or equipment designed for single-die packaging; not cost effective nor designed or optimized for wafer-level packaging or multi-die SiP processes.
Wafer thinning and packaging of thin die will require new, cost effective equipment, materials, and processes.	R/O	This issue becomes more critical as wafer diameter increases and die thickness decreases; issues include stress relief, surface thickness variation, wafer warpage, handling after thinning, singulation, packing/shipment methods from wafer fabs to packaging houses.
New equipment capability to support assembly of SiP with a variety of components including ICs, passives, optical devices, MEMS, and biochips on the same substrate.	R/O	Greater flexibility, versatility, and precision will be required, as well as the ability to handle new processes and materials. High units per hour to reduce cost. A good example is assembly and test of chip on wafer wafer processing.
Need high thermal conductivity materials for high thermal density devices.	R/O	The new materials properties required have been included in the Emerging Research Materials Chapter [of Ref. 2].

2.2 Single Chip Packaging Trends

Extensive work [4–11] has been carried out to understand the technology implementation of area array packages for high-reliability applications. Figure 2-2 categorizes single-chip microelectronic packaging technologies into three key technologies: (1) the early introduction wire-bonded plastic ball grid arrays (PBGAs) and quad flat no-lead (QFN); (2) advanced flip-chip BGA (FCBGA) and ceramic column grid arrays (CGAs); and (3) smaller foot print chip scale/wafer level (CSP/WLP), and leadless quad flat no lead (QFN), multi-row QFN, advanced QFN (aQFN); and land grid array (LGA) packages. There are numerous variations of packages. Only design, assembly, and reliability of conventional and advanced QFN packages are discussed in detail.

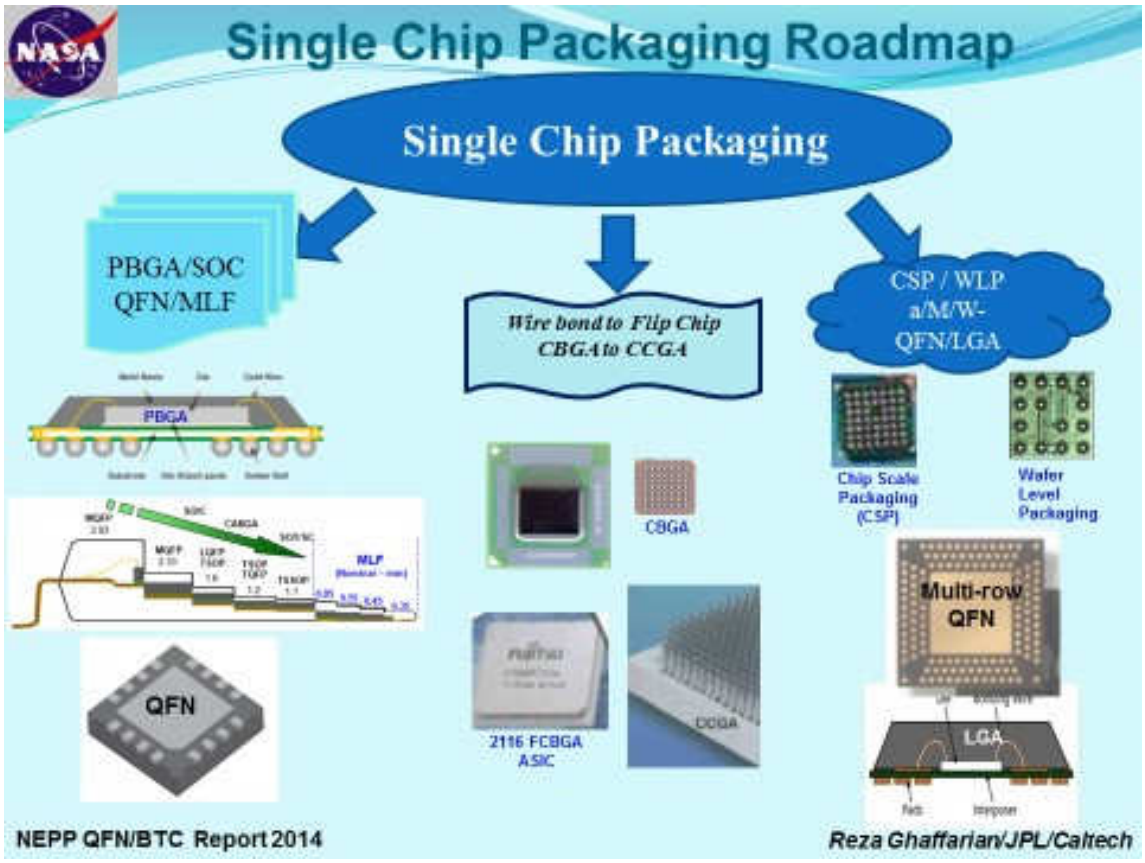

Figure 2-2. Microelectronic single-chip packaging technology trend, low and high I/O. coarse and fine pitch, and leaded and leadless configurations.

Plastic ball grid arrays (PBGAs) and chip scale packages (CSPs) are now widely used for many commercial electronic applications including portable and telecommunication products. BGAs with 0.8- to 1.27-mm pitches are implemented for high-reliability applications, generally demanding more stringent thermal and mechanical cycling requirements. The plastic BGAs, which were introduced in the late 1980s and implemented with great caution in the early 1990s, further evolved in the mid-1990s to the CSP (also known as fine-pitch BGA) having a much finer pitch from 0.4-mm down to 0.3-mm pitches.

To accommodate higher I/O single-chip die, the flip-chip BGA (FCBGA) is has been developed. FCBGA is similar to PBGA, except that internally a flip-chip die is used rather than a wire-bonded die. Because of these developments, it has become even more difficult to distinguish different area array packages by size and pitch; its internal die attachment configuration must also be considered. The ultimate size reduction can be achieved by protecting single die at the wafer level, hence the introduction of wafer level package (WLP). WLPs also address the key issues of using single bare die, and they improve ease of handling and functional testing.

For high-reliability applications, ceramic and hermetic packages of area array packages were implemented. The ceramic BGA (CBGA) package uses a higher melting ball ($Pb_{90}Sn_{10}$) with eutectic attachment to the die and board. Contrary to PBGA version, the high melt ball does not collapse during solder interconnection reflow, hence, a control standoff for improved reliability. The column grid array (CGA) or ceramic column grid array (CCGA) is similar to a CBGA except that it uses column interconnects instead of balls; hence, higher flexibility for improved reliability. The lead-free CGA uses a copper column instead of a high melting lead/tin column.

The flip-chip BGA (FCBGA) is similar to the BGA, except that internally a flip-chip die rather than a wire-bonded die is used. Refer to published reports, books, papers [4–10] for this category of microelectronics packages. Investigation of flip-chip BGAs included process optimization, assembly reliability characterization, and the use of inspection tools (including X-ray and optical microscopy) for quality control and damage detection due to environmental exposures.

2.3 Array Chip Size Packaging Trend

2.3.1 Chip Scale Packaging (CSP) Trends

The trend in microelectronics has been toward ever increasing I/Os on packages, which is, in turn, driving the packaging configuration of semiconductors. Key advantages and disadvantages of CSPs compared to bare die are listed in Table 2-2. Chip scale packaging can combine the strengths of various packaging technologies, such as the size and performance advantage of bare die assembly and the reliability of encapsulated devices.

The advantages offered by chip scale packages include smaller sizes (reduced footprint and thickness), lower weights, easier assembly processes, lower overall production costs, and improvements in electrical performance. CSPs are also tolerant of die size changes, since a reduced die size can still be accommodated by the interposer design without changing the CSP's footprint.

CSPs have already made a wide appearance in commercial industry as a result of these advantages, and now, even their three-dimensional (3D) packages are being widely implemented. Unlike conventional BGA technology at typically 0.8–1.27-mm pitch, CSPs utilize lower pitches (e.g., currently, 0.8 to 0.3-mm pitch) and hence, will have smaller sizes and their own implementation challenges.

Table 2-2. Pros and cons of chip scale package (CSP).

Pros	Cons
Near chip size	Moisture sensitivity
Widely used	Thermal management
Testability for known good die (KGD)	Limits package to low I/Os
Ease of package handling	Electrical performance
Robust assembly process	Routability
Only for area array version	Microvia needed for high I/Os
Accommodates die shrinking or expanding	Pitch limited to use standard printed circuit board (PCB)
Standards	Reliability is poor in most cases
Infrastructure	Underfill required in most cases to improve reliability
Rework/package as whole	Array package version
	Inspectibility
	Reworkability of individual balls

In an effort to systematically characterize the CSP as a package group, they may be classified into categories or types including: (1) the flex circuit interposer type; (2) the rigid substrate interposer type; (3) the custom lead frame type; and (4) the wafer-level package (WLP) type. A typical chip scale packaging process starts with the mounting of the die on the interposer using epoxy, usually a non-conductive type (although conductive epoxy is also used when the die backside needs to be connected to the circuit). The die is then wire bonded to the interposer using gold or aluminum wires. Wire bond profiles must be as low and as close to the die as possible in order to minimize package height. Plastic encapsulation to protect the die and wires then follows, usually by transfer molding. After encapsulation, solder balls are attached to the bottom side of the interposer, then the package is marked, and finally, the parts are singulated from the lead frame.

In summary, several different approaches are being employed by different companies to meet the packaging challenge of mounting high-pin count integrated circuits (ICs) to substrates. Each of these approaches has its own merits and drawbacks.

- Mount the IC internally, wire bond or flip-chip, on a flexible/rigid organic or ceramic substrate, and package the chip into a suitable package material. Apply small solder bumps to the bottom of package, flip over, and mount onto suitable mounting pads on the printed circuit board (PCB). This is commonly referred to as ball grid array, or BGA, technology. If the package dimensions are nearly the same as those of the IC, this technology is called chip scale packaging, or CSP. The principal advantages of BGAs and CSPs are their ability to protect the IC (with package) and their close similarity to flip-chip.
- Attach the IC die to the bare PCB and wire bond from the die bonding pads directly to bonding pads of the PCB. This is commonly referred to as chip-on-board (COB) or chip-and-wire direct-chip attachment (DCA).
- Permanently attach small solder bumps to the bottom of the IC die, flip it over, and then mount it onto suitable mounting pads on the PCB. This is commonly referred to as direct flip-chip.

Figure 2-3 shows flip-chip die bond, chip-and-wire direct chip attachment, and chip scale package configurations.

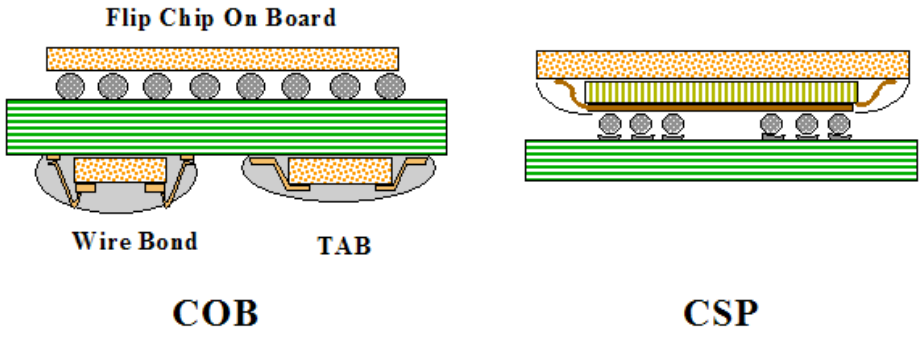

Figure 2-3. Chip-on-board/flip-chip die attachment and chip scale package configurations.

2.3.2 Flip Chip on Board [FCOB])

Flip-chip assembly is fast becoming the assembly method of choice over wire bond to connect a chip. Direct attachment of flip chips on board (FCOBs) with fine-pitch solder bumps are being increasingly used to address performance, power, size, and I/O requirements. The FCOB requires underfill to ensure solder bump reliability. However, added processing costs associated with underfill dispensing and curing, add challenges especially for fine-pitch assemblies as well as reliability. Concerns due to underfill delamination make FCOB a less likely option for the future generations of microelectronic packaging. Furthermore, reliability issues arise when low-K dielectric material (ultra low-K dielectric in the future) is used in the integrated circuit (IC) manufacturing. When such ICs are assembled on organic substrates, the stiff solder bumps could crack or delaminate the low-K dielectric material under thermal excursions.

2.3.3 Wafer Level Packages (WLP)

Microelectronic packaging is migrating from wire bond to flip chip at the die level to meet aggressive requirements for improved electrical performance and reduced size and weight. For wafer bumping, solder electroplating is commonly employed, especially for fine pitch applications. Wafer-level chip-scale packaging (WLCSP) typically utilizes wafer die and direct solder sphere placement technology (see Figure 2-4). In WLCSP, pitch and solder ball size are usually much higher and the number of I/O much lower than for the use of flip chip within a package. However, many companies plan to use WLPs for higher pin-count applications, including analog parts with larger die sizes. This will increase the number of wafers to be processed, as well as the unit volumes. The memory die is one example of a large die whose adoption significantly increases the number of wafers.

One of the major drivers for the adoption of WLPs in portable products is form factor, and mobile phones increasingly contain WLPs, representing the largest single product application. Demands for greater functionality in smaller spaces is driving the adoption of WLPs in mobile phones faster than in any other segment of the market.

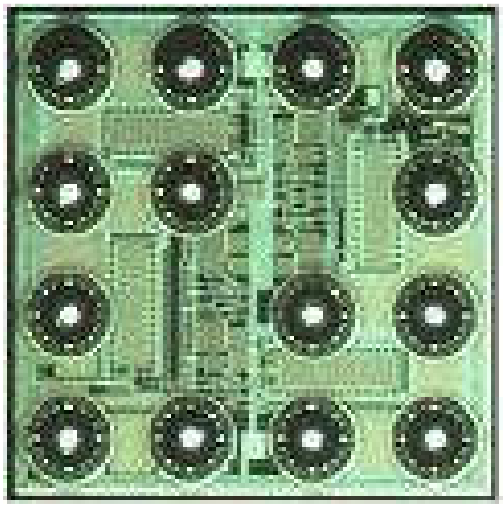

Figure 2-4. An Example of a wafer-level CSP. Note the bumps on the die.

3. LEADLESS PACKAGE STYLES

Leadless packages are generally near a die size similar to array CSPs, which have hidden terminations pads, but they are also different. They do not have solder ball spheres, but rather metallized terminations or pads and a large heat-dissipation pad under the package. Leadless packages are also known as bottom-termination components (BTCs) and numerous other nomenclatures (see Table 3-1). The terms include quad flat no-lead (QFN), dual-row/multi-row QFN (DRQFN/MRQFN), dual flat no-lead (DFN), and land grid array (LGA) packages. In addition, new terms were added for the more recently introduced improved versions. These include the advanced QFN (aQFN) and array QFN packages, which have generally multiple row terminals accommodating a higher number of inputs/outputs (I/Os). The number of I/Os approaches that of CSP/FBGA packages with the advantages of lower cost for potable and telecommunication applications.

The new I/O configuration of QFNs with an extra internal heat-sink pad will add new requirements for design, assembly, rework, and reliability limits, which are significantly different from the array CSP packaging technologies. Since there are no leads or balls in leadless packages to compensate for distortion from package or board warpage, these packages require much more control than those of CSPs in design and assembly processes. The new requirements add challenges in the second level assembly and reliability.

Inspection for assembly integrity verification and quality control become even more challenging than those difficult conditions for CSPs. The outer terminations could be inspected visually, but we were still unable to determine integrity under the terminations. For the heat-sink pad, only voiding condition can be determined with nondestructive tools such as X-ray. This chapter summarizes the literature surveyed covering these aspects of leadless packaging technologies as well as second-level reliability and correlation to workmanship defects such as voids to reliability.

Table 3.1. Typical leadless packaging styles, nomenclatures, and package supplier.

QFN Style	Definition	Reference
MLF/QFN	Micro-lead frame Quad flat no-lead package	[11, 12]
DRMLF	Dual-row MLF	[13]
aQFN	Advanced QFN	[14]
Array QFN	Array QFN	[15]
DFN	Dual flat no-lead package	[16]
NBA-QFN	No bump array QFN	[17]
TQFN	Thin QFN	[18]
VQFN/WQFN	Very thin QFN	[19]
LGA	Land grid array	[20]

3.1 Land-Grid-Array (LGA) Packaging Trend

Land grid array (LGA) packages have been increasingly used in portable electronics and wireless products because of the LGA low profile on the printed wiring/circuit boards (PWB/PCB) and direct Pb-free assembly process compatibility. Since LGA has lower standoff height and different material properties compared with the conventional BGA package; its reliability behavior becomes a concern. A major concern is the board-level solder-joint reliability of the LGA packages under thermal loading. For high-reliability applications, this approach may become a popular approach with a much wider commercial industry implementation of the European Union restriction of hazardous substances (RoHS).

LGAs in plastic package versions with low I/O and sizes have been available for thinner consumer products because of lower cost and lower assembly standoff compared to ball-grid-array versions. In some cases, the LGAs are optimized for improved radio-frequency (RF) performance for wireless applications.

For example, high coefficient of thermal expansion (HCTE) ceramic LGAs have been recently introduced replacing HCTE ball grid array (BGA) packages. The LGA solder interconnect is formed solely by solder paste applied at the board assembly because there are no sphere attached to the LGA. It was reported that for HCTE LGA [20], a lower standoff height of approximately 0.06-mm to 0.1-mm, depending on solder paste volume and PCB geometry, could be achieved. The pad surface finish of LGAs is generally electroless gold plating, 0.1 to 0.5 μm, over electroless nickel. The LGAs with such a surface finish become RoHS compliant. Key features of an LGA packages include:

- LGA package eliminates the risk of damaged columns or spheres due to shipping or handling.
- LGA packages are RoHS compliant and can be used for either lead containing or Pb-free assemblies.
- LGA packages have a lower mounted height than CGA/BGA; this can allow for more space above the device for a heat-sink solution or for small form-factor applications.
- HCTE LGA Pb-free solder paste reported to have a better board-level reliability than ceramic ball grid array (CBGA) versions with tin-lead.
- LGAs in general have much lower board-level reliability. The reduction on reliability is yet to be established.

3.2 Conventional Leadless Packaging Trends

In a 2003 paper [21], the authors state that within the last few years, the QFN package has taken industry by storm and they had already shipped one billion parts. Figure 3-1 shows a number of early generation leadless packaging configurations including MicroLeadFrame® package (MLF®), which was introduced more than a decade ago.

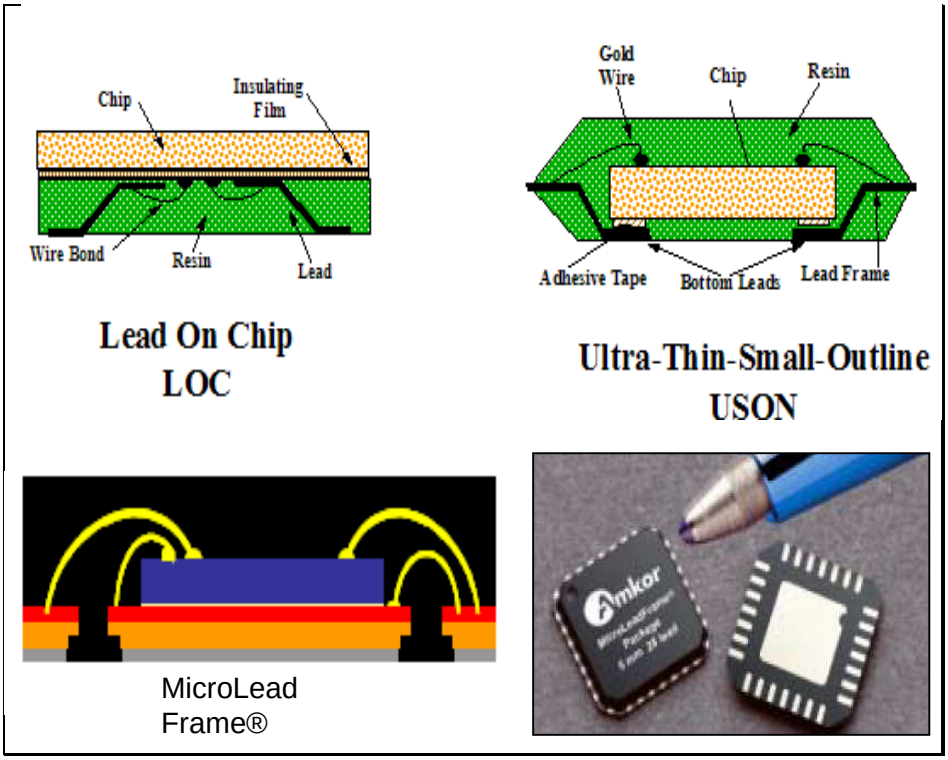

Figure 3-1. Examples of early generation of leadless packages including MLF® package.

The MLF® is a near CSP plastic encapsulated package with a copper lead frame substrate. It is a leadless package where electrical contact to the PCB is made by soldering the peripheral lands on the bottom surface of the package to the PCB, instead of the conventionally formed perimeter leads such as thin small outline package (TSOP). For MLF, the large conductive bottom pad improves the thermal and electrical properties of the package. Note the top images show earlier versions of the leadless packages such as lead on chip. There are no bottom heat-spreader pads in the early version of leadless packages.

The exposed die-attach pad on the bottom efficiently conducts heat to the PCB and provides a stable ground and electrical connections through conductive die-attach material. The design also allows enhancement of electrical performance by enabling the standard 2 GHz operating frequency to be increased up to 10 GHz with some design modifications.

3.3 Advanced Leadless Packaging Trends

The Association Connecting Electronics industries (IPC) [22] recently released the IPC 7093 specification, "Guidelines for Design and Assembly Process Implementation for Bottom Termination Components," covering the rapidly growing leadless packaging categories. The BTC is a generic term for packaging technologies which their external connections consist of metallized terminals that are an integral part of the package body and intended for surface mounting. This class of components includes quad flat no-lead (QFN), dual-row/multi-row QFN (DRQFN/MRQFN), dual flat no lead (DFN), and land grid array (LGA). The standard describes the critical design, assembly, inspection, and reliability issues associated with BTCs.

Figure 3-2 shows an example of advanced QFN (aQFN) package [14]. The aQFN is an improved version of conventional QFN with multiple row terminals accommodating higher number of I/Os. The number of I/Os become similar to that of CSP/FBGA packages with the advantage of lower cost for portable and telecommunication applications. The multiple-row QFNs; however, are more difficult to

assemble, there are more opportunities for solder-joint bridging especially when pitch is smaller, and there are higher potential for risk due to thermo-mechanical environmental exposures. The thermo-mechanical solder-joint reliability of aQFN was improved by modifying packaging processes including double-sided etching of copper lead frame to create isolated copper posts with higher standoff.

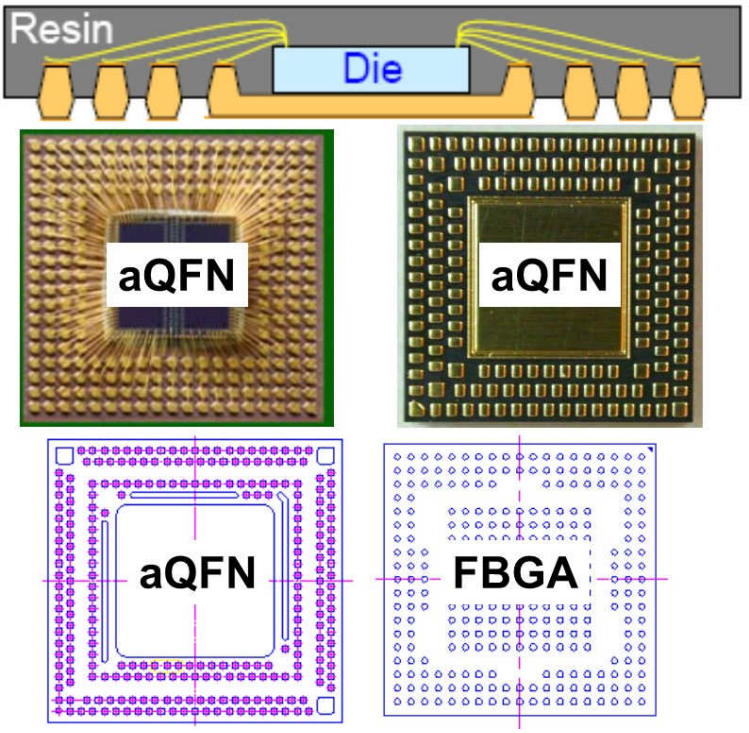

Figure 3-2. The advanced QFN (aQFN) package configuration and re-design of FBGA to aQFN for thermal and electrical characterization [14].

To compare the aQFN device characteristics to an FBGA, the authors re-designed a chip device in an FBGA package and used it in an aQFN package to produce identical functionality for testing. The author listed the key package sizes, thermal, and electrical characteristics of the packages. For example, it was shown the theta JA (θ_{JA},ºC/W) for the air velocities of 0.0, 1.0, and 2.5 m/s were 23.5, 17.8, and 15.7 for the aQFN and they were 35.7, 31.3, and 29.1 for the FPBGA. This means the reductions of about 34% to 46% in temperature for the aQFN, which contributed to its more effective heat dissipation. Testing was performed under 1 W power dissipation and 25ºC ambient temperature. Even though the longest trace in FBGA was shorter than aQFN, the aQFN outperformed the FBGA both thermally and electrically.

The electrical simulation data in frequency domain to 20 GHz for the insertion loss and the return loss were shown in plots. From these plots, author concluded that the aQFN can function above 16 GHz (at -0.3dB) and 17 GHz (at -15dB), which is significantly higher than the frequencies for the FPBGA package. In addition to the excellent thermal and electrical performances, the aQFN is also cost-effective compared to FBGA since it does not require a substrate as an FBGA does.

4. LEADLESS PACKAGE PCB DESIGN/ASSEMBLY

4.1 PCB Design Requirement

It is common that the QFN package supplier to perform some experimental trials to develop guidelines for the PCB pattern design and document them in the application notes. For example, a QFN package supplier [21] published the first revision of its application notes in September 2002. The QFN packages are designed based on the revisions of JEDEC Publication 95, e.g., 4.19, 4.20, a design standard for outlines quad no-lead staggered and inline multi-row packages (with optional thermal enhancements).

Figure 4-1 shows a PCB pad pattern design recommend for the QFN. As apparent, the design requires that the lands on the package bottom side are to be rectangular with rounded edge on the inside. Since the package does not have any solder balls, the electrical connection between the package and the motherboard is made by printing the solder paste on the motherboard and reflowing it after component placement. In order to form reliable solder joints, special attention is needed in designing the motherboard pad pattern and solder paste printing.

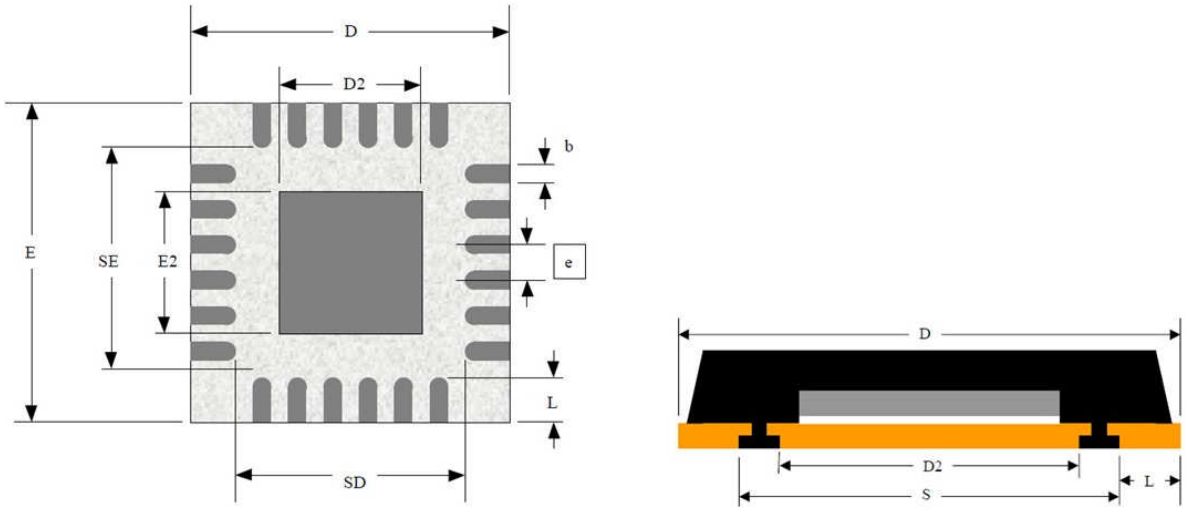

Figure 4-1. MLF® (full lead design) component dimensions needed for PCB land pattern design [21].

In general, in order the QFN performs at an optimum functionality and reliability, special attention should be given to ensure that the PCB is designed properly and that the package is mounted appropriately. For enhanced thermal, electrical, and board-level performance, the exposed pad on the package is soldered to the board using a corresponding thermal pad on the board. Furthermore, for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region. The number of thermal vias incorporated into the design depends on the power dissipation and electrical requirements of the specific application. However, thermal dissipation data show that there is a point where additional thermal vias may not significantly improve the thermal performance of the package. The PCB footprint design needs to be considered from dimensional tolerances due to package, PCB, and assembly.

The IPC consensus specifications for BTC/QFN packaging technology should be reviewed. Generic guidelines provided by the IPC specification should be combined with the specific application notes to achieve an optimum performance and reliability. Three key IPC specifications related to this subjects are [22]:

- IPC 7093: Guidelines for Design and Assembly Process Implementation for Bottom Termination Components

- IPC 7351: Generic Requirements for Surface Mount Design and Land Pattern Standard
- IPC 7525: Stencil Design Guidelines

The target audience of the IPC 7093 is composed of managers, designers, process engineers, operators, and technicians who deal with the processes of electronic design, assembly, inspection, and repair. The IPC committee accepts that even though the document is not a complete recipe—refer to package supplier application notes and literature—it identifies many of the characteristics of robust and reliable assembly processes and provides guidance information to component suppliers regarding the issues being faced in the assembly processes. The IPC committee identifies two key issues in BTC: (1) providing the appropriate amount of solder paste; and (2) ensuring solder-joint reliability is met.

Providing an appropriate solder amount requires the effective pad design, which is becoming challenging since most current QFN packages have fine pitch pad design; therefore, it is very limited room available for the optimum pad configuration. The pad design should also consider the soldering reflow process since during assembly, liquid solder buoyancy of the individual small pads will compete with the larger heat-sink pad solder surface tension—the two competing forces if become unbalanced, they will cause to induce processing defects.

4.2 PCB Assembly Challenges

Industry and package suppliers have placed significant efforts to overcome the challenges of forming reliable solder joint for QFN package assemblies. This is because of the small no-lead termination surface area and the sole reliance on printed solder paste on the PCB surface. This is further complicated by the large thermal pad underneath the package and its proximity to the inner edges of the terminations. In addition to the consideration for the pad pattern design to eliminate some of the assembly problems, it is also special considerations are needed in stencil design and paste printing for both perimeter and thermal pads.

For the perimeter QFN termination pads, it is recommended that the standoff heights should be about 50 to 75 µm (0.002 to .003 in.) with good side solder fillets in order to achieve optimum and reliable solder joints [21]. Although a joint with no or low fillet, but a good standoff height, reduces the life, but still the residual life may be sufficient to meet the application requirement. The stencil aperture opening for perimeter pads should be designed to achieve a maximum paste release. This is typically accomplished with consideration of (1) Area Ratio (area of aperture opening/aperture wall area), and (2) Aspect Ratio (aperture width/ stencil thickness). This package supplier recommends that the stencil aperture should be 1:1 to PCB pad sizes with the stencil being laser cut and electro polished.

IPC 7093 recommends use of a 125 µm (0.005 in.) stencil thickness for $\leq$ 0.5 mm [0.02 in.] pitch or smaller and 150 µm [0.006 in.] stencil thickness for larger pitches. In some cases in order to get enough solder volume to mitigate gold embrittlement, the use of thicker stencil or overprinting may be considered. However, these methods for applying solder can lead to issues with solder paste release and bridging.

For an advanced array QFN [23], the author found that an optimum solder joint at each termination is achieved for a stencil design with 20% opening for heat-sink pad that is divided into a 2 × 2 matrix and a termination-opening ratio of 1 to 1.3 values. Experimental results showed that when the solder on the thermal pad exceeded 40%, the solder joint on the termination pad decreased [in size?]. The reason is that during solder reflow process, the surface tension of the molten solder on the heat-sink pad causes the array QFN package to be lifted. This results in a higher solder standoff on the terminations by pulling solder upward away from the side, which were to form solder fillet.

For the thermal pad, solder joint attachment should have minimal voids in order for the solder to effectively remove the heat from the die within the package and enhance electrical performance. Voids should be minimized since voids-free solder may not be possible because of presence of thermal vias and the existence of a large thermal pad. Also, out gassing occurs during the reflow process, and this

may cause defects (splatter and solder balling) if the solder paste coverage is large. The package supplier recommends use of smaller multiple openings for the thermal pad solder paste printing rather than a large opening. This result in 50% to 80% solder paste coverage. Figure 4-2 [13] shows a few options to achieve these levels of coverage. For an optimum paste release, the area and aspect ratios should be greater than 0.66 and 1.5, respectively. Other package suppliers may recommend different pad opening sizes for the stencil design depending on heat-sink and termination pad configurations.

IPC7093 discusses that the standoff height varies by the amount of solder that wets or flow into the plate through hole (PTH) via. The encroached via provides and easy path for solder to flow into the PTH and decreases package standoff height while plugged via impedes the flow. IPC recommends achieving 50 µm, thick solder joints and solder paste coverage of at least 50% for plugged via types and 75% for encroached via types.

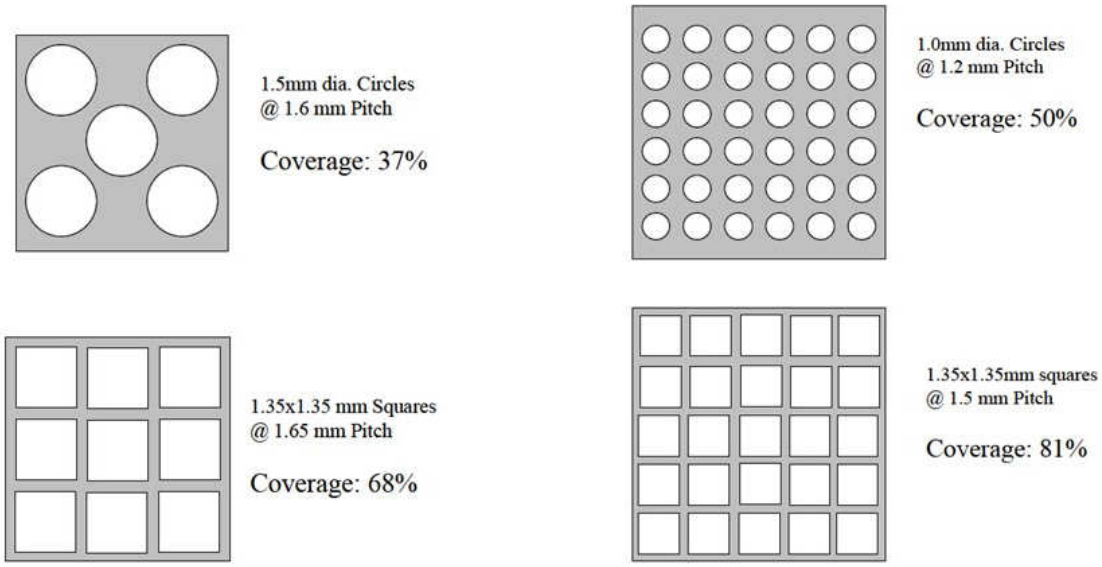

Figure 4-2. Thermal Pad Stencil Designs for 7 x 7 and 10 x 10 mm MLF® Packages [13].

4.3 X-ray for Solder-Joint Integrity and Voids

X-ray transmission radiography is an inspection technique in which X radiation passes through a specimen to produce a shadow image of its internal structure. X-ray radiography, in its static film version, was for decades a common nondestructive evaluation technique for electronics parts and hybrid electronics. For example, MIL-STD-883 once defined the X-ray feature requirements for small-scale electronic devices. Real-time X-ray detection systems, which replaced film radiography, are now widely used to define features and select the areas of interest for further evaluation. With the advancement of microelectronics with much smaller feature sizes, real-time X-ray has now become a necessity for inspecting and detecting fine and hidden features of electronic packages and assemblies. Magnifications of 1000× are now obtainable from commercially available equipment.

Figure 4-3 compares visual and X-ray inspection approaches for defect detection, especially for solder-joint interconnections. X-ray is specifically useful for features such as package internal wire bond anomalies, assembly solder-joint voids, bridges, missing elements, and geometric changes in feature sizes. In other cases, visual inspection is far superior to X-ray detection for solder-joint defects, including dewetting, microcracks, and “cold and disturb” anomalies. It is therefore critical to evaluate the limitations of various types of X-ray systems for detecting damage and cracking and for inspecting hidden solder joints. Ideally, a combination of various inspection techniques may be performed in order to assure quality at part, package, and system levels.

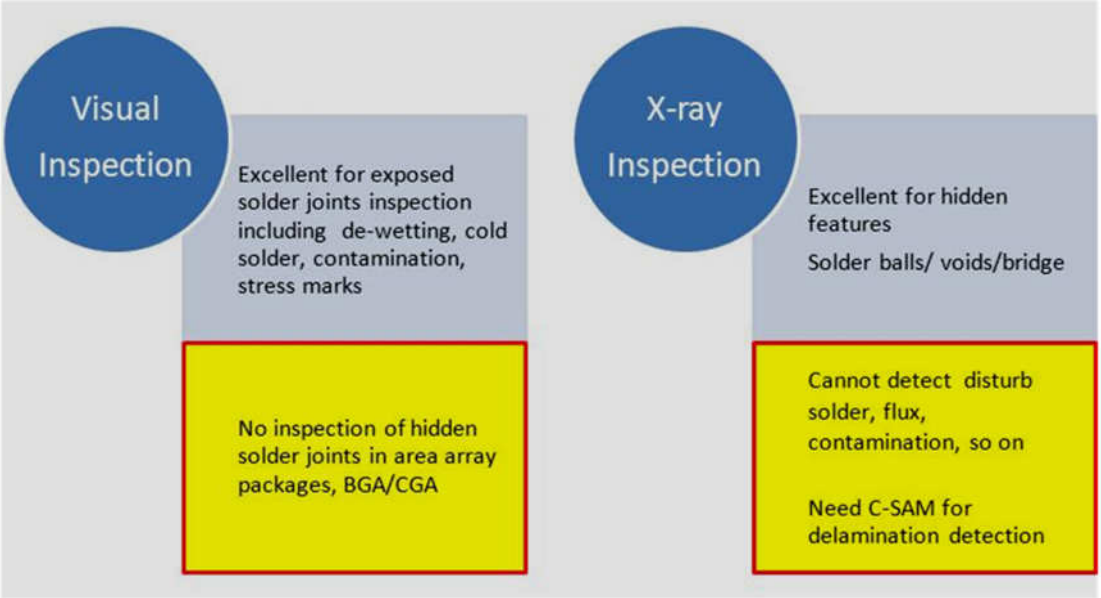

Figure 4-3. Strengths and weaknesses of using X-ray vs. visual inspection to detect key solder-joint defects.

Voids within solder joints under the QFN exposed thermal pad can have an adverse effect not only on thermal performance, but more importantly on high speed and RF performances. These voids increase the current path of the circuit. Generally, the maximum size for a void should be less than the via pitch within the plane to assure effectiveness of each via as heat dissipation.

With regards to the effect of voids on QFN, it is predicted from thermal simulation(see Figure 4-4) that smaller multiple voids in thermal pad up to 50% of the pad area do not affect thermal performance It is also stated that the voids in thermal pad region do not impact the reliability of perimeter solder joints[13,22]. Large voids, however, should be avoided by masking thermal vias to prevent solder wicking inside the via during reflow. Methods of masking includes (1) via tenting (from top or bottom side) using dry film solder mask, (2) via plugging with liquid photoimageable (LPI) solder mask from the bottom side, and (3) via encroaching.

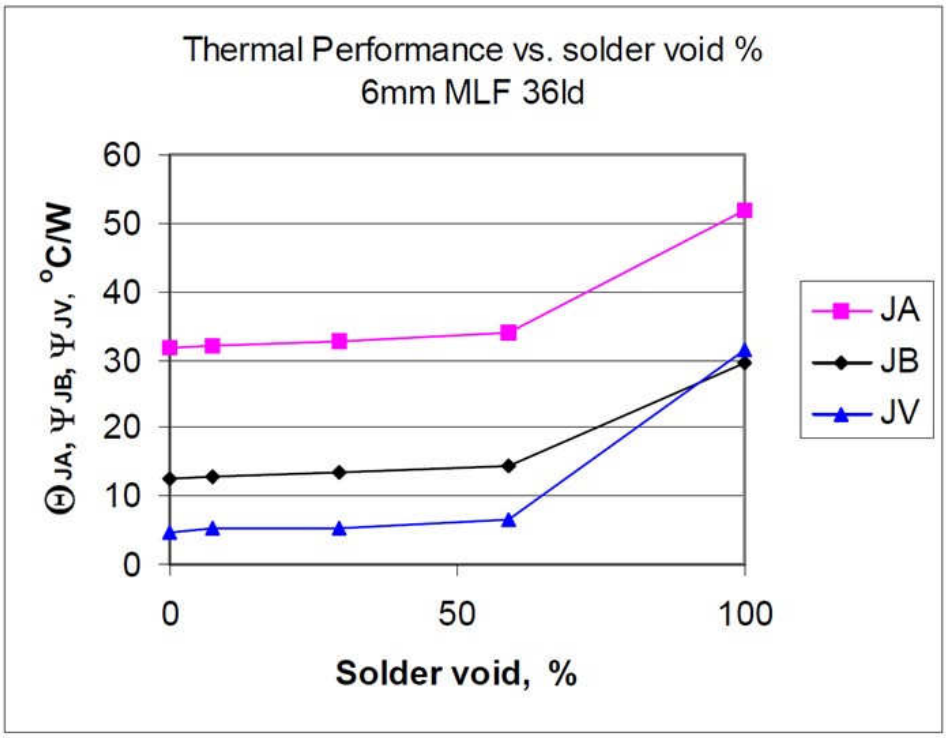

Figure 4-4. Effect of Voids on Thermal Performance [13, 22].

5. LEADLESS ASSEMBLY RELIABILITY

For low volume and high-reliability applications, the use of QFN package should be concentrate on understanding key parameters affecting long-term reliability and workmanship defects with a potential of a latent failure. In contrast to portable electronics which cost and miniaturization are key drives for the development of QFNs, the cost advantages become negligible in the overall system cost for use in a high-reliability application. The key motive for their use in such applications is their high-frequency functional advantages. Therefore, in order to achieve the highest assembly reliability with the lowest risk of insertion, it is required to perform optimization in board design, process, and testing to meet the stringent requirements. The following sections present key parameters that affect reliability of conventional and advanced QFN package assemblies.

5.1 Assembly Reliability of Conventional QFN

In a 2003 paper [21], guidelines were provided for in-board design and surface mount of MLF package based on extensive surface mount experimental test data. The authors also presented accelerated temperature cycling reliability test data for different material sets, various body/die sizes, temperature cycle conditions and board thickness. For example, it was shown that the die size within the package can have significant effect on the board level reliability (see Figure5-1]. The curve shows the data for the first cycles-to-failures vs die-to-package ratio which are normalized for the same test condition and board thickness using a relevant acceleration factor for a variable. It is apparent that the life can be very low if the die over the package size ratio is very high and the life increases non-linearly for a lower value of this ratio.

The effect of package land size was evaluated by using 0.5-mm (0.020 in) pitch for a 48-termination package and 0.8-mm for a 28 termination package. This resulted in land size of 0.23x0.4-mm and 0.28x0.6-mm, respectively. The area ratio become 1.82 which is equivalent to a 2X improvement in fatigue life based on the Weibull cycles-to-failure data. It was postulated that the larger land resulted in a wider and a longer solder joints, and thus a longer path for the crack propagation before a complete separation. The effect of PCB thickness was as expected, reliability decreased with an increase in thickness. The solder-joint reliability reduced by about 33% for the 1.6-mm thick board in comparison to the 0.8-mm thick for the 10-mm 68 lead QFNs assemblies.

Even though a significant effect of die-to-package on reliability is apparent, especially for the ratio greater than 70%, the authors suggested that reliability might be sufficient for most handheld and consumer electronic applications. The reliability might not be sufficient; however, for some other applications such as automotive and network hardware. Improvement approaches were recommended included: (1) increase the standoff height and (2) change solder fillet formation. Increase in standoff was accomplished by implementing a thicker lead frame on the package or the “Bumped MLF”. The resulting bump height was as much as 100 µm (4-mils) underside, which in turn results in increased standoff (joint thickness) by100 µm (4 mils). Final element analysis (FEA) showed a 2X improvement in reliability which agreed with the results which also showed about a 2X improvement in board level reliability (see Figure 5-2)

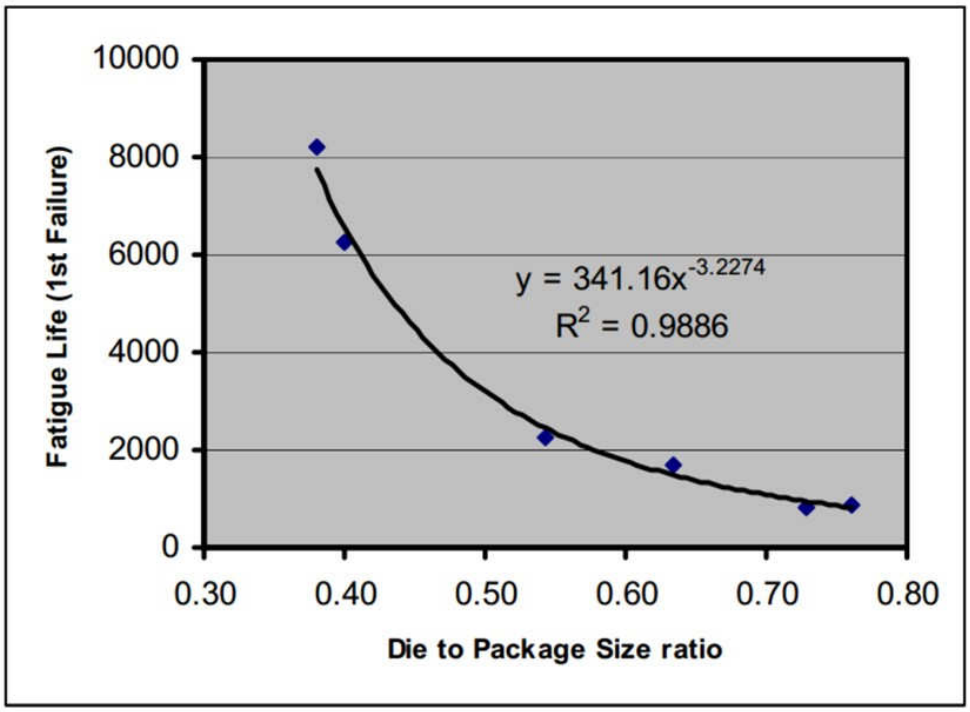

Figure 5-1. Effect of Die to Package ratio on board level reliability [21].

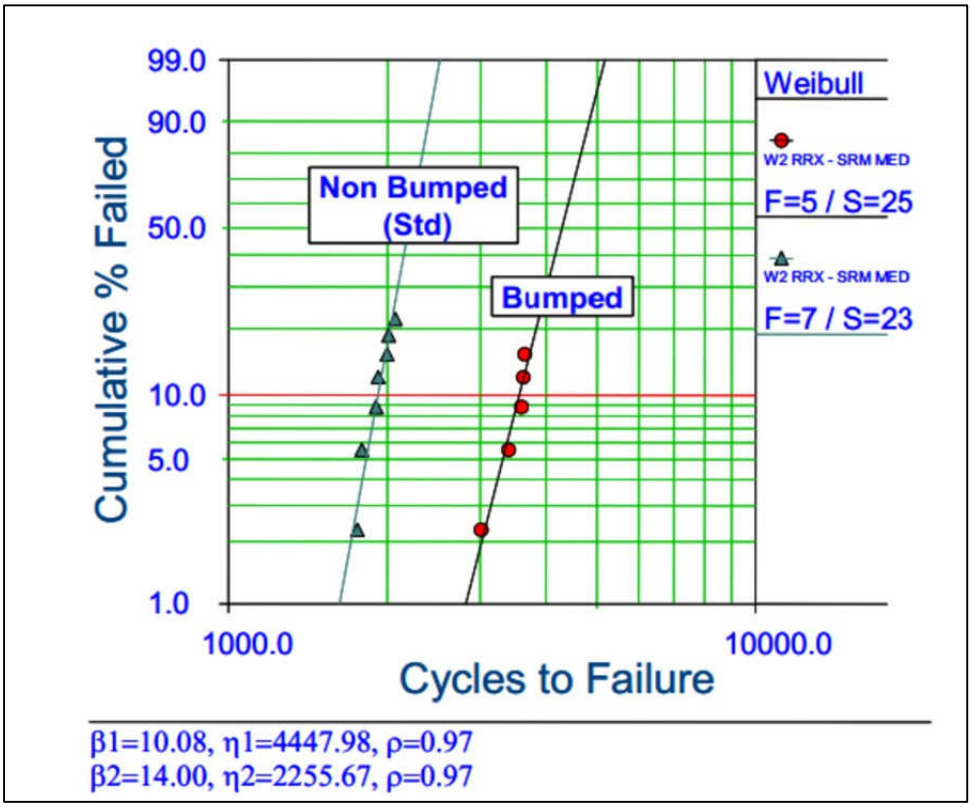

Figure 5-2. Weibull plot showing the effect of bumping the package lands. Advanced QFN [21].

In another 2003 paper [25], the authors presented a comprehensive detailed solder-joint fatigue testing with models and life prediction for QFN assemblies. Design analyses were performed to establish the effects of package geometry, material properties, and thermal cycling test condition. The authors concluded that the relative fatigue life predictions were in agreement with the test results.

It was shown that solder-joint reliability are improved for smaller package size, more center pad soldering, smaller die size, thinner die, bigger die pad size, thinner board, longer termination length/width, smaller pitch, higher solder standoff, better solder fillet, higher mold compound CTE, and smaller temperature range of thermal cycling test. However, the effects of land size, mold compound modulus, and die attach material are found to be insignificant.

Thermal cycle characterization of QFN on thicker PCBs (2.36-mm (0.093 in) and 3.17 mm (0.125 in)) as well as applicability of simple life projection model—Coffin-Manson—were the subject of a more recent study [26]. Both tin-lead and Pb-free solders were evaluated. Figure 5-3 shows the Weibull plots generated by the authors based on their test results (0º/100ºC and -40º/125ºC) for both SnPb and SnAgCu solder joints for the 10-mm 68 termination QFN package assembled onto a 2.36 mm (0.093 in) thick board.

The characteristics cycles-to-failure (0º/100ºC cycle) for SnPb and SnAgCu were about the same (3521 vs 3683 cycles); however, under the -40º/125ºC test condition, the SnAgCu solder joints had 26% shorter characteristic life cycles than SnPb solder joints. For the 3.17-mm (0.125 in) thick board and 0º/100ºC cycles, the characteristic life cycles decreased by 30% for SnPb and by 50% for SnAgCu; the decreases were about 20% for both solder joints under -40º/125ºC thermal cycling tests.

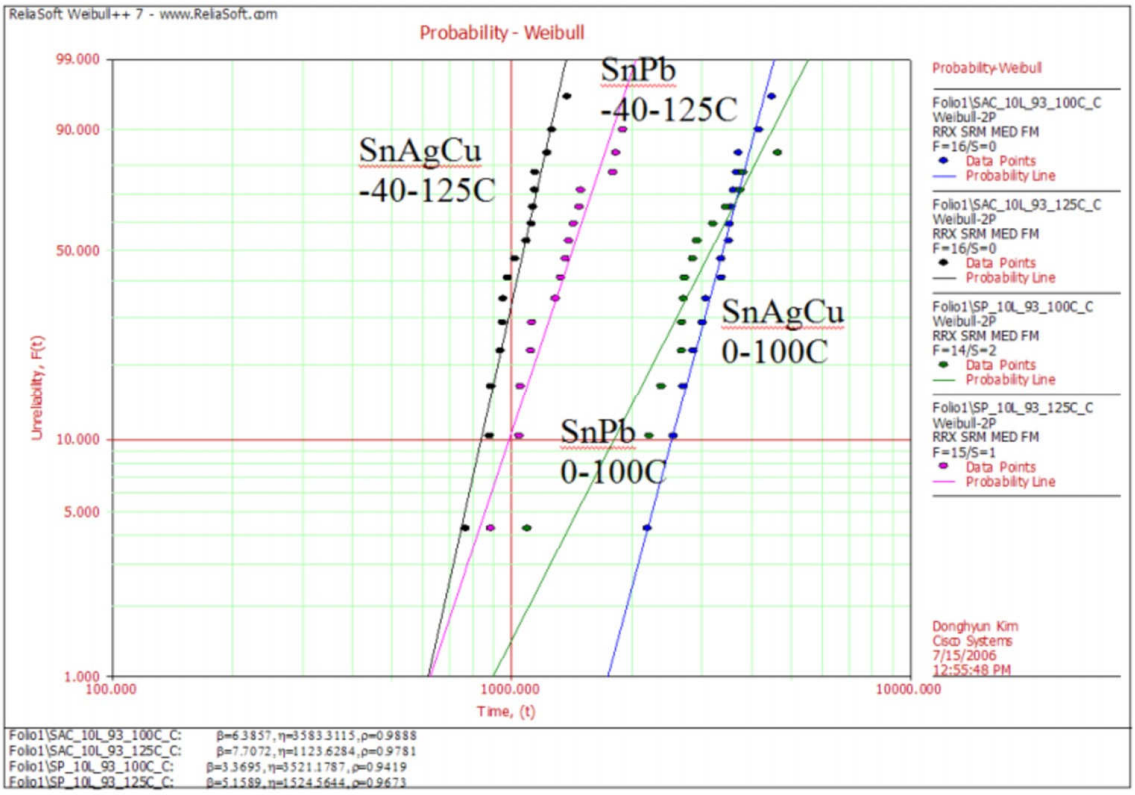

Figure 5-3. Weibull of SnPb and SnAgCu solder joints in 10mm 68 lead QFNs on 93mils thick boards, thermal-cycled at 0-100ºC and -40º-125ºC test conditions [25].

These authors also showed the importance of die-to-package ratio on solder-joint reliability. When die size increased from 3.7-mm to 4.8-mm in the 7-mm 48 lead QFNs, it was found that the board level reliability wad reduced by about 50%. The board level reliability decreased by about 30-50%.when the die size increased from 2.1-mm to 3.2-mm in the 5-mm 32 lead QFNs.

The authors use the Coffin-Manson relationship to project the life for QFN assemblies (SnPb or SnAgCu) under different operating thermal cycle conditions (see Figure5-4). The maximum operating temperature is assumed to vary while the lowest temperature was set as 0ºC. This plot shows the SnAgCu solder joint has about 2X larger acceleration factor (AF) than that for the SnPb solder joint. The error% in AF prediction is found to be within ±66%.

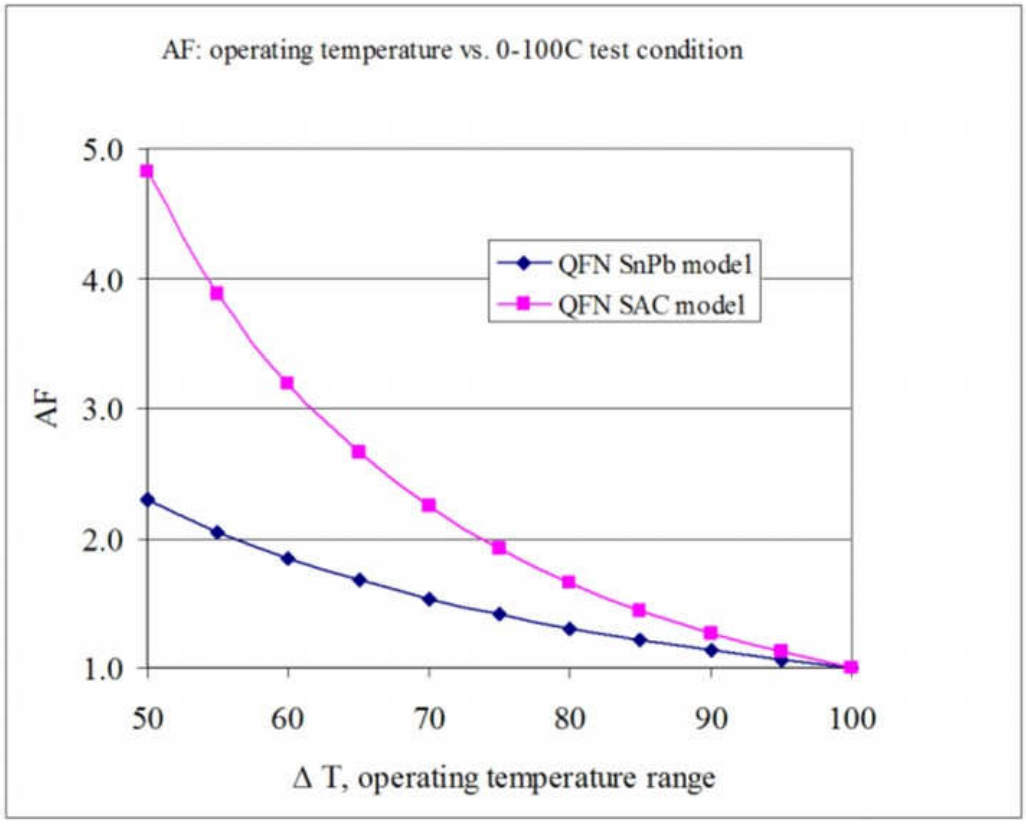

Figure 5-4. Acceleration factor comparison in Coffin-Manson type model for QFN: SnPb vs. SnAgCu [25].

Recently, modeling analyses were performed [27] to compare behavior of conventional and dual-row QFN (DRQFN) package assemblies under thermal conditions and warpage performance effects on board level solder-joint reliability. It was shown that conventional QFN had slightly better thermal performance than DRQFN and that the critical solder joint is at the package corner and crack is likely to occur along the termination and solder interface for both packages. The board level solder-joint fatigue life (-40º/125ºC) of conventional QFN is about the same as DRQFN (2099 vs 1817 cycles). In the follow-on paper published in 2013 [28], design of experiment (DOE) modeling was used to determine the key reliability factors for a multi-row QFN (MRQN) packages. The key factors shown to be the CTE of molding compound, the height of solder joint and the CTE of PCB. When all these improvement factors were considered in the modeling design, the thermal cycle projected to increase from 677 to 4165 cycles (-40º/125ºC), a factor of about 5.4 times.

Even though the impact of conformal coating and potting was discussed for BTC/QFN assemblies, the authors [29] did not present any detail information on the test condition. It simply states that it is observed that BTC/QFN failures occurred very rapidly during temperature cycling (–40º/125ºC) with urethane based potting materials with all units failed at the sub 100 cycles. The packages had good quality joints with sufficient solder thickness 63 to 75 µm (0.0025 to 0.003) in standoff). The discussion further carried out based on common knowledge and modeling knowing the key effect of underfill and thick conformal coating known by industry. It is known that underfill is designed for improving resistance to mechanical loading including shock resistance.

It is also known that the use of underfill and thick conformal coating can greatly influence failure behavior under thermal cycling. Polymeric materials have glass transition temperature which their properties significantly changes beyond that temperature. During thermal cycling if underfill and coating materials pass through their Tgs, then, that causes potential problems. Conformal coating should not bridge between PCB and the component.

On warpage, the potting shrinkage considered the issue deemed the most damaging to BTC packages based on the model of deflection in a PCB. Similarly, modeling showed that QFN package also deforms due to potting compound, the warpage shown to be an order of magnitude higher for potted package at the corner solder joints. On solder stresses, it was noted very high stresses during the cold temperature dwell, again especially those in the corners.

5.2 Assembly Reliability of Advanced QFN

Array and advanced QFNs are the next generation of QFNs with multi-row terminations. A few published papers addressed this topic. Reliability information is just started being presented, especially for the PCB assembly.

For example, a comprehensive investigation was presented on advanced QFN package [23], which was performed both to optimize the array package, to define reliability approaches, and to determine assembly requirements. Regarding assembly and reliability, the author stated that careful consideration was given to stencil design since industry has established that the majority of solder-joint failures are due to printing process. IPC 7525 guideline is used to evaluate the effects of variable such as the die paddle opening, the termination aperture ratio, and the die pad segmentation. It was reported that the 3D X-ray inspection did not show sufficient resolution to examine the solder-joint coverage on interface between the copper and solder interface. The effect of solder coverage and other variables were deemed necessary to be determined by destructive cross-sectional analysis method. Based on extensive evaluation, the author recommends using a stencil design with 20% opening for the die pad and 2 × 2 matrix segmentation at a 1:1.3 termination aperture ratio.

For solder-joint reliability evaluation, the board level drop tests—applicable for the handheld condition—was carried out using a modified drop condition B of JESD22-B110 and daisy chain package and PCB had for monitoring drop cycles to failures. The Weibull plots of the board drop test results are shown in Figure5-5. The array QFN with a 20-µm anchor design (TV3) performed the best with the first failure observed at 161 drops. For this case, the ideal condition of solder-joint cracking was the key failure mechanism rather than the undesirable internal wire bond breakage as it was the case for the TV2. Comparison of three types of failure mechanisms are shown in Figure 5-6.

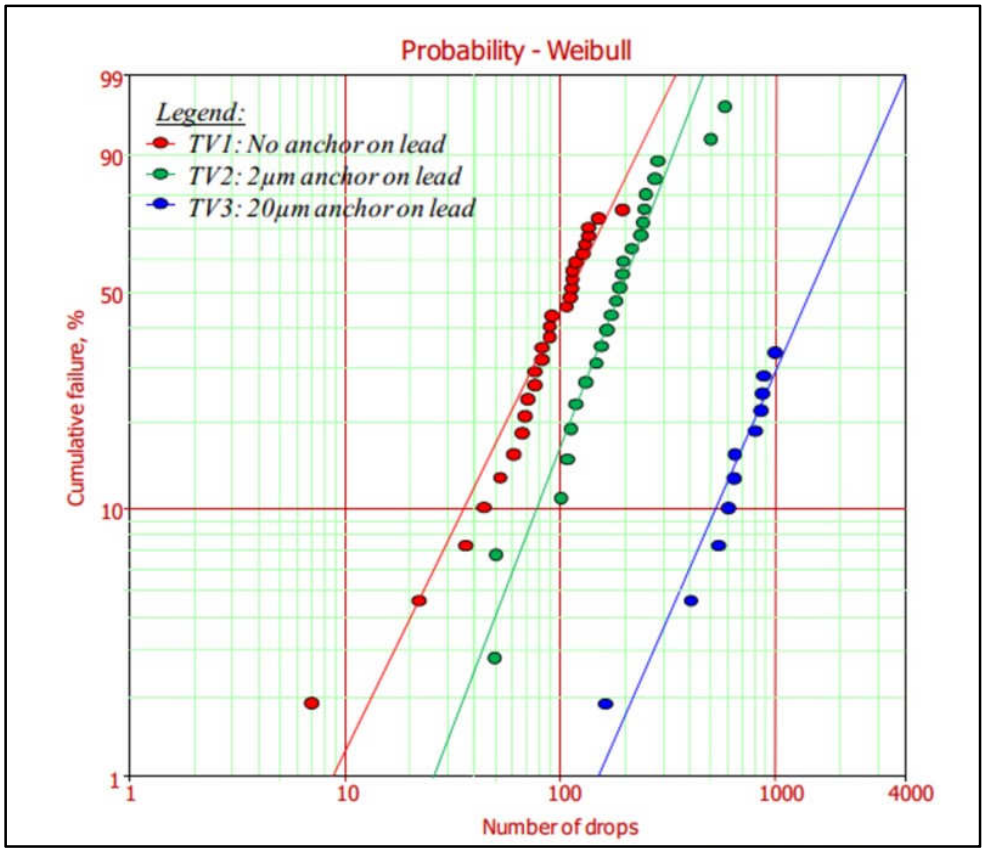

Figure 5-5. Weibull plots on comparison of TV1 (red), TV2 (dark green) and TV3 (blue) board level drop test performance. Test was stopped at completion of 1000 drops [23].

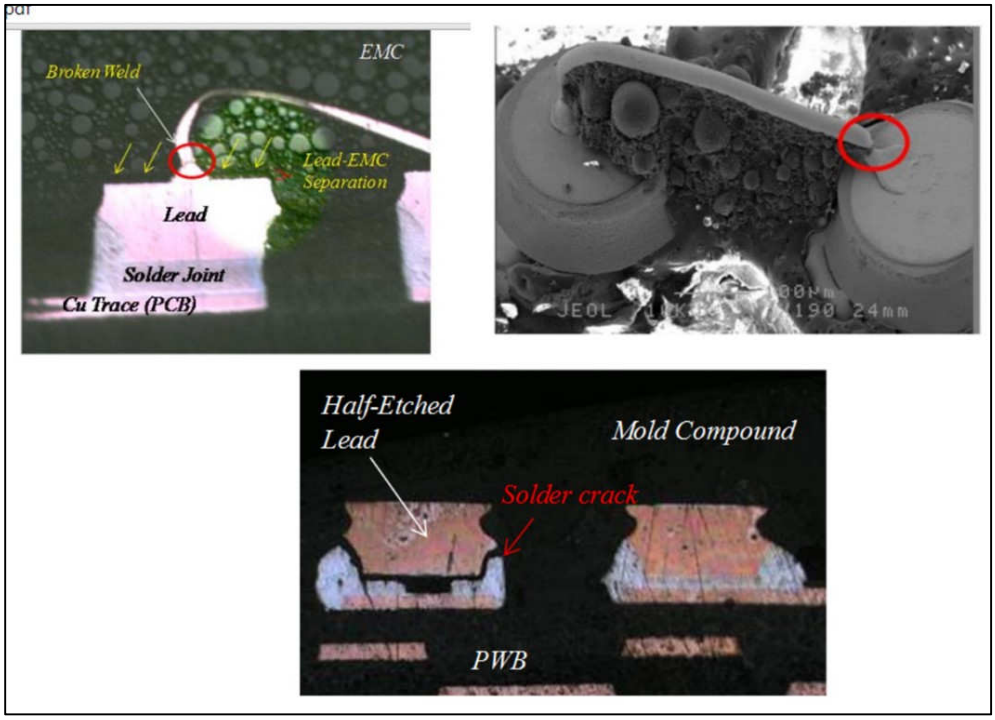

Figure 5-6. Failure detection by cross-sectioning: (1) TV1 after 7 drops with lead detachment (top left), (2) TV2 after 49 drops with broken weld (top right), and (3) TV3 after 161 drops with solder-joint failures (bottom) [23].

Board level reliability evaluation was also the subject of a recent high-density package (HDP) industry consortium user group [30]. The consortium tested over twenty QFN packages including: (1) packages with various body and sizes, (2) packages with various numbers of termination rows, (3) packages with various termination surface finishes, (4) packages with various terminal pitches, and (5) package assemblies evaluated under one temperature cycling range of 0 to 100ºC, but with the dwell times of 10 and 60 minutes.

A total of 17235 cycles were completed for the 10-minute dwell testing and 6000 cycles for the 60-minute dwells. A few QFN assemblies failed early in the sub-1000-cycle ranges revealing no apparent evidence for such early failures even though it was thought that isolated poor workmanship of solder joints might have been the key contributor. The Weibull plots were therefore produced with inclusion of data from early failures and without their inclusion. When early failure data were excluded, significant improvement was found correlating the failure points to the Weibull plots (see figure 5-7). The failure plots are for the 164 I/O, 0.5 mm pitch, dual-row QFN packages cycled under two dwells. The thermal cycle with 10-minute dwells showed larger cycles to failures compared to the 60-minute dwells, about 1.9-fold increase in lifetime.

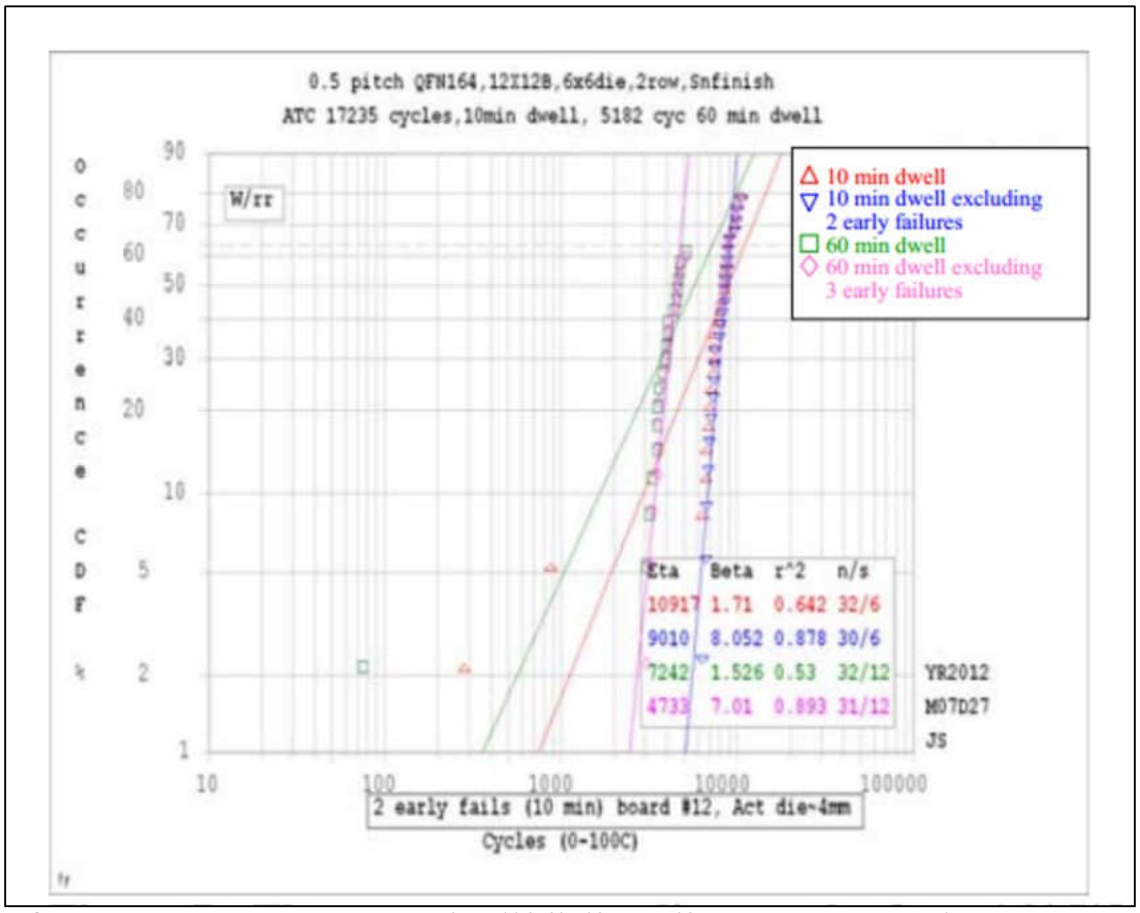

Figure 5-7. The temperature cycling results for a 164 I/O, 12 mm x 12 mm body size, dual row QFN. Die size was measured at 3.78 mm x 3.78 mm [30].

For other QFN package assemblies, a similar reduction in thermal cycle life due to the 60-minute dwells were observed even though the levels dependent on the package styles. For example, Figure 5-8 shows the Weibull plots for the largest QFN package with 236 I/O, 0.5-mm pitch, and 3-rows where its middle row was connected by via-in-pad technology. The impact of the 60-minute dwell is apparent with the changes in the fitted Weibull lines and their characteristic values.

The consortium presented optimization condition for the 164 I/O, dual-row, and 12-mm x 12-mm body QFN, it was concluded that the smaller the die size, the larger the pad size, and the larger volume solder fillets all cause to increased solder-joint fatigue life. On the other hand, for the 140 I/O QFN, an undersized pad coupled with the via-in-pad design on the SMT lands (and potentially with the NiPdAu lead frame finish) are the major contributors to the shortening of solder-joint fatigue life [see Figure 5-9]. In summary, solder-joint fatigue life of MRQFN, e.g., 236 I/O, can be become comparable to the level of fine-pitch BGA with an optimized PCB land pattern and a low ratio of die to body size.

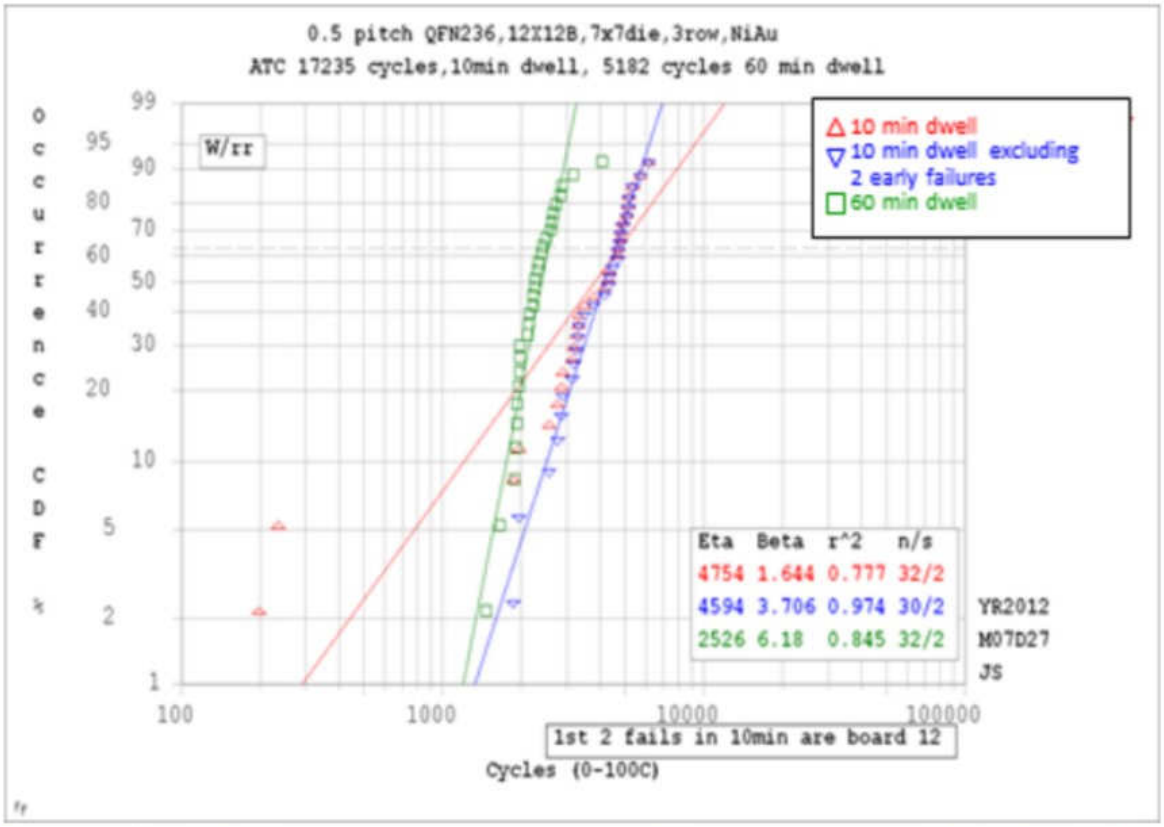

Figure 5-8. The temperature cycling test results for 236 I/O, 12 mm x 12 mm body size, NiAu lead frame finish, 3-row QFN [30].

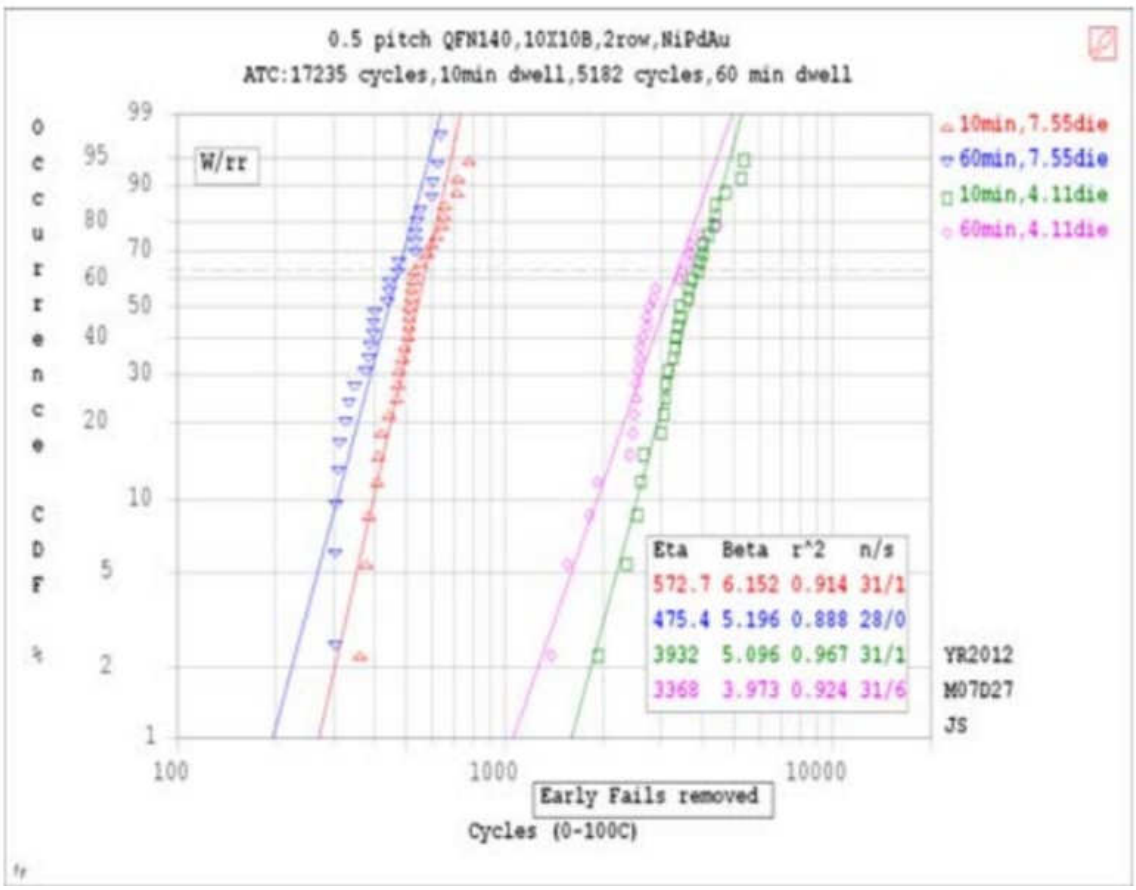

Figure 5-9. The temperature cycling testing results for the 140 I/O, 10 mm x 10 mm, NiPdAu lead frame finish, dual row QFN [30].

6. SUMMARY

This report reviewed literature on leadless packages which are near the die size similar to array CSPs. The report presented board design, manufacturing, and processing parameters and their effects on assembly reliability. Leadless packages are also known as quad flat no-lead (QFN) or the generic term of bottom termination components (BTCs). The BTCs were selected for literature surveying because of their significant growth, which is projected by the iNEMI roadmap, reduction in cost, and improvement in functionality, especially for use in high-radio frequency applications.

Design, assembly, and reliability data gathered for conventional leadless packages including QFN, dual-row/multi-row QFN (DRQFN/MRQFN), dual flat no lead (DFN), and land grid array (LGA). Similarly, when data were available, they were gathered for advanced QFN (aQFN) and array QFN packages. The aQFN packages are improved versions of conventional QFN with multiple-row terminals accommodating higher number of I/Os. The number of I/Os reaching to the level of CSP/FBGA packages with the advantage of lower cost and improved RF characteristics for potable and telecommunication applications. Key findings discussed in the report are summarized in the following list.

- It is projected that QFN packages grow at a rate of 15% compound average annual growth rate whereas single chip packages such as DiP show negative growth.
- It is categorized the BTCs into three key groups to better address the key design, assembly, and reliability issues associated with each category. These categories are: (1) conventional single/dual row QFNs, (2) advanced array QFNs, and (3) LGAs. The literature surveyed indicates a number of papers and a guideline document were published for conventional QFNs, but limited work was reported on array QFN and LGA packages.
- It is recommended for effective use of QFN packages to review the key important generic guidelines which are discussed in the IPC guidelines and specifications, e.g., IPC 7093, 7351, and 7525 along with the specific application notes generated by the package suppliers. Additional testing by user may be required to address issues associated with the use of specific design requirement and SMT equipment.
- It is reviewed the key parameters affecting solder-joint reliability for QFNs. The key parameters include solder standoff and fillet as well die-to-package ratio.
- It is highly recommended to not only continuously review emerging QFN packaging technologies, but also to test evaluate a number of the well-established packages to better understand nuances on assembly and reliability for effective implantation in low-volume and high-reliability environmental applications.

Understanding key technology development and characteristics of QFN and advanced QFN packaging technologies, assembly, quality assurance, and reliability are important in judicially selecting and narrowing the follow-up applicable technology, and quality assurance and reliability test methods in preparation for low-risk insertion into electronic systems for NASA use.

7. ACRONYMS AND ABBREVIATIONS

aQFN	advanced quad flat no-lead
ASIC	application-specific integrated circuit
BGA	ball grid array
BOK	body of knowledge
BTC	bottom termination component
CAAGR	compounded average annual growth rate
CGA	column grid array
CMOS	complementary metal oxide semiconductor
COB	chip-on-board
CSP	chip scale package
CTE	coefficient of thermal expansion
DCA	direct chip attachment
DFN	dual flat no-lead package
DiP	dual-in-line package
DOE	design of experiment
DRMLF	dual-row micro-lead frame
DRQFN	dual-row quad flat no-lead
EMS	electronics manufacturing services
FCBGA	flip-chip ball grid array
FCOB	flip chip on board
FEA	final element analysis
FPBGA	fine pitch ball grid array
HCTE	high coefficient of thermal expansion
HDP	high-density package
IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
iNEMI	International Electronics Manufacturing Initiative
I/O	input/output
IPC	Association Connecting Electronics Industries
ITRS	International Technology Roadmap for Semiconductors
JPL	Jet Propulsion Laboratory
KGD	known good die
LCC	leadless chip carrier
LGA	land grid array
LOC	lead on chip
MEMS	micro-electro-mechanical systems

MLF	micro lead frame
MRQFN	multi-row quad flat no-lead
MtM	more than Moore
NBA	no-bump array
NASA	national aeronautics and space administration
ODM	original design manufacturer
OEM	original equipment manufacturer
PBGA	plastic ball grid array
PCB	printed circuit board
PGA	pin grid array
PTH	plated through hole
PWB	printed wiring board
QFN	quad flat no-lead
RDL	redistribution layer
RF	radio frequency
RoHS	(European Union) restriction of hazardous substances
SIA	semiconductor industry association
SiP	system in package
SMT	surface mount technology
SO	small outline
SOC	small outline chip
SOT	small outline transistor
Tg	glass transition temperature
TQFN	thin quad flat no-lead
TSOP	thin small outline package
TSV	through silicon via
TV	test vehicle
USON	ultra-thin-small-outline
VQFN	very thin quad flat no-lead
WLP	wafer level package
WCSP	wafer level chip scale package
WLCSP	wafer-level chip-scale packaging
WLP	wafer level package

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