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Heat Sink Induced Thermomechanical Joint Strain in QFN Devices

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***Abstract*—A blade server system (BSS) utilizes voltage regulator modules (VRMs), in the form of quad flat no-lead (QFN) devices, to provide power distribution to various components on the system board. Depending on the power requirements of the circuit, these VRMs can be mounted as single devices or banked together. In addition, the power density of the VRM can be high enough to warrant heat dissipation through the use of a heat sink. Typically, at field conditions (FCs), the BSS are powered on and off up to four times per day, with their ambient temperature cycling between 25°C and 80°C. This cyclical temperature gradient drives inelastic strain in the solder joints due to the coefficient of thermal expansion (CTE) mismatch between the QFN and the circuit card. In addition, the heat sink, coupled with the QFN and the circuit card, can induce additional inelastic solder joint strain, resulting in early solder joint fatigue failure. To understand the effect of the heat sink mounting, a FEM (finite element model) of four QFNs mounted to a BSS circuit card was developed. The model was exercised to calculate the maximum strain energy in a critical joint due to cyclic strain, and the results were compared for a QFN with and without a heat sink. It was determined that the presence of the heat sink did contribute to higher strain energy and therefore could lead to earlier joint failure. Although the presence of the heat sink is required, careful design of the mounting should be employed to provide lateral slip, essentially decoupling the heat sink from the QFN joint strain. Details of the modeling and results, along with DIC (digital image correlation) measurements of heat sink lateral slip, are presented.**

***Keywords*—Heat sink mount, solder strain, lead-free solder, FEM modeling, thermal cycling**

Introduction

In modern electronic applications, electronic board assemblies are required to pass industry reliability tests and customer specifications. At the core of these reliability specifications are the solder interconnects (solder joints) that provide mechanical and electrical interoperability. The reliability of the devices requires the joints to survive thermal assembly processing, shock events resulting from shipping and handling, high and low cyclical vibration, and field-induced thermal cycling, all of which contribute to strain events that can individually or collectively lead to joint cracking and/or fatigue failure. Fig. 1 shows the typical thermal strain contributors incurred throughout the life of an electronic module. The box in Fig. 1 marked FC models the thermal-induced strain due to power on/off thermal cycling.

Recently, due to the ROHS (restrictions on hazardous substances) regulations on the use of tin-lead alloys as interconnects, the electronics industry has had to seek alternatives made from less hazardous metals. The solder metallurgy of choice to replace SnPb are alloys of tin-silver-copper, often referred to as SAC alloys (for SnAgCu). However, due to their lower ductility and higher stiffness, challenges in interconnect strain failures are being realized. Emerging as a low cost frontrunner for SAC is the alloy SAC305, which has a composition of 96.5% Sn, 3% Ag, and 0.5% Cu.

Another shift in modern electronic assemblies is the on board distribution of power levels driving various circuits. There is a growing use of QFN-based VRMs to regulate this discrete on board power delivery. These QFN devices, which are of fingernail scale, utilize a solder joint geometry that is paddle-shaped with a high planar to height aspect ratio. Unlike a typical barrel-shaped solder connection, these joints experience higher strain during thermal cycling, which can lead to joint failure.

In addition, due to the QFN high heat load, heat sinks are often employed to dissipate thermal energy. Fig. 2a shows an in situ picture of four in-line QFN devices on a circuit board with a heat sink and thermal interface material. Fig. 2b shows a side view schematic of the same structure. Unfortunately, certain methods employed to mount the heat sinks securely to the board assemblies can contribute to increased strain loading on the solder interconnects. An example of this mounting is a low cost in-line riveting process that rigidly constrains the heat sink to the PCB. A rigidly attached heat sink can increase the amount of solder strain realized during thermal cycling, which is a cause of early failure. This paper presents an FEM (finite element model) exercise to understand the strain energy resulting from the heat sink method of assembly. The model uses a power on/off field condition (FC) to drive the thermal strain energy, resulting from the CTE mismatch of the various components. The FC used consisted of four cycles per day with 270 min dwell times at hot (75°C) and cold (25°C) temperatures with linear ramp times of 45 min.

Material Properties

To model the thermal mechanics of the system, the elastic-plastic modulus and creep properties of the solder are required

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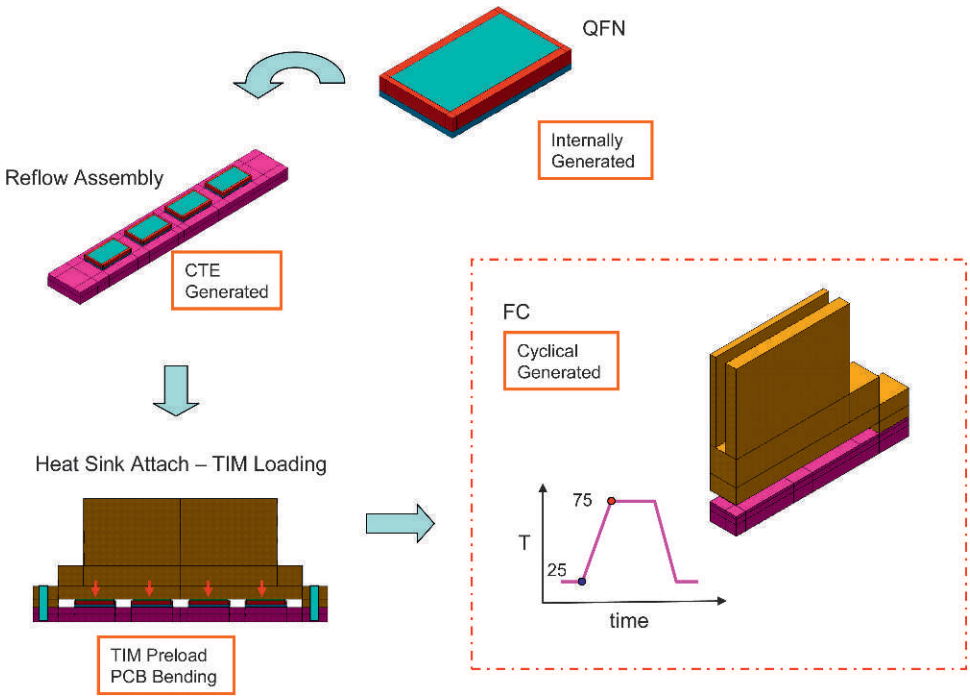

Fig. 1. Process-induced strain contributors.

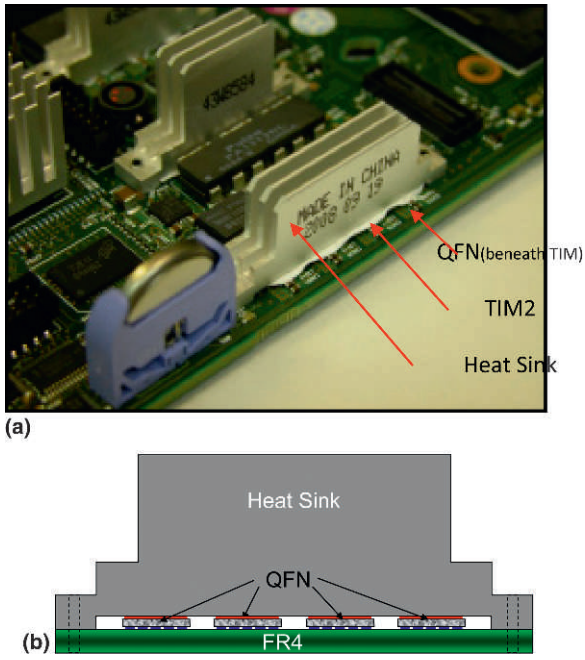

Fig. 2. (a) Heat sink mounted over four QFN modules. (b) Schematic showing side view of heat sink mounted over four QFN modules.

in addition to the elastic properties of the QFN and FR4 printed circuit board. Table I reports the material properties used in the numerical analysis.

In the case of the FR4 circuit board, a sample section representing the footprint of the heat sink was extracted and the effective storage modulus and CTE were measured using a DMA (dynamic mechanical analyzer) and a TMA (thermomechanical analyzer). A single sample was measured under the target area and was assumed to be sufficient for modeling purposes, as board processing should produce negligible variability. Fig. 3 shows the results of the DMA modulus measurement.

For the QFN, a detailed understanding of the assembly was acquired and material properties were assigned. In one region of the QFN, effective material properties of the Cu-Fe-Pb frame and surrounding polymer encapsulation were derived based on volumetric proportions. For effective E_x and E_z, a parallel mixing rule was employed, whereas for E_y, a series mixing rule was employed. Also, the overall CTE of the QFN device was measured using the average of three samples measured on the TMA and correlated to a discrete QFN FEM model. Model results were comparable to the measured results and the discrete material definition was utilized in subsequent modeling exercises. The TIM2 material was a low-cost material that allows lateral compliance without contributing to joint strain. It is applied to the top of the QFN in direct contact with the die surface and with the underside of the heat sink. No other TIMs were considered.

A time hardening creep model for SAC305 was used to analyze the creep behavior of the solder interconnects. ANSYS FEA[1] software incorporates the constituent model into the analysis using seven constants reported in Table II.

In previous modeling of SnPb solder creep, the ANAND [2] viscoplastic model has been widely used, as well as other constitutive models. However, these models may not capture

[1]ANSYS is a trademark of ANSYS, Inc.

Table I
Material Properties and Dimensions

Material	Dimensions (mm)	E (GPa)	Poisson	CTE (ppm)
Silicon die	6 L × 3.25 W × 0.65 H	130	0.22	3
Lead frame CuFe (CDA194)	singulated structure under die	121	0.33	16.3
Sumitomo EME-G770HCD	6.5 L × 4 W × 0.65 H	29	0.3	7
Estimated smeared Sumitomo/CuFe QFN section	Modulus derived from mixing rules 0.28 H	E_x: 47; G_{xy}: 28.8 E_y: 75; G_{yz}: 18 E_z: 75; G_{xz}: 28.8	0.3	10.5 TMA measured QFN
Circuit board (FR4)	4 QFN bank Footprint under heat sink Free height 0.51 mm (0.02 in.)	Measured temperature dependent	0.35	x: 17.4; y: 18.5; z: 18.5
Thermagon T_putty	Working height 50% compression	0.0014 estimated from measured compression data	0.4 estimated	92
Heat sink aluminum 6063 T5	46.5 L ×7 W × 15.8 H	68.9	0.33	23.4
SAC305 pads	0.5-1.9 L (variable) × 0.25 W × 0.1 H	Purdue data	0.33	22.86

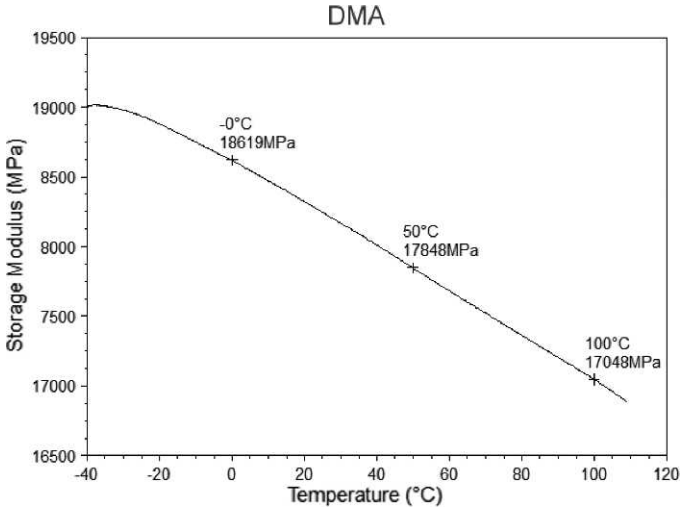

Fig. 3. PCB modulus measurement.

the primary creep contribution shown in the curve in Fig. 4. In the ANAND model, the primary creep contribution was considered to be reached instantaneously and for this reason was not selected for this study. With the emergence of SAC alloys, it has been shown that primary creep is not negligible and should be included in the calculation [3]. The time hardening creep model includes both the primary and secondary creep components [1, 3]. Eq. (1) shows the constituent relationship between creep and the time and temperature components of stress.

$$\varepsilon_{creep} = C_1\,\sigma^{C_2}\,t^{C_3+1}\,e^{-C_4/T}/(C_3+1) + C_5\,\sigma^{C_6}\,t\,e^{-C_7/T} \quad (1)$$

(Time, Temperature; Strain, Stress)

Modeling

A full linear model of the four QFNs, heat sink, and board was developed and exercised from a stress-free condition at 25°C to 0°C and then to 125°C, which is a typical ATC (accelerated thermal cycle) used in reliability testing. The results were probed to determine regions of highest strain, and possible model reduction. The effect of potential solder joint height process variability was not considered in the modeling effort. Based on the linear model results, a quarter symmetry model was developed, regions of higher strain were refined with a higher element count, and the inelastic and creep material properties for SAC305 were introduced. The resulting mesh used for the nonlinear analysis is shown in Fig. 5. The quarter symmetry model was first run, without creep properties, for one ATC cycle to evaluate the displacement in the system and the total strain realized in a critical joint. This critical joint, which we call the DNP (distance from neutral point) is illustrated in Fig. 6, which is a bottom view of the QFN. The model was exercised for two boundary conditions, one with the heat sink rigidly mounted, which simulated the riveted assembly (no slip condition), and the other simulating frictionless contact or lateral slip condition at the heat sink/PCB interface.

To evaluate the effects of creep on the interconnects, the full quarter symmetry model was run with the time hardening creep materials factored in. The model was cycled for four FC cycles with the heat sink rigidly attached and max creep strain energy density was recorded for the DNP interconnect for the last cycle. The creep strain energy density [4, 5] can be directly output from ANSYS and is recognized in the industry as a method to compare solder interconnect work done for various cyclical loading conditions. In this exercise, the riveted heat sink condition is compared with the system without a heat sink, which is the ultimate condition for a heat sink mounted with lateral slip enabled at the heat sink/PCB interface.

Measurements

Measurements of the in situ mounted system provided valuable insight into the thermal coupling of the riveted heat sink. Although it was assumed that a rigid connection was made by the rivets, DIC measurement revealed that there was some slip in the system. Even though slip is desirable to decouple thermal interconnect strain, protection against linear and rotational shock must be ensured.

Fig. 7 gives the measurement results of the riveted system at 100°C. The dashed lines indicate the rivet position in the PCB board. The solid short black and blue line above and

Table II
Time Hardening Creep Model [1]

	C_1	C_2	C_3+1	C_4	C_5	C_6	C_7
Sn3.8Ag0.7Cu	1.134E−4	4.577	0.5136	4886.5	5.05E−7	11.521	2.26E+4
Sn1.0Ag0.5Cu	1.533E−5	1.542	0.3002	2.77.2	1.36E−6	14.176	1.55E+4
Sn3.0Ag0.5Cu	2.244 E−4	0.613	0.4722	531.211	2.32E−4	1.0268	1.5509E+4

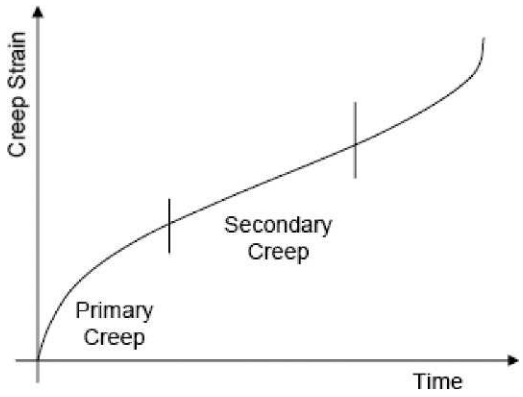

Fig. 4. Creep curve.

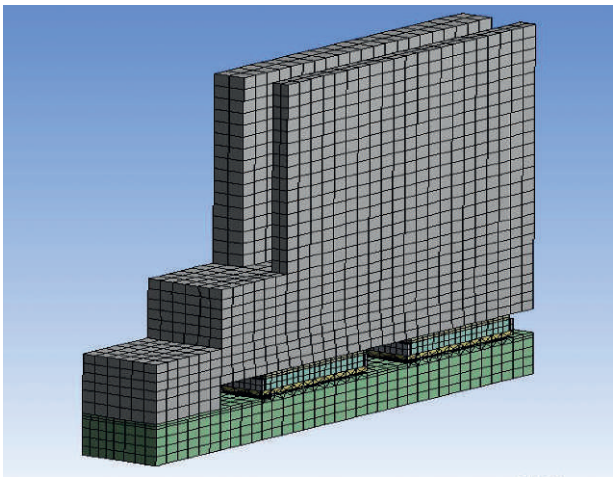

Fig. 5. Mesh on quarter symmetry model.

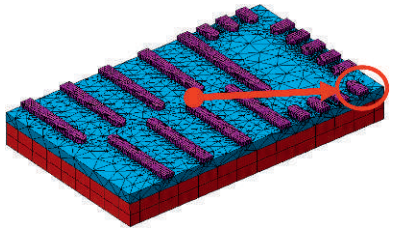

Fig. 6. Bottom view of QFN-DNP interconnect.

below the dashed lines indicate the position of rivets in the heat sink. The total in-line displacement of 20 μm is what is expected by eq. (1) wherein ΔL (19 μm) is thermal expansion; L (43 mm) is the distance between rivets; Δa (6 ppm) is the CTE difference between the PCB and the heat sink, and ΔT (75°C) is the temperature difference between a stress free state at 25°C and a measured temperature of 100°C.

$$\Delta L = L \times \Delta a \times \Delta T \tag{2}$$

Results

Figs. 8a and 8b show the deformation contour plots for the no slip and slip conditions (excluding creep), respectively, for 100°C. We can see from the plot's circled area that the no slip condition drives a stronger coupling of the PCB, which is expected. However, it cannot be determined from these plots whether the coupling of the heat sink increases or reduces the strain in the solder interconnects.

The results for the total strain in the DNP joint present a clearer picture regarding heat sink coupling and subsequent strain increase. Maximum total strain for the no slip condition (Fig. 9) is 7.2% versus 5.8% for the slip condition. Therefore, the presence of heat increases the total strain in the DNP solder interconnect by approximately 25%.

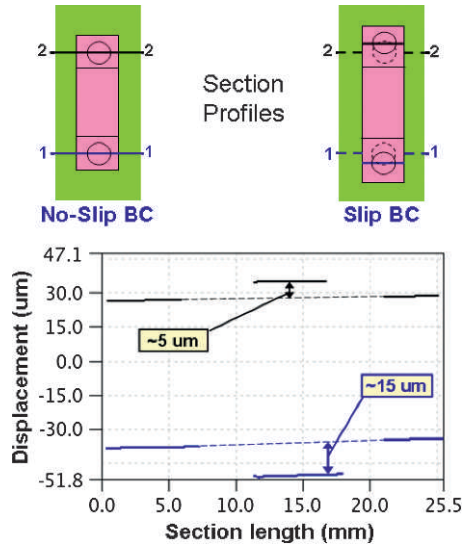

Fig. 7. DIC in-line slip measurement (blue line = 1-1).

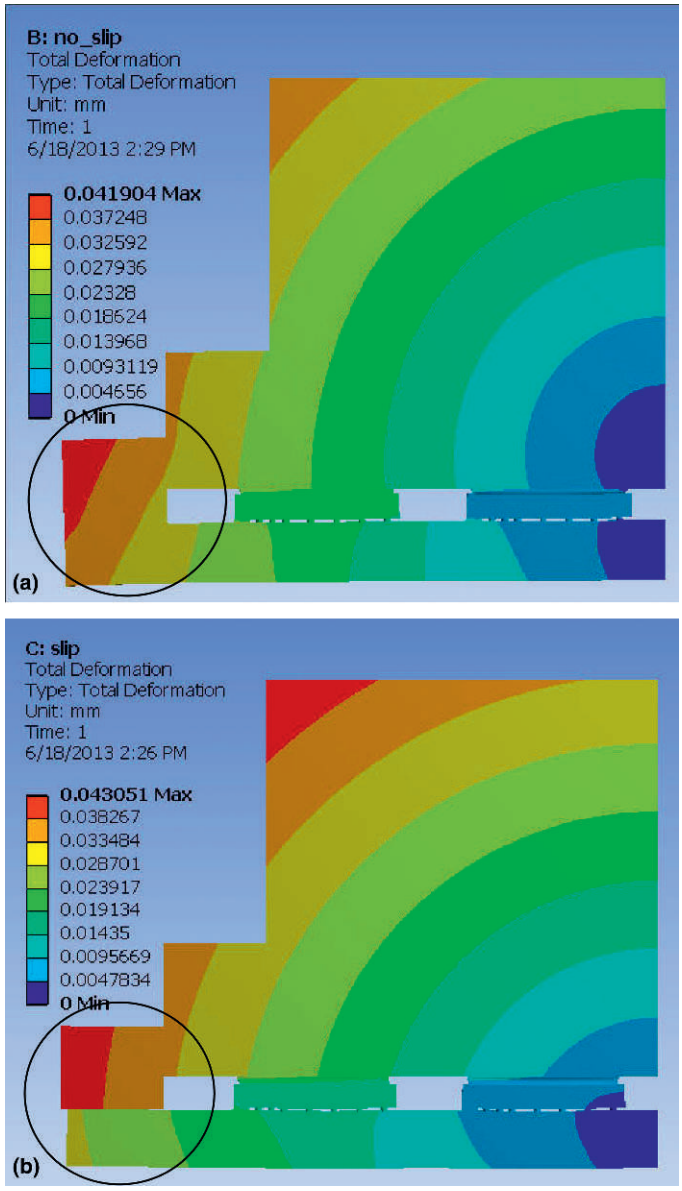

Fig. 8. (a) No slip, total deformation. (b) Slip, total deformation.

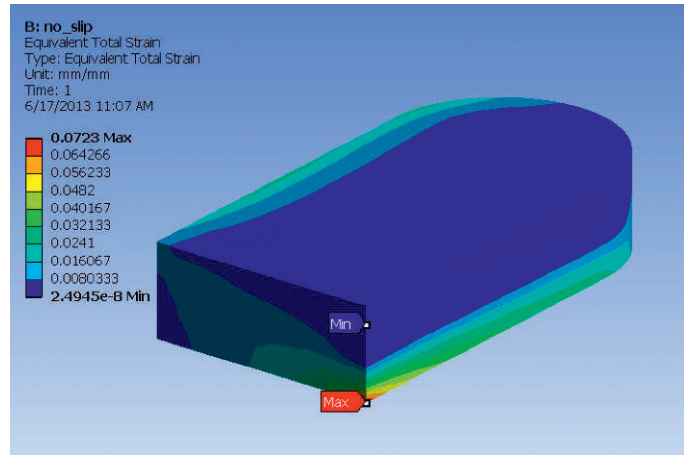

Fig. 9. No slip, total strain.

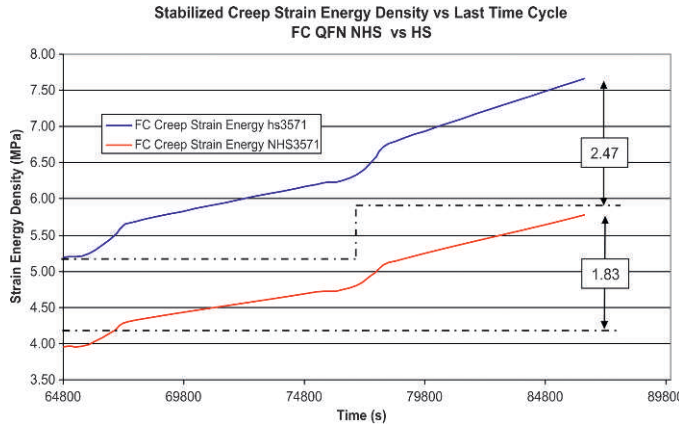

Fig. 10. Field condition strain energy density.

When we include creep strain in the models and exercise them through four FC cycles, we can extract the stabilized strain energy density (work) for the last cycle and compare the results. As previously mentioned, we compared the rigidly mounted heat sink condition to no heat sink, which represents the idealized lateral slip condition. The graph in Fig. 10 is a plot of the delta work done for the last cycle in the DNP interconnect for both conditions. Comparing the results from the two cases, we see that the presence of the heat sink increases the work done by approximately 35% $[= 100(2.47 - 2.83)/1.83]$.

To mitigate the strain induced from the coupling of the heat sink, and thus improve cyclical life, it is essential to consider the heat sink mounting technique. Factors to consider include heat dissipation, shock, and vibration, when designing a heat sink that provides lateral slip to reduce strain coupling in the solder interconnects. Fig. 11 shows an in-line design (two mounting points) that can satisfy these requirements.

In this design methodology, slip is allowed in the in-line direction by virtue of the slot. A two or four leg split post, which can be fixed to the PCB, can be designed to eliminate radial clearance while providing the necessary stiffness to resist shock and vibration. The TIM can be functionally held between QFN and heat sink with the preload washer and retainer. The concept of providing lateral slip to heat sink mounting is not relegated to QFN type devices but can be extended to any high power device. For example, Fig. 12 is a schematic which illustrates a method to provide compliance along the thermal expansion direction (i.e., diagonally) for a four point heat sink mounted device.

Thermally induced expansion is a radially driven coupling in a four point mounting system. As can be seen in Fig. 12, a soft axis is provided normal to the radial direction to provide for differences in expansion. This soft axis can be implemented in the form of a flexural design as shown in Fig. 13.

Conclusion

High powered integrated modules are increasingly being used on PCBs in electronic systems. These modules are

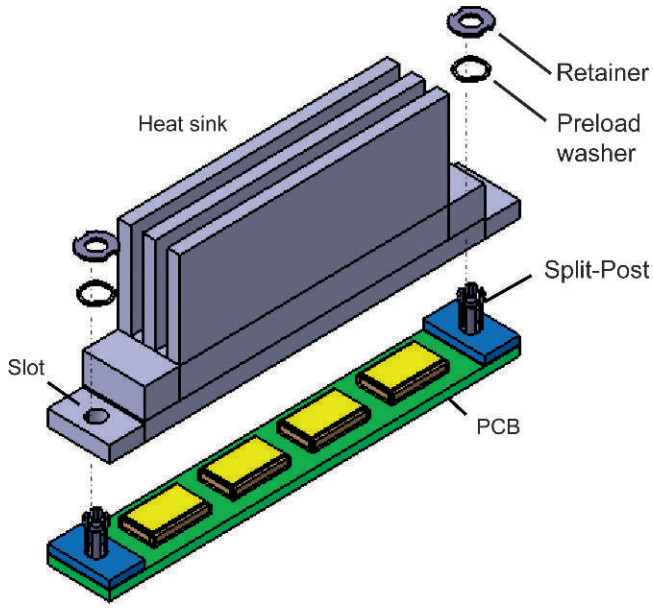

Fig. 11. In-line heat sink lateral slip mounting concept.

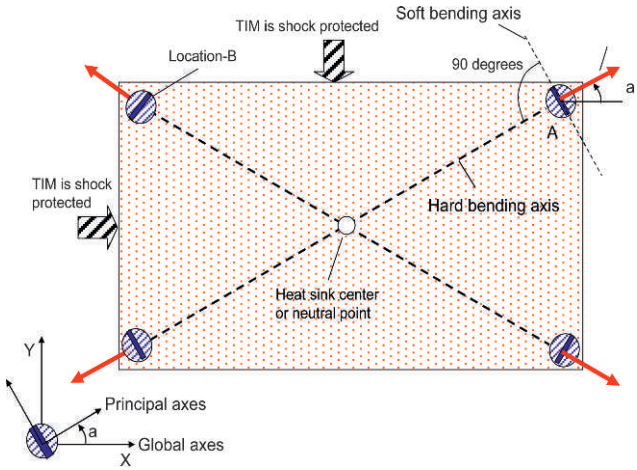

Fig. 12. Four point heat sink lateral slip schematic.

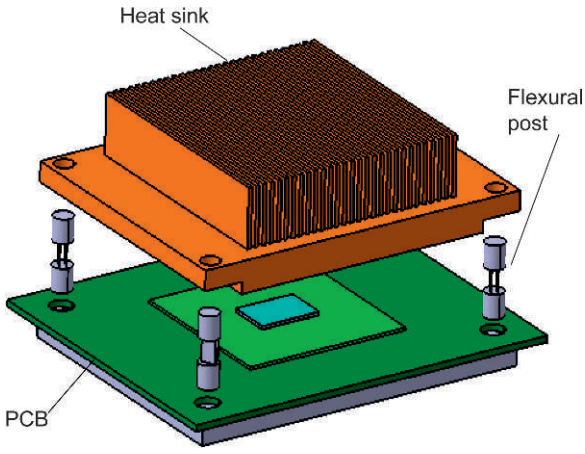

Fig. 13. Four point flexural concept.

typically surface mounted to the PCB using solder interconnects of various geometries. Critical to their life expectancy is the number of power on/off cycles the modules realize before failure. A common point of failure is the fatigue of the solder interconnects leading to cracking and eventual open circuits. Chip package interaction due to thermomechanical coupling, driven by CTE differences and thermal gradients, generates nonrecoverable inelastic strain in the solder interconnects, leading to potential fatigue failure. Heat sinks, which are necessary to dissipate the high thermal energy, can lead to added inelastic strain in the solder interconnects. To reduce this added strain, a carefully designed heat sink mounting system providing thermomechanical decoupling should be considered. By providing lateral slip at the mounting points, while maintaining shock protection of the solder interconnect, a heat sink mounting can be designed to minimize interconnect fatigue life.

Acknowledgments

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