NEAR TERM SOLUTIONS FOR 3D PACKAGING OF HIGH PERFORMANCE DRAM

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INTRODUCTION

The revolution in performance driven electronic systems continues to challenge the IC packaging industry. To enable the new generations of processors to reach their performance potential many manufacturers have developed interface formats to enable greater memory bandwidth. To ensure that the memory functions are able to support the increased signal speed, package developers are relying more and more on innovative 3D package assembly techniques and process refinement.

For some applications companies have had limited success in stacking die elements directly onto an interposer substrate using wire-bond processes. Stacking two or more memory die with perimeter located bond pads has been fairly successful however, because the die elements will typically have the same physical outline, spacers are needed between layers to clear the wire-bond loop height. Additionally, overall finished package height can be critical for a number of applications. Even though the die elements can be made very thin, the accumulated elements within the stack can be excessive. High performance DRAM die are especially difficult to stack. This is due to the center positioned wire-bond sites. This factor has complicated the die stacking process and because of the excessively long wire-bond interface, functional signal speed is significantly degraded.

Effective 3D stacking of DRAM devices can offer many benefits; improved performance, increased component density and greater surface area utilization. The methodology selected for package assembly, however, must consider process complexity, the costs associated with each process, overall package assembly yield and end product reliability. This paper will explore the positive and negative aspects of the package assembly variations noted above, comparing both performance attributes and physical limitations. Additionally, the authors will introduce a very innovative and very thin 3D package design and assembly process developed specifically for center-bond pad DRAM die. The methodology promises to remain economical because it requires no special die level process steps and utilizes the existing package assembly infrastructure.

Key words: DRAM, DDR, 3D memory,

BACKGROUND

Semiconductor memory plays an essential role in the development of countless electronic devices ranging from computers and gaming consoles to multimedia and telecommunications products. In order to furnish a broad supplier base and maintain a high level of performance, memory products must adhere to strict standards. These standards have been developed through close cooperation of semiconductor manufacturers through the JEDEC Solid State Technology Association. (JEDEC is an acronym for 'Joint Electron Devices Engineering Council'). The JEDEC JC-42 members have issued widely-used standards for device interfaces for random access computer memory (RAM), including the growing family of double data rate (DDR) memory standards.

The JEDEC DDR3 SDRAM standard in particular has been broadly adopted by the industry, offering improved performance, lower power and greater functionality than the earlier generation memory devices (e.g. DDR1 and DDR2). The primary benefit DDR3 SDRAM technology has over its DDR2 SDRAM predecessor is its ability to transfer data at twice the rate, enabling greater bandwidth. For example, with two transfers per cycle of a quadrupled clock, a 64-bit wide DDR3 module can achieve a transfer rate of up to 64 times the memory clock speed. With a memory clock frequency of 100 MHz, DDR3 SDRAM gives a maximum transfer rate of 6400 MB/s and the JEDEC DDR3 standard permits chip capacities of up to 8 gigabits. DDR3 memory also provides a reduction in power consumption of 30%. The DDR3 will function with only a 1.5V supply voltage, while the earlier DDR device families required 1.8V to 2.5V for operation. According to JEDEC, 1.575 volts should be considered the absolute maximum required for operation, especially when memory stability for servers or other mission critical devices is considered.

Advancement in Memory Technology

The successor to DDR3 is the DDR4 that will furnish higher bandwidth at an even operating lower voltage. The DDR3, however, is projected to account for 89% of the 808 million DRAM module units in 2011. This is up from 67% from the previous year (source: IHS iSuppli Research). DDR3 module manufacturing will likely continue to rise through 2012 by more than 90% with the cycle expected to decline in 2014 when DDR4 finally enters high volume production. Originally, the DDR4 production was expected to start in 2012, however, according to analysts, volume manufacturing of the DDR4 has been delayed due to new point-to-point topology, manufacturing complexity, high clock-speeds (~4266MHz) and other reasons. But the production ramp up of the fourth-generation double-data rate DRAM will be rapid. At present the analysts expect DDR4 to immediately gain a 12% share and by 2015 and DDR4 modules are projected to take a majority share of

market at 56%, compared to 42% for DDR3, (out of total DRAM module shipments of approximately 1.1 billion units).

Although the JEDEC specification for DDR4 was not finalized in 2011, a number of manufacturers began supplying demonstration memory for testing purposes. Samsung Electronics, for example, recently announced that it completed development of their 1.2V 2GB DDR4 non-buffered dual in-line memory modules using the 30nm process technology. The new DDR4 DRAM module is said to achieve data transfer rate of 2.133Gbps at 1.2V. In a notebook application, the DDR4 module is expected to reduce power consumption by 40 percent (compared to the current 1.5V for the DDR3 modules).

Demand for High Density Memory

The current industry solution for the stacked DRAM DDP (dual-die-package) employs conventional face-up wire-bond technology. The examples shown in Figure 1 are typical two-die packaging solutions for DDR memory. The DDR memory die, however, have the wire-bond sites located in the center of the die (similar to that detailed in the upper example).

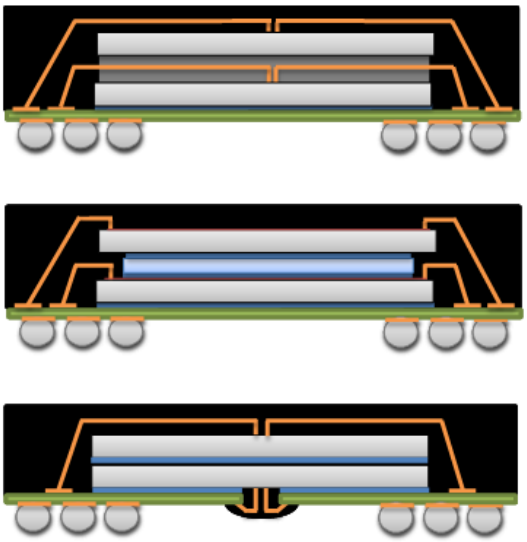

Figure 1. Multiple die memory package assembly variations.

Vertical stacking two center-bond die in the face-up configuration is being done but maintaining a uniform surface for mounting the second tier die over the wire-bonded first tier site is most difficult and the wire length is excessive. To minimize wire-bond length, a number of suppliers have adopted a surface redistribution layer (RDL) where copper conductors are provided on the wafer surface to re-route the center-bond site to the outer edge of the die element as shown in the center example. Others have resorted to both face-up and face-down die mounting typical of that illustrated in Figure 2. The lower die is mounted first using through-window-wire-bond processing. The second die is then mounted face-up onto back surface of the lower die and wire-bonded.

The vertical stacking of memory elements or stacking of pre-packaged single die memory devices has enabled greater memory densities; however, the current configurations cannot furnish the optimum finished package outline densification, performance enhancements and power-reduction goals. Although these package assembly variations have found a level of success for past applications, new innovations are needed to overcome issues associated with maintaining signal integrity and to overcome performance degradation that commonly occur as memory densities increase.

ENHANCED DDR MEMORY PERFORMANCE

Servers with multi-core processors will continue to require more memory bandwidth and the increased demand for product miniaturization and high-performance computing continue to call for higher density and higher speed memory devices and modules. Additionally, more innovative solutions will be needed to provide the higher bandwidth memory in less space to prepare for the significant growth anticipated for next generation smart phones and personal media electronics.

One of the key issues for DDP assembly is maintaining balance on signal functions while minimizing overall trace lengths. An innovative dual face-down (DFD™) package developed by Invensas improves these aspects for both die elements within the package This construction (cross-section detailed in Figure 2) also provides improved thermal as well as electrical performance and yield enhancements when compared to current DDP assembly.

Figure 2. Invensas ‘dual face-down package’ for center-bond DDR memory.

The DFD package enables flexible access. The separated DQ signals from the two die elements can be tied together or used separately (depth or width expandable). Using the through-window wire bond process for both die elements eliminates the need for expensive RDL on the wafer. The resulting short interface between the die bond sites and the interposer provides minimal interconnect pathway length for better electrical performance and significantly reduces gold wire usage.

DFD Package Substrate Design

The base material selected for the dual die package substrate is a 200 micron thick glass reinforced Bismaleimide-Triazine (BT) with 12 micro thick (1/2 oz.) copper foil laminated to both outer surfaces. The laminate is one of the preferred substrate materials for array configured semiconductor package applications.

The physically stable characteristics of the materials composition make it an excellent selection for larger panel size fabrication as well (Table 1).

Table 1: Two-Metal Layer substrate material stack-up.

Description	Material	Thickness
Core dielectric	B-T/Glass	200 microns
Foil [1]	Copper	12 microns
Electroplate [1]	Copper	10 microns
Barrier plating [1]	Nickel	5-12microns
Finish plating [1]	Gold	0.5-1.3 microns
Soldermask [1]	AUS-308	25 +/- 7 microns

[1] Material build-up is on both sides of core

The finished dual-face-down package substrate is 280 +/- 50 microns thick and measures 11.5mm per side. Two narrow slots are provided between the wire-bond land features to accommodate the through-window wire-bond process (Figure 3).

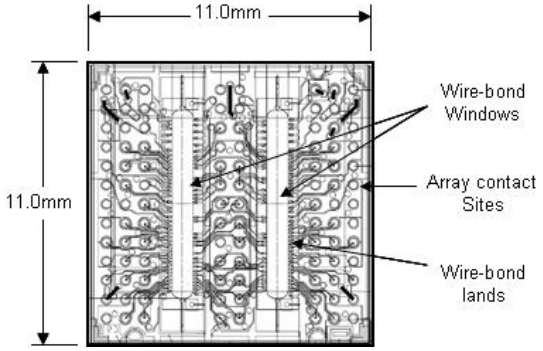

Figure 3. Substrate developed for the dual face-down package (bottom view).

The conductive traces connecting the wire-bond lands and ball attachment land have a uniform width of 35 microns with equal spacing between conductors. The land features furnished for attaching the solder ball contacts are soldermask defined providing a 450 micron diameter surface.

DFD Assembly Process

The Invensas DFD Multi-Die Package for DRAM provides enhanced electrical and thermal performance by utilizing a face-down only device configuration. This arrangement minimizes interconnect pathway lengths to terminals while offsetting the stacked die to reduce thermal impedance as shown in Figure 4.

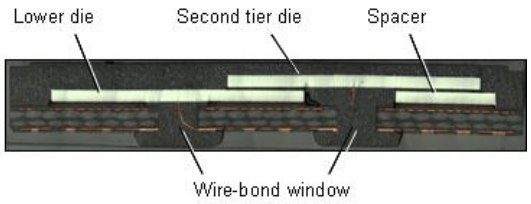

Figure 4. Cross section of face-down offset wire-bond.

The first phase assembly sequence begins with the transfer of an arrayed substrate strip to a stencil printing system where a die attach adhesive compound is printed onto the substrates surface. Utilizing a precision die attach system, pre-heated die elements are placed onto the adhesive-lined substrate. A spacer element of the same thickness of the die element is also placed onto the substrate to support the second tier die attachment. (The initial prototype DFD components were developed using two Micron 1Gb DDR3 devices). When all die elements and spacers are cured the strip is transferred to a dispensing system to deposit a pattern of adhesive on the back surface of the lower die and spacer. Following the second tier die attach and cure, the strip assembly is inverted to expose die bond pad areas in preparation for the wire-bond process.

Note: In preparation for 'through-window' wire-bond, the strip is subjected to an aggressive plasma cleaning process to ensure that the wire-bond sites on the die and substrate are free of any contamination that could compromise the wire-bond interface. Following the cleaning process the strips are immediately transferred to a high speed wire-bond system.

The wire-bond process is not unlike that used for single die face-down assembly. The initial stage of the 'gold wire-bond' process employs either an open hydrogen flame or an electronic spark to melt the wire end to form a small ball feature. The gold ball is then pressed down onto the semiconductors die bond site and, using a precise force, time and a short bust of ultrasonic energy, completes the first phase of the wire-bond process. The gold wire is then drawn upward and looped over to align with the bond site on the substrates outer surface.

The next step of the wire-bond interface uses a 'wedge-bond' process. This process relies on precise force and ultrasonic energy to join the gold wire to the Ni/Au plated substrate land. (Figure 5).

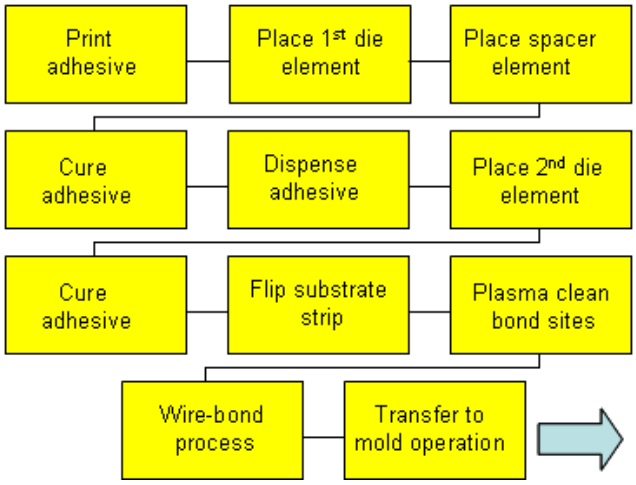

Figure 5. First phase DFD package assembly sequence.

Following a thorough visual inspection to verify wire-bond process uniformity and quality (Figure 6) the assembled strip is transferred to the molding and the final assembly operations.

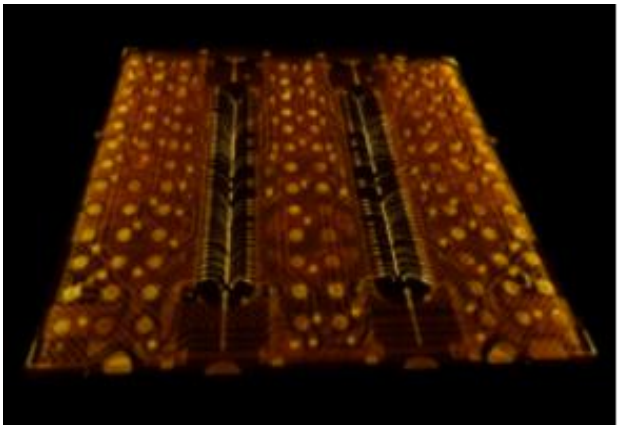

Figure 6. 3D X-ray view of bottom surface DFD first phase assembly.

The final phase of the package assembly includes an injection molding process, laser marking, ball attach, singulation, electrical test and burn-in (Figure 7).

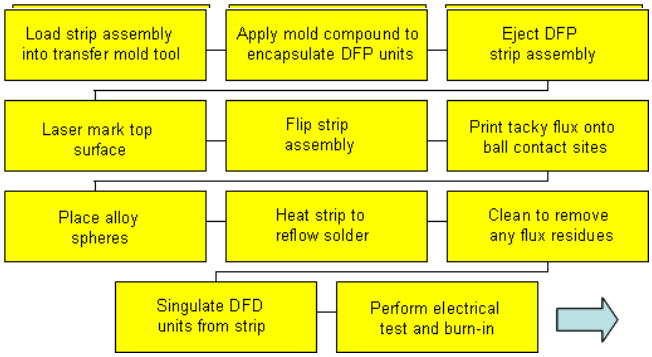

Figure 7. Second phase DFD package assembly process sequence.

Assembly Material Breakdown

- First layer adhesive: 45 micron thick Henkel 'Ableflex' material (print process).
- Second die attach adhesive: 30 micron thick Henkel 'Ablebond' material (dispense process).
- Wire-bond interface: 20 micron diameter Au wire.
- Die thickness: 150 micron.
- Mold compound: Hitachi Chemical (injection mold and slot fill in same step).

FBGA Contact Attachment

The JEDEC design standard describes the contact features on the FBGA as balls, bumps or other protruding terminals (excluding pins) constructed from a variety of alloy and/or even polymer based materials. The standard states that the distance or pitch between the centerlines (e) of any two adjacent rows or columns of balls can be one of three dimensions; 0.5mm, 0.65mm or 0.80mm, besting compliance with existing JEDEC DRAM standards and accommodating efficient surface routing of the circuit on the DIMM substrate, the Invensas engineers selected the 0.8mm ball pitch variation. The 0.8mm contact pitch also enables a wider choice for ball diameter selection as shown in Table 2.

Table 2: Standard FBGA contact diameter variations.

e	Contact diameter variations (mm)		
	Min.	Nom.	Max.
0.80	0.45	0.50	0.55
	0.40	0.45	0.50
	0.35	0.40	0.45
	0.30	0.35	0.40
	0.25	0.30	0.35

The contact selected for the DFD package application is a 450 micron diameter SAC105 (tin-silver-copper) alloy solder ball attached to a 450 micron diameter land. The solder ball attachment process consisted of a sequential three stage operation beginning with the printing of a tacky flux onto each contact site, placing the pre-formed 450 micron diameter solder spheres onto the flux prepared sites and mass reflow soldering to complete the joining process. Although a flux material selected for this process is classified as 'no-clean', a thorough semi-aqueous cleaning process followed solder reflow to remove any residual materials or particles from the interposer's bottom surface.

The final operation is the separation of the individual DFD units from the strip configuration. Although future designs may be able to accommodate die punch singulation (commonly preferred for high volume manufacturing), the package developed for this program relied on a precision saw singulation process that resulted in furnishing a very smooth wall surface (Figure 8).

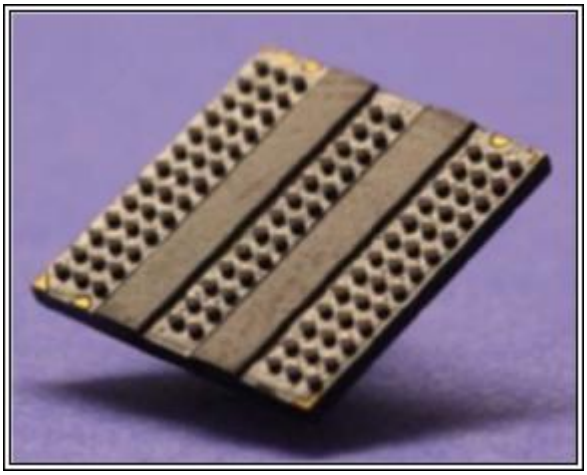

Figure 8. Bottom view of a completed two die DFD package assembly.

Addressing JEDEC Compliance

Although JEDEC members have not yet developed a mechanical outline that represents the DFD application, the Invensas engineers attempted to adhere to the existing design guideline specifications published in JEDEC Design Standard 'JEDEC PUBLICATION 95 DESIGN GUIDE 4.5' for the Fine-pitch, Square Ball Grid Array Package (FBGA) family. The standard simply states that the carrier body of the package has a metalized circuit pattern applied to a dielectric structure. One or more semiconductor devices can be attached to either the top or the bottom surface of this dielectric carrier. On the underside of the dielectric carrier is an array pattern of metalized balls, which form the mechanical and electrical connection from the package body to a mating feature such as a printed circuit board.

In regard to determining the ball locations, the matrix pitch and the offset of the central row(s) or column(s) of balls from datum A or B defines the ball location on an FBGA package as detailed in Figure 9.

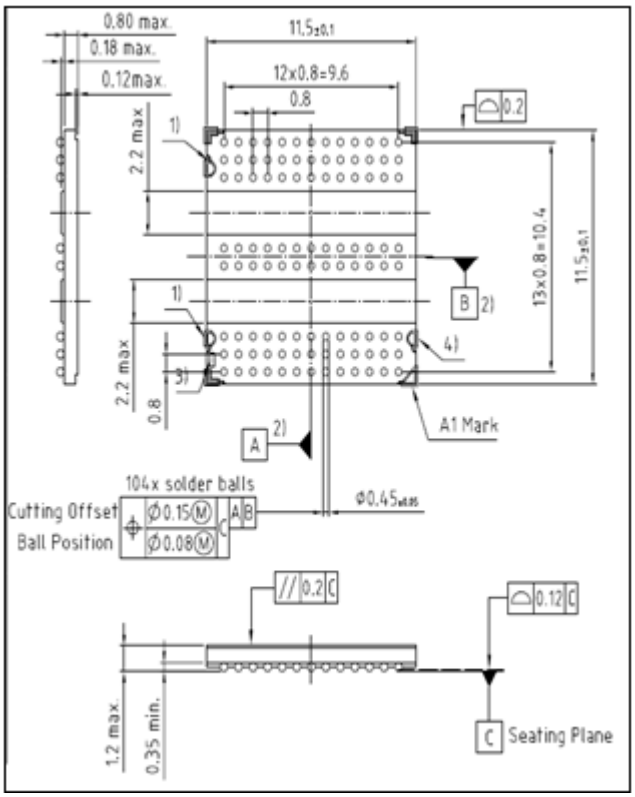

Figure 9. Mechanical outline detail for the Invensas two DDR3 die, face-down wire-bond package.

The JEDEC standards further states that the interposer's surface that contains the die elements may be encapsulated by various techniques to protect the semiconductor(s). The standard defines the symbols, definitions, algorithms, and specified dimensions and tolerances for what they refer to as a "flange-type" FBGA package with square bodies. The term 'flange' describes the area of the package that extends beyond the outline of the die elements. The specification uses metric dimensioning per JEP95, Section 3, SPP-003, and adheres to the geometric dimensioning and tolerance methods defined in ASME Y14.5M-1994. This standard does not attempt to document all FBGA designs being produced. It simply establishes the design requirements that shall be followed for future FBGA outlines included in JEDEC Publication 95 (JEP-95). The total finished package height of 1.2mm provides a profile that enables the potential for mounting devices on two sides of a standard RDIMM substrate.

RDIMM SUBSTRATE DEVELOPMENT

The RDIMM (dual in-line memory module) format developed for high performance DDR applications is designed to interface to a host PCB through a row of bottom edge located contacts. The JEDEC registered MO-269 product outline document that controls the requirements for the DIMM substrate specifies a common contact pitch of 1.0mm and that the edge contact features be plated with a Ni/Au surface finish. The registered outlines prepared by JEDEC Committee JC-11 reflect products with anticipated usage in the electronics industry but are not automatically classified as a 'standard' and users are cautioned that "changes are likely to occur". There are three RDIMM profile variations defined in the JEDEC MO-269 document that are physically identical accept for their height; one that is 50.0mm in height, another at 30.0mm in height (defined as 'low profile') and a third having a significantly lower height of 18.75mm is identified as 'very-low profile' (Figure 10).

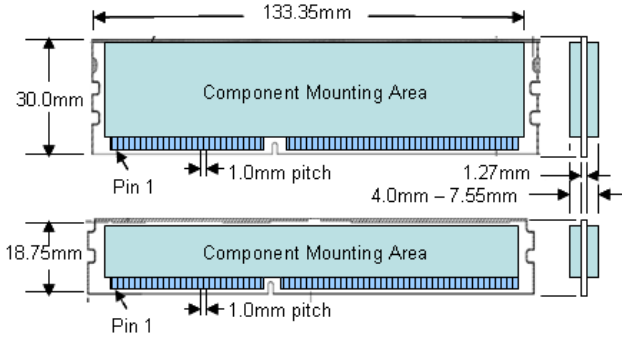

Figure 10. Comparing low profile and very low profile DIMM module outlines.

In addition to the basic outline dimensions the document also considers differing memory package profiles and includes variations requiring heat spreaders. The example furnished in Figure 11 represents a high performance memory product currently in volume production with 18 single die packaged DDR Memory + Register supplied on a standard 'Low Profile' DIMM substrate.

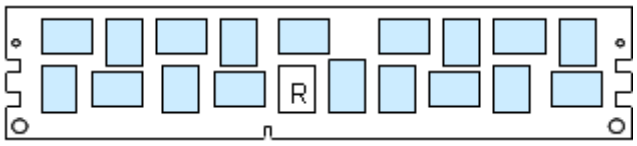

Figure 11. DDR memory DIMM with single die packaging.

Because of the inconsistent package placement and orientation of this product, circuit interface is less than optimum requiring as much as ten circuit layers (8 signal layers + power and ground).

The Invensas developed DFD memory package outline is 11.5mm square. This is only slightly larger than a single die DDR memory package outline. Because the DFD memory package units can be arranged in a single side-by-side row, user are able to adapt the 'Very-Low (18.5mm) Profile' DIMM substrate variation (Figure 12).

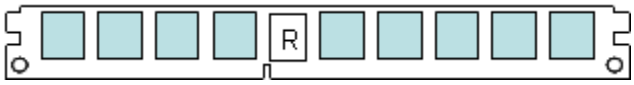

Figure 12. Nine dual die DDR memory units mounted onto a Very Low Profile DIMM substrate.

The two die face-down package has three primary attributes; 1) it furnishes a direct circuit path from the die element to the package substrate and, when compared to other two die innovations, significantly reduces inductance. 2) allows the devices to be configured with a common orientation in the single row format enables the use of a significantly lower profile substrate design and a more direct circuit interface between packages. 3) This less complex routing scheme also has the potential to reduce fabrication cost by eliminating two circuit layers from the DIMM substrate.

SUMMARY AND CONCLUSIONS

Increasing demand for product miniaturization and high-performance computing continue to call for higher density and higher speed memory devices and modules. The server and enterprise markets adopting multi-core processors need greater memory bandwidth. The mobile electronics markets continue to see significant growth in smart phones and tablet products as well. Manufacturers are expecting higher bandwidth memory to be packed in less space while facilitating reduced power usage. The device stacking segment of memory products is growing in response to increased demands for densification, performance and power-reduction. The current industry solution for stacked dual-die-package for DDR memory, however, employs conventional face-up wire-bond processes. The center-bond format results in excessive wire-bond loop spans. While mounting one die in the face-down orientation helps in reducing wire-bond length for one die, the wire-bond interface for the face-up die mounted on the backside of the bottom die remains significantly longer.

When there is a wide difference in wire length between the two die elements, package performance is compromised. To reduce wire-bond length and provide a more uniform die to substrate interface, companies have resorted to modifying the wafer to provide copper conductors from the center-bond lands to the outer edge of the die element. This wafer level redistribution layer (RDL) process adds significant cost. And even though the wire-bond sites are at the outer edge of the die, a spacer must be added between the lower die and upper die to provide clearance for the wire-bond loop profile. Companies are also finding that in exchange for increased memory density they are faced with serious thermal performance constraints.

Invensas believes that the DFD packaging innovation described in this paper extends the µBGA® face-down structure advantage to multiple devices and represents only one potential embodiment of the concept for multi-memory device packaging. DFD has been enabled in part due to advances in silicon processing technology which have brought die sizes down to a workable range. The company has proved that the offset die stacking process can be accomplished efficiently while maintaining a finished package outline that is compatible the requirements for high performance RDIMM applications.

The dual die face-down package offers clear advantages over existing industry practices in both electrical and thermal performance. In regard to performance, finite element analysis (FEA) data compiled for the two-die DFD memory configured device projects as much as 25% reduction in package thermal resistance. In regard to economics, it's estimated that the overall packaging cost is reduced by 15 to 20% when compared to alternative two die memory package variations. Additionally, the DFD assembly process uses existing BGA package assembly and test infrastructure, no new materials or specialized equipment is required.

Note: Extensive computer modeling was conducted throughout the two-die package design and development program. The test vehicles are currently being subjected to a broad range of physical testing that is in compliance with their intended use environment. When the reliability evaluations are completed on the DFD test vehicles, the company is confident that the results will be published.

REFERENCES

1. JEDEC JESD79, *'Double Data Rate Synchronous Dynamic Random Access Memory (DDR3) Standard'.*
2. JEDEC JESD209, *'Low Power Double Data Rate (LPDDR) SDRAM 1.2 V I/O'.*
3. IHS iSuppli, Research *'DRAM Module 2011 Market Tracker'.*
4. JEDEC PUBLICATION 95 DESIGN GUIDE 4.5, '*Fine-pitch, Square Ball Grid Array Package (FBGA)'.*
5. JEDEC registered outline MO-269, '*DDR3 SDRAM DIMM (dual inline memory module) Family with 1.00mm Contact Centers'.*