

Assembly and Reliability of 1704 I/O FCBGA and FPBGAs

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Abstract

Commercial-off-the-shelf ball/column grid array packaging (COTS BGA/CGA) technologies in high reliability versions are now being considered for use in a number of National Aeronautics and Space Administration (NASA) electronic systems. Understanding the process and quality assurance (QA) indicators for reliability are important for low-risk insertion of these advanced electronic packages. This talk briefly discusses an overview of packaging trends for area array packages from wire bond to flip-chip ball grid array (FCBGA) as well as column grid array (CGA). It then presents test data including manufacturing and assembly board-level reliability for FCBGA packages with 1704 I/Os and 1-mm pitch, fine pitch BGA (FPBGA) with 432 I/Os and 0.4-mm pitch, and PBGA with 676 I/Os and 1.0-mm pitch packages.

Key Words: ball grid array, BGA, flip chip BGA, FCBGA, FPBGA, CSP, thermal cycle, drop, solder joint reliability

Introduction

Ball grid arrays (BGAs) and chip scale packages (CSPs) are widely used for many electronic applications, including portable and telecommunication products [1]. BGAs with 1.27-mm pitch and 1000 I/Os or less and having tin-lead solder alloys are implemented for high-reliability applications that generally demand more stringent thermal and mechanical cycling requirements. The I/Os are continuously increasing, and plastic BGAs (PBGA) packages with 1.0-mm pitch up to about 2000 I/Os are offered by package suppliers. PBGAs were introduced in the late 1980s and implemented with great caution in the early 1990s, further evolving in the mid-1990s to fine-pitch BGAs (FPBGAs, also known as CSPs) having much finer pitches of 0.4 and 0.3 mm.

In general, area arrays come in many different package styles, including the plastic ball grid array (PBGA) with ball composition of eutectic $\text{Sn}_{63}\text{Pb}_{37}$ alloy or slight variations such as $\text{Sn}_{60}\text{Pb}_{40}$. The ceramic BGA package uses a higher melting ball ($\text{Pb}_{90}\text{Sn}_{10}$) with eutectic solder attachment to the die and board. The column grid array (CGA) or ceramic column grid array (CCGA) is similar to a BGA except that it uses column interconnects instead of balls. The lead-free CCGA potentially could use copper instead of a high melting lead/tin column. The flip-chip BGA (FCBGA) is similar to the BGA, except that internally a flip chip die rather than a wire-bonded die is used. For PBGAs with more than 1000 I/Os, FCBGA is used in order to accommodate even the larger number of I/Os required for the flip-chip die within FCBGA package.

Extensive work has been carried out in understanding technology implementation of area array packages for high reliability applications. The work included process optimization, assembly reliability characterization, and the use of inspection tools, including x-ray and optical microscopy, for quality control and damage detection due to environmental exposures [2–12]. In previous investigations, the 1156 I/O PBGA package was the highest I/O PBGA package evaluated for assembly reliability. FCBGA with 1704 I/Os package assemblies were evaluated in this investigation.

This paper provides comprehensive process/reliability test results for a test vehicle configuration with FCBGA1704 as well other fine-pitch BGA (FPGA) packages. Numerous test vehicles (TVs) were built to determine issues associated with process and reliability of two extreme type PBGA packages. Packages with extremely high I/Os and packages with fine pitch were assembled side by side in a test vehicle to narrow issues associated with their manufacturing on one board. The package configurations were 1704 I/Os FCPBGA with 1.27-mm pitch and FPBGA 432 I/Os with 0.4-mm pitch. A PBGA with 676 I/Os was used as baseline. Both vapor phase reflow and a rework station were used to reflow $\text{Sn}_{63}\text{Pb}_{37}$ tin-lead eutectic solder paste. Solder balls have either tin-lead or lead-free solder alloy composition. Process variations for these types of packages as well their yields after process optimization and implementation are also presented. Furthermore, results for thermal cycle reliability of TVs with daisy chain configuration under four thermal profiles are presented and discussed in detail, including optical, x-ray, and x-sectional SEM photomicrographs showing damage progress.

Package and Assembly Variables

Test vehicles (TVs) were built with daisy-chain FCBGA packages with 1704 I/Os and 1.0-mm pitch, FPBGA packages with 432 I/Os and 0.4-mm pitch, and a control PBGA package with 676 I/Os and 1.0-mm pitch. Figure 1 shows a photomicrograph of a section of ball pattern of FCBGA1704 package (left) and daisy-chain design pattern for the all-ball connections and probe pads for local global and local monitoring. As apparent in a few locations, daisy-chain patterns were

not in a regular pattern, showing an irregular jumper that needed to be verified through probing of assigned balls prior to committing to building printed circuit boards. Visual inspection of the package by microscope revealed that these irregular daisy connections were on the surface of package and therefore could be identified visually as marked on the photomicrograph. Figure 2 shows the board design with daisy-chain pattern and routing of traces to the edge of the board for daisy-chain monitoring.

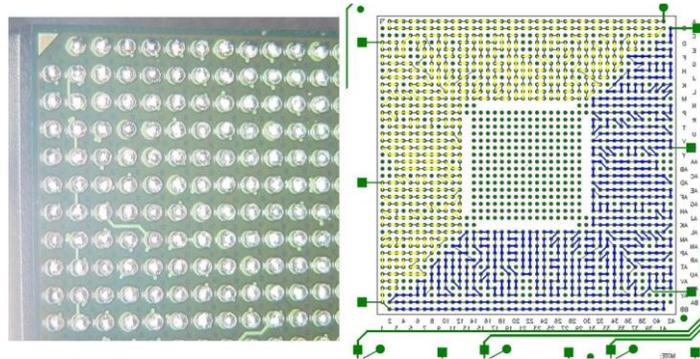


Figure 1 - Photomicrograph (left) and daisy chain pattern of 1704 I/O flip-chip BGA (FCPBA) with 1.0-mm pitch and 42.5-mm² body size.

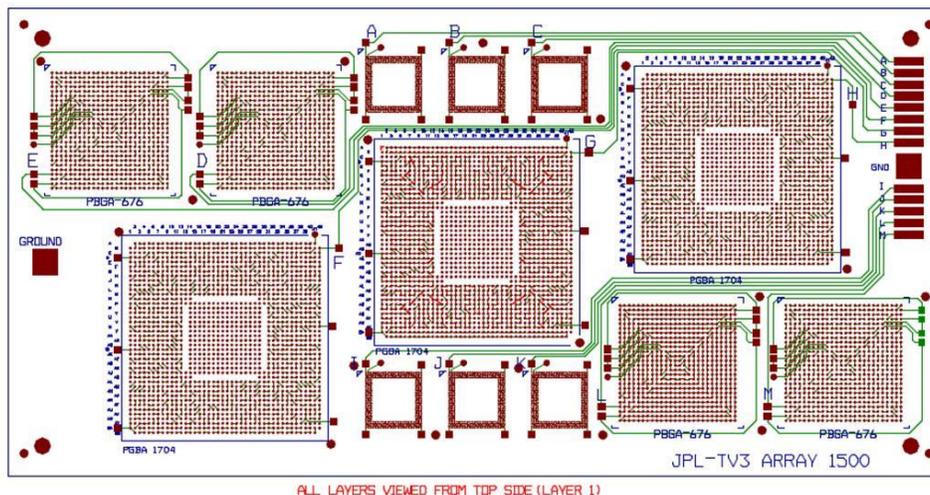


Figure 2 - Test vehicle design showing combined package and board daisy-chain patterns at three locations for the 1704 I/O flip-chip BGA (FCPBA) package with 1-mm pitch and 42.5-mm² body size. Location and board daisy-chain patterns for PBGA 676 I/Os and 432 I/Os are also apparent in the design.

A design of experiments (DOE) technique was used to cover various aspects of processing and packaging assembly reliability. The following packages and parameters were evaluated as part of a larger DOE implementation:

- The FCBGA1704 with 1.0-mm pitch and 42.5-mm² body size designed in three locations, one at the center with high sensitivity to mechanical loading. Numerous daisy chains were designed on board to compliment daisy chains on a package in order to generate complete chains for solder joint failure monitoring. Probe pairs were added near packages to monitor subdivided daisy chains.
- Six 432 I/O FPBGAs with 0.4-mm pitch and 13-mm² body size as well as four 676 I/O PBGAs with 1.0-mm pitch and 27-mm² body size were included in the evaluation.
- Boards were made from high glass transition temperature (T_g) FR-4 materials with 0.093-inch thickness. They had a hot air solder leveling (HASL) tin-lead surface finish commonly used for tin-lead solder.
- A standard 4-mil-thick stencil was used for paste printing of the whole board. However, a mini stencil with 4-mil thickness was used for paste printing locally when it was required to accommodate assembly of FCBGA1704 packages by a rework station.

Solder paste volumes were measured at the four corners and at the center for several assemblies to document actual paste print volume, distribution, and solder paste release efficiency. Vapor phase reflow was used to assemble all packages, including the 1704 I/Os when it was required as part of the DOE design. Only the FCBGA1704 packages were also

assembled using a rework station as required by design. A number of FCBGA1704 packages were mechanically strengthened by applying spot bond adhesives at the corners and centers after assembly. A test vehicle was conformally coated. These assemblies were first subjected to inspection and daisy-chain continuity checks to determine manufacturing robustness of various package configurations. They were then exposed to a number of environmental conditions to evaluate their reliability and failure mechanisms. Both the process yield and reliability results for FCBGAs, FPBGAs, and PBGAs are discussed below.

Test Vehicles and Assembly Parameters

Figure 3 shows a test vehicle assembly with one 1704 I/O, six 432 I/O FPGAs, and four 676 I/O PBGAs. All boards were laminated from a high Tg FR-4 epoxy having 4×6 inch surface area and thickness of 0.093 inch as specified by IPC 9701. All packages had daisy chains where most pairs of pads were connected internally within the die and a few connected through exposed traces. Complementary pairs of PWB pads were designed so that their connections within package daisy chain pairs completed a specific daisy-chain pattern for solder joint failure monitoring. Daisy chains for each package were used for monitoring at intervals to detect failures due to either thermal cycling or drop tests. Additional small probing pads were added at each side of the package for manual probing in more detail, enabling further narrowing of failure locations.

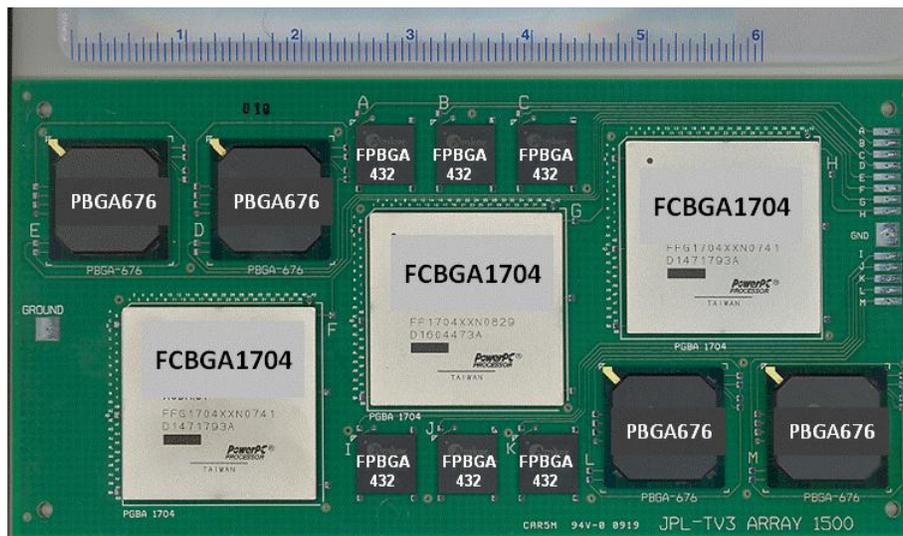


Figure 3 - Photomicrograph of a partially populated test vehicle showing the spot staking of the FCBGA1704 at the corners and periphery.

Solder Paste Volume

Initially, type III (-325+500) RMA pastes, solder particle diameter between 25 and 45 microns, were used for paste deposition on the PCB pad's patterns using a paste print machine with standard parameters, including paste print speed. Later, type V (-500) RMA paste, solder particle diameter between 15 and 25 microns, was used to improve assembly yield for fine pitch BGA parts. The rule of thumb for an aperture opening is for it to be about four to five times the solder powder diameter. After deposition, each paste print was visually inspected using a microscope for detecting gross defects such as bridging or insufficient paste deposition. For the FCBGA1704, on rare occasion, print quality was improved by either adding a small amount of solder paste when insufficient paste was detected or by removing solder paste from the connecting pads when bridging was discovered. Figures 4 and 5 show representative photomicrographs of paste print and quality for the FCBGA1704 and the FPGA432, respectively.

In addition, solder paste areas and heights were measured using a laser profilometer with a three-dimensional (3D) measurement capability. Measurements were made at numerous locations—including corner and peripheral center pads—to gather solder volume data and their corresponding distributions. Figure 6 shows an example of photomicrographs of FCBGA1704 pads after solder paste deposition quality and solder paste characteristics parameters, including heights and areas. This figure also shows color-coded height distribution of solder paste print for this set of pads. A similar distribution with acceptable quality was achieved for solder paste deposition of PBGA676 with 1.0-mm pitch. Overall, no major manufacturing issues were encountered with the paste depositions for the two BGAs with 1.0-mm pitch.

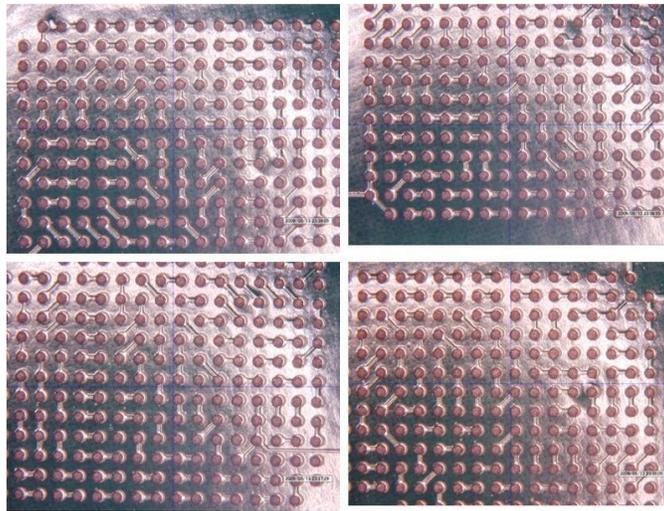


Figure 4 - Representative photomicrographs of paste print deposition quality for the FCBGA1704 pattern on PWB.

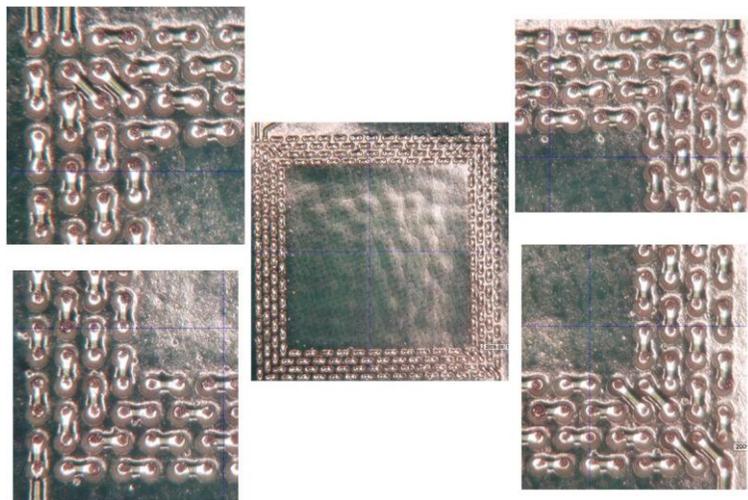


Figure 5 - Representative photomicrographs of paste print deposition quality for the FPGA432 pattern on PWB.

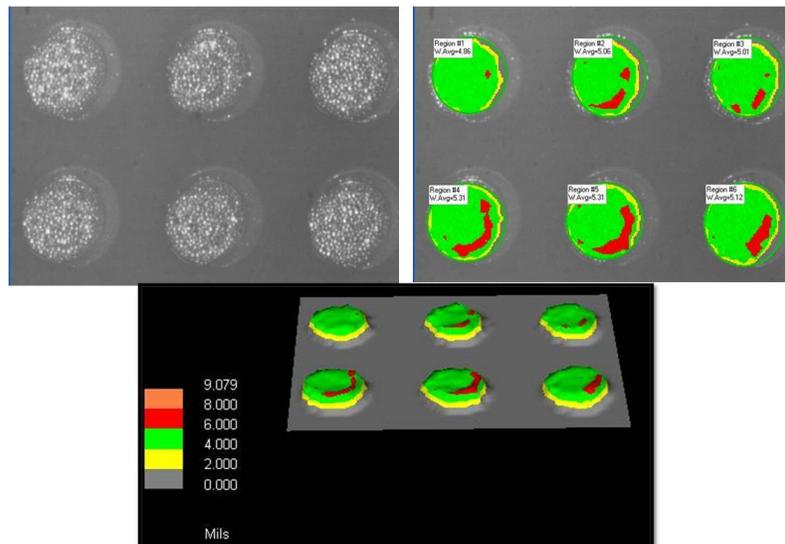


Figure 6 - Solder paste print quality and estimated volumes for FCBGA1704 using a laser profilometer. Color-coded solder height distribution (bottom) can also be seen.

Figure 7 shows an example of photomicrographs of solder paste print and color-coded height for the FPBGA432. Uneven distribution of solder pastes is apparent especially from color-coded figures. The variation shown for solder paste print

quality was considered unacceptable when type III solder paste was used. Use of solder type III was discontinued after a few trial paste depositions. Type V solder paste was used after initial trial with some improvement. Figure 8 shows representative plots of solder paste distribution and color-coded heights for the FPBGA432 package using the type V solder paste.

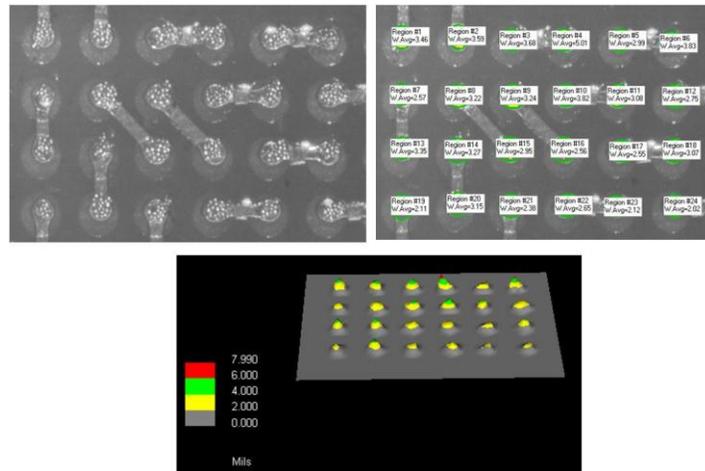


Figure 7 - Examples of plots of solder type III paste print quality and volumes for FPGA432 using a laser profilometer.

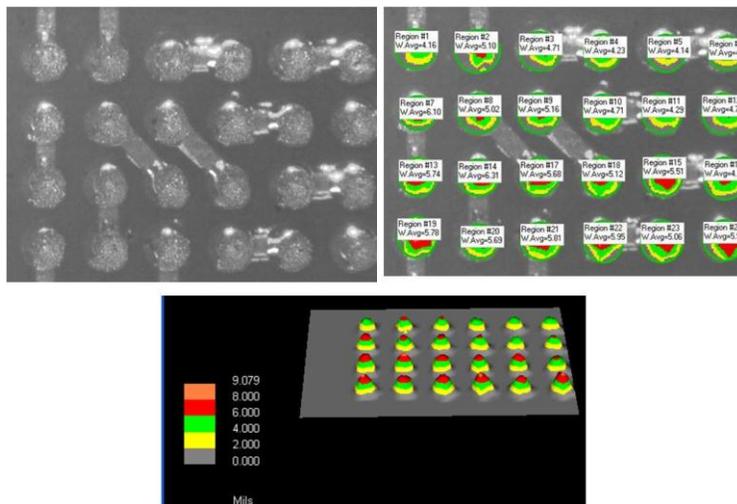


Figure 8 - Examples of plots of solder type V paste print quality and volumes for FPGA432 using a laser profilometer.

Attachment Procedures

Intentionally, a large number of FPGA432 packages were designed close to the FCBGA1704 package. The reason for such configuration was to determine paste print quality and manufacturing challenges associated with a large array package surrounded by small fine pitch ones. As envisioned, significant processing challenges were encountered during assembly. These were further aggravated in some cases where the package had lead-free solder balls that were assembled with tin-lead solder paste. To minimize solder bridging of FPGA432, a 4-mil-thick stencil was used for both standard and mini stencil paste printing. Appropriate aperture opening size for each package type was designed to achieve a minimum level of solder paste volume.

Initially, type III with coarser solder powders was used, but it was thought that the use of type V solder paste with a finer mesh should improve manufacturability and yield for the fine pitch BGA packages. Package placement was accomplished using an automatic placement machine. However, placement by rework station was also performed to determine feasibility of such approach. Solder paste reflow was performed using a vapor phase reflow machine set up for tin-lead process. Reflow profiles were based on a previously established profile that was tailored using a sample run with the attached thermocouple generating the reflow thermal profile. Vapor phase consists of an infrared preheating followed by a constant temperature boiling vapor zone.

Infrared preheating temperature and time as well as time in vapor phase are the only key parameters that can be modified to achieve better solder attachment quality. For the FPBGA1704, mini stencil was used for paste printing and rework station for package placement and solder reflow.

X-ray Evaluation

Real time x-ray systems are categorized as 2D and 3D x-ray systems. The 2D system is a standard x-ray inspection system with a microfocus source and a stationary image intensifier as the detector, capable of producing offset pseudo 3D features. The 2D x-ray systems are very effective in testing single-sided assemblies. With the use of a sample manipulator, an oblique view angle enhances inspection of both single and double-sided assemblies with some loss of magnification due to increase in distance between source and detector. Experience is needed in discerning between bottom-side board elements and actual solder and component defects. This can be very difficult or even impossible on extremely dense assemblies. In any case, only certain solder-related defects such as voids, misalignments, and solder shorts are easily identified by transmission systems. However, even an experienced operator can miss other anomalies such as insufficient solder, apparent open connections, and cold solder joints. The x-ray system with a rotational detector allows oblique generation of x-ray images with a higher magnification and a better intensity resolution since the focal spot remains the same and there is, therefore, no loss of magnification. An isocentric manipulator keeps the field of view unchanged when the oblique view mode is used. This feature allows better characterization of some defect features, including wettability and void location in area array packages.

Daisy-Chain Resistance Results

As the first step, daisy-chain resistances for package assembly were measured after first and subsequent builds to verify process acceptance. All packages had a pair of connected pads, which complemented specific pairs of PWB pads to build loops of continuous daisy chains for solder joint opens. A short could be detected when lower-than-nominal resistance values were measured. The results of manufacturing yield for various conditions of assembly using vapor reflow and rework station are summarized in Table 1. Manufacturing yield for FCBGA1704 was favorable with only one open whereas this was not the case for the other two packages. The FPBGA432 showed unacceptably low yield while results for PBGA676 were mixed with medium to high yield.

Inspection after TV Build

For PBGA package assembly, visual inspection is of limited use since it is difficult to inspect peripheral ball interconnection and impossible to inspect hidden balls under the package. X-ray evaluation is needed for area array packages to determine shorts and possibly opens in a rare occasion. For the test vehicle with daisy-chain package configuration, verifications were performed: (1) through daisy-chain continuity checking and (2) through x-ray quality detection for shorts and in a rare occasion for opens. For the FPGA432 assemblies, shorts were clearly detected by x-ray and gross opens in some cases apparent by being much smaller size balls. In a few cases, open and package lift was even apparent under optical microscope. To reduce cost, representative quality was verified by cross sectioning only after environmental tests.

Table 1 - Summary of daisy-chain resistance measurements after build and in some cases after local reflow by rework station.

ID with Process-Environment	A 432- SnPb	B 432 SnPb	C 432 SAC105	D 676 SnAg	E 676 SnPb	F 1704	G 1704	H 1704	I 432SAC 305	J 432 SnPb	K 432 SAC405	L 676 SAC305	M 676 SAC405
SN01-Tv3-Vap-CF-Nbnd-JM	Open	Open	Open	2.1	Open	NP	6.9	NP	Open	3.2	Open	2.1	1.9
SN02-Tv3-Vap-16bnd-RIT	0.3	Open	Open	2	2.1	o	6.1	Open	1	0.8	0.9 (AR)	2.1	2.1
SN03-Tv3-Vap-16bnd-JM	0.6 (AR)	0.1 (AR)	0.6 (AR)	1.8	1.9	NP	6.8	NP	NP (AR)	0.5 (AR)	0.2 (AR)	1.7	1.6
SN04-Tv3-Vap-Nbnd-RIT	0.9	0.7	0.7	1.9	2.1	NP	6.6	NP	0.8	0.7	0.7	1.7	1.6
SN05-Tv3-Vap-16bnd-JM	0.1 (AR)	0 (AR)	0.6 (AR)	1.5	1.8	NP	6.3	NP	np	NP (AR)	0.6 (AR)	(R/R)	1.3
SN06-Tv3-Vap-16bnd-RIT	1	0.9	0.9	1.9	1.9	NP	6.9	NP	1	0.9	0.9	1.9	2
SN07-Tv3-Vap-Nbnd-JM	0.4	0.1	Open	2	1.9	NP	6.3	NP	np	0.2	Open	1.9	Open
SN-10-TV3-3PvLLC-LFll-Vap-Nbnd-JM	1.2	1.2	1.1	2.4	2.5	Open (AR)	7	6.4	0.9	0.8	0.9	1.9	Open (RR)
SN11-TV3-RWK-TL-TL;Nbnd-JC	0.8	0.7	0.7	1.7	1.7	NP	6.6	NP	0.8	0.8 (AR)	0.8	1.7	2.2
SN12-TV3-RWK-TL-TL;16bnd-RIT	0.6	0.6	0.7	1.7	1.8	NP	6.8	NP	0.7	0.7	0.7 (AR)	1.8	1.8
SN13-TV3-RWK-TL-TL;16bnd-RIT	0.7	0.7	0.7	1.8	1.9	NP	6.3	NP	0.8	0.7	0.7	Open	1.7
SN21-TV3-Vap-LF-TL-Nbnd-RIT	0.7	Open	0.7	1.8	2	Open	5.3	NP	0.6	0.6	0.6 (AR)	1.5	1.4
SN22-TV3-Vap-LF-TL-Nbnd-JC	1.2	0.6 (AR)	1.1	2.4	2.5	NP	5.7	NP	1.2	0.4 (AR)	1.1	2.2	10.8
SN23-TV3-Vap-LF-TL-16bnd-JC	0.4	0.2 (AR)	0.8 (AR)	1.7	1.7	NP	6.8	NP	9.5	0.3	0.7 (AR)	1.6	1.6
SN24-TV3-Vap-LF-TL-16bnd-RIT	0.7	0.7	0.7	2	2.2	NP	6.2	NP	0.9	0.8	0.8	1.7	1.7
Manufacturing Yield	Low	Low	Low	High	High	NA	High	NA	Low	Low	Low	Med	Med

AR Airvac reflow 2nd time

R/R Rework/Replace

NP No part to begin with

X-ray After Assembly

X-ray inspection followed the daisy-chain continuity check to selectively verify package/assembly conditions. The 2D real time x-ray transmission system with up to 70° oblique angle views was utilized for this inspection. Figure 9 shows representative x-ray photomicrographs for the FPBGA432, marking a potential open with an arrow. Figure 10 shows additional x-ray photomicrographs with arrows pointing to shorts and potential opens.

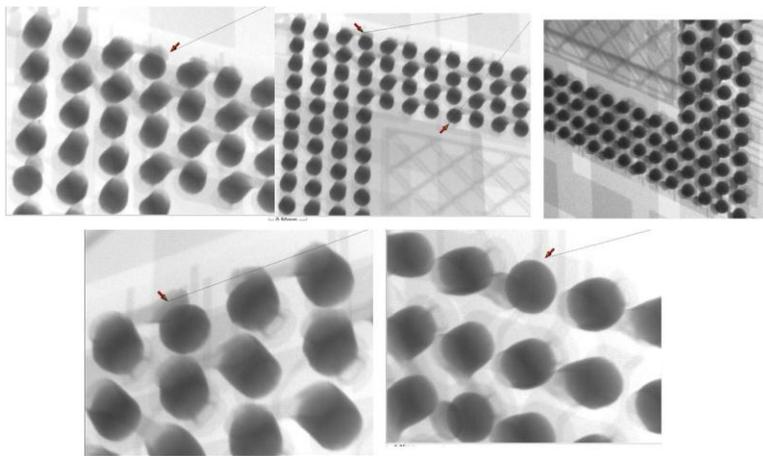


Figure 9 - As-assembled X-ray photomicrographs for the FPBGA432 attachments.

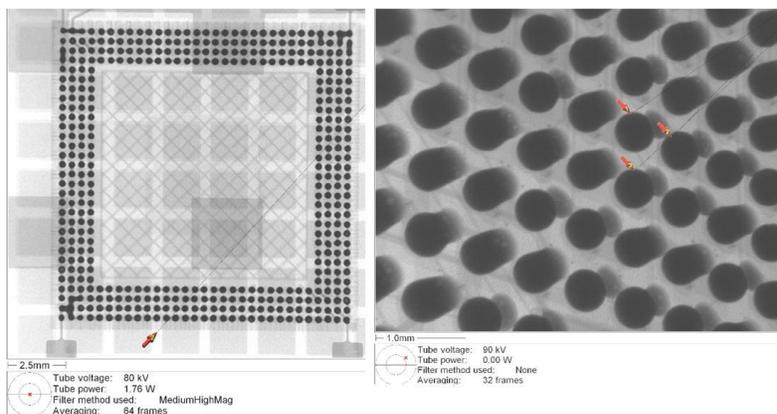


Figure 10 - Representative as-assembled x-ray photomicrographs for FPBGA432 attachments showing shorts (left) and open conditions.

The x-ray of PBGA676 shown in Figure 11 showed minimum voids with no apparent shorts or opens. Only one test vehicle was fully evaluated prior to thermal cycling. A comprehensive x-ray evaluation of all assemblies may have revealed defects in rare occasions similar to those observed for the FPBGA432 packages. This statement is given based on inconsistency in daisy-chain resistance values for the PBGA676 package assembly.

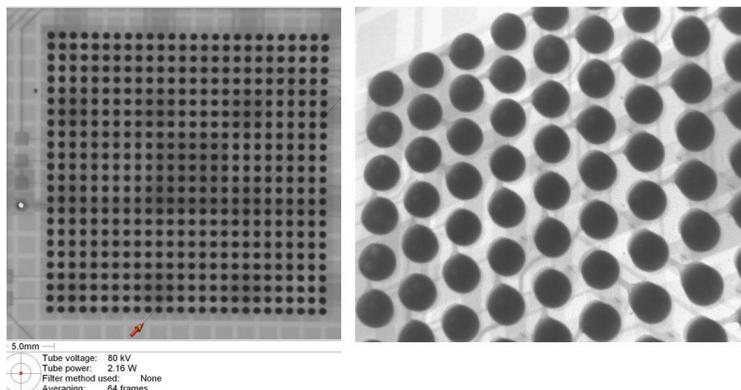
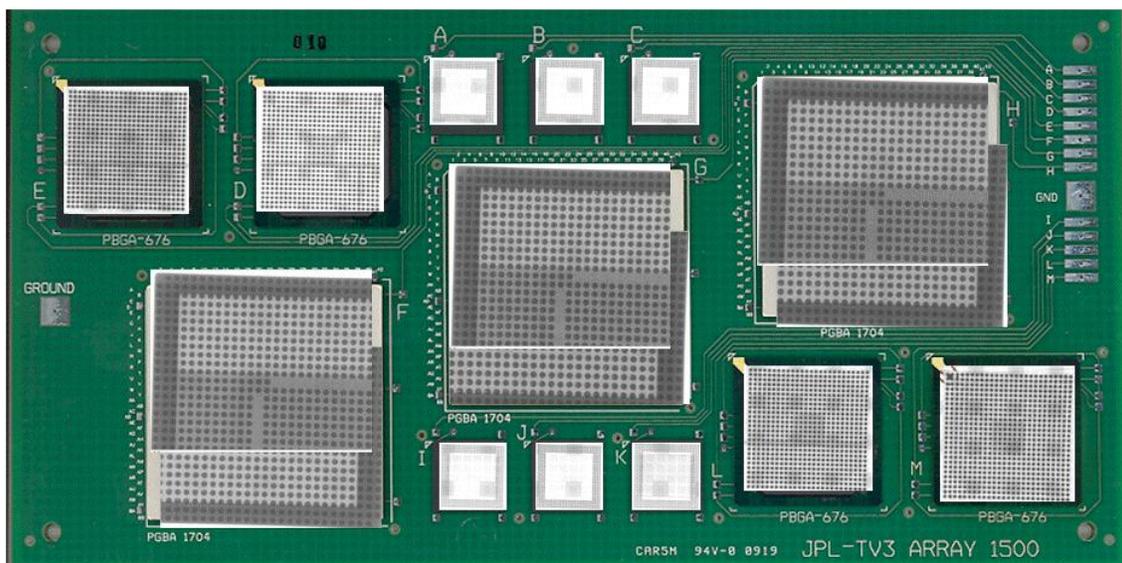
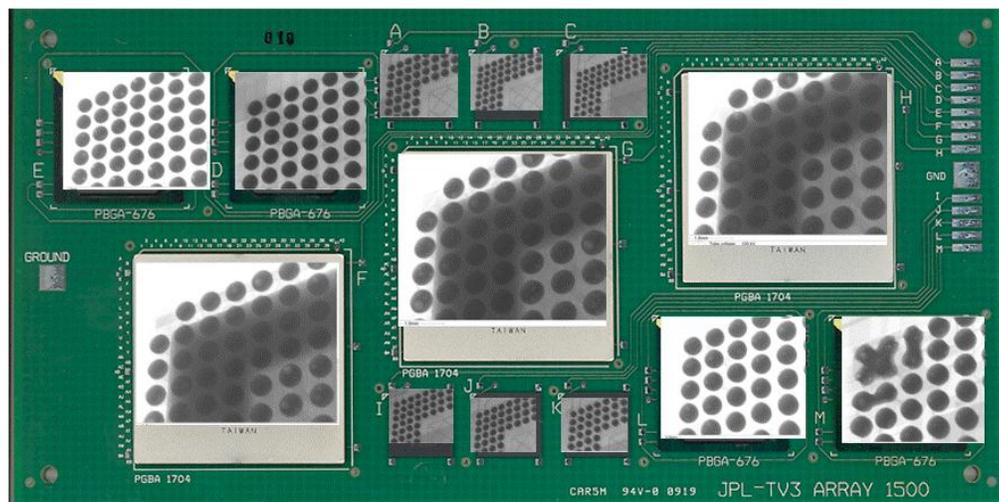


Figure 11 - As-assembled x-ray inspection of PBGA676.**After Thermal Cycling**

X-ray evaluation was also performed after temperature cycling for two assemblies when one of the FCBGA1704 packages revealed a daisy-chain open. A representative x-ray of the test vehicle for all parts laid on over their respective packages is shown in Figure 12. These x-ray photomicrographs further confirm the previous findings after assembly for the 432 I/O FPBGA packages. It also revealed shorts and potential opens due to manufacturing challenges for fine-pitch BGA surrounding the large FCBGA1704 package. For this specific test vehicle, only one out of four PBGA676 packages revealed open (location M) by daisy-chain continuity test after assembly. For this case, the daisy-chain continuity test result is in agreement with x-ray findings. However, daisy-chain continuity failure after thermal cycling identified for the FCBGA1704 could not be verified through x-ray evaluation at lower magnification. Further evaluation was carried out at a much higher x-ray magnification to determine if clear indication of failures could be identified. Figure 13 shows a representative x-ray of the top-right corner of packages at higher magnification, revealing more detail of shorts and potential opens where applicable. Figure 16 shows an x-ray of the FCBGA1704, location F, where failure was identified through daisy-chain evaluation. Again, no apparent damage or cracking was detected by x-ray. The photomicrographs, however, showed clearly the levels of voids—key advantage of x-rays—for solder balls and solder joints.

**Figure 12 - X-ray of package assemblies after thermal cycling laid over their respective packages showing their array configuration.****Figure 13 - X-ray of package assemblies after thermal cycle showing only the top right corner balls at high magnification for better representing damage and anomalies.**

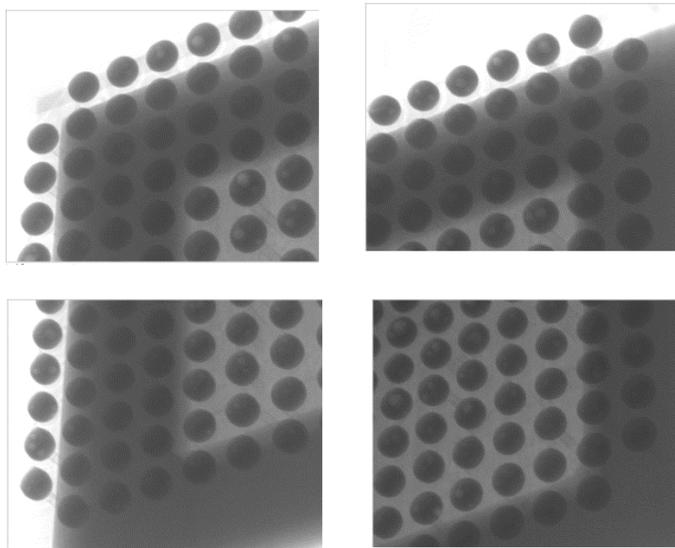


Figure 14 - X-ray of FCBGA1704 package assemblies after thermal cycle showing the corner balls at higher magnification for better representing damage and anomalies due to cycling. No damage could be detected, but it shows levels of voids. Note that this package showed daisy-chain open after cycling.

SEM Microscopy Characterization

Contrary to conventional package assemblies where solder joints can be inspected by optical microscopy at intervals during thermal cycling, this is not the case for FCBGA packages that require accessibility to periphery solder balls and special optical microscopes. The only known approaches are package/board daisy-chain development for monitoring or destructive test by dye-and-pry and x-sectioning evaluation. These approaches are not foolproof either since failure other than solder joint may cause false detection. Because of x-sectioning a limited number of balls, this destructive technique provides only damage indicators for those balls' x-section, which generally may also be representative of other balls.

After failure detection by daisy-chain monitoring, scanning electron microscopy (SEM) evaluation was performed. In addition, elemental analysis was performed using dispersive x-ray spectroscopy (EDS) to obtain semi-quantitative elemental results for the flip-chip solder alloys and interface interconnections. A representative FCBGA1704 specimen was cut from the TV, close to the package edge, in order to be able to mount the specimen on the SEM mounting fixture and rotate the sample for full characterization at higher magnifications. Figure 15 shows representative SEM photomicrographs for a ball of FCBGA1704 package prior to cross-sectioning at various magnifications. Solder alloy phases are revealed through using the backscatter feature of the SEM microscope. No gross microcracks, either within the balls or at the package interfaces, are apparent. For the flip-chip BGA, the outer rows may or may not represent the most severe stress condition; therefore, the SEM photomicrographs evaluation may possibly not be representative of internal damage, especially for ball interconnections at the package die periphery.

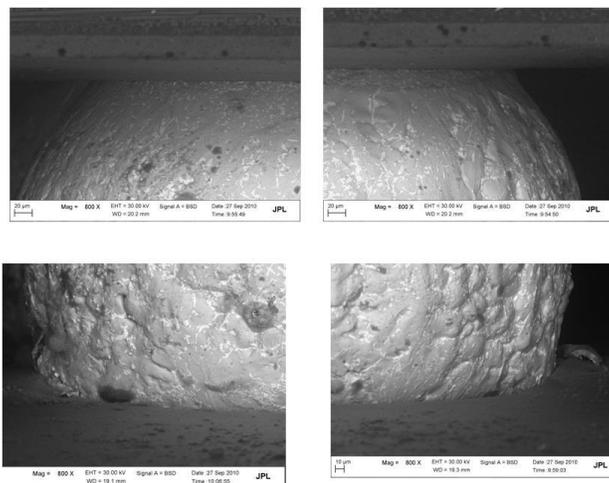


Figure 15 - SEM photomicrographs of a FCBGA1704 solder after thermal cycling and prior to cross-sectioning.

X-sectional Verification

After initial SEM evaluation, x-sectioning was performed diagonally through the center of the FCBGA1704 package in order to reveal substrate lay-up structure, heat sink attachment feature, flip-chip solder and underfill integrity, and solder interconnection damage levels at the package and board interfaces. Heat sink and lay-up configurations, including die and substrate thicknesses, affect board level thermal cycle reliability and therefore are characterized. Figure 16 shows a representative SEM photomicrograph of an x-sectioned FCBGA1704 package showing measurement values for various sections of the package, including flip-chip balls at the die and flip-chip balls at the package/board level. Flip-chip solder balls are much smaller than those at the package level and have about a four times lower gap than the BGA balls. It is also apparent that high-density substrate with two layers of filled microvias were employed for transition of low pitch flip-chip at the die level to the higher pitch at the package level.

Flip-chip solder ball alloy compositional uniformity within solder and at the die and substrate interfaces is shown in Figure 17. There is no apparent degradation after a number of thermal cycles even though daisy-chain open is detected. Microvias shown in the figure also appear to show no degradation. The underfill under the die appears to show minimum degradation. Figure 18 shows SEM photomicrographs of package solder balls and their interface integrity at the board and package interfaces. Note that the solder encloses the pad on the board since the board was designed as non-solder mask defined (NSMD) condition. This is not the case for the package that had a solder mask defined (SMD) pad. In addition, lead from tin-lead solder paste had diffused away from the board pad into the lead-free solder ball. It is not known whether this condition existed after assembly or tin-lead solder initially was segregated from lead-free alloy and lead was diffused later during thermal cycling.

Figure 19 shows x-ray elemental analysis along the center line of the package solder balls whereas Figure 20 shows x-ray elemental mapping for the solder ball. Elemental mapping for each element such as tin and lead are obtained through an EDS scan and are presented as different color intensity for visual observation. The solder is heavily distributed with tin having a minimum level of copper that is scattered throughout the solder ball. The silver element has to be accumulated specifically since it had no visual appearance; it was calculated to be about one percent, which is much lower than the expected four percent based on the SAC405 lead-free alloy composition.

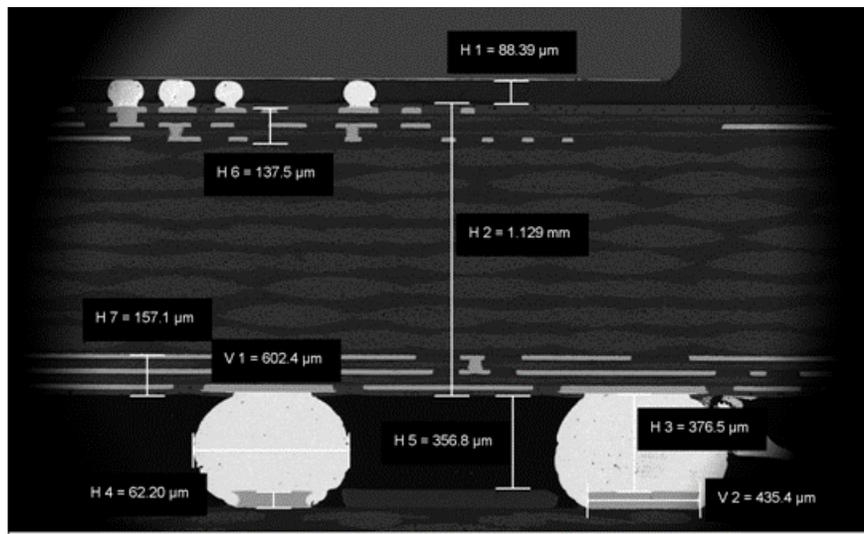


Figure 16 - Cross-sectional photomicrograph of FCBGA1704 assembly after thermal cycling showing flip-chip balls at the die and at the package/board levels and their sizes.

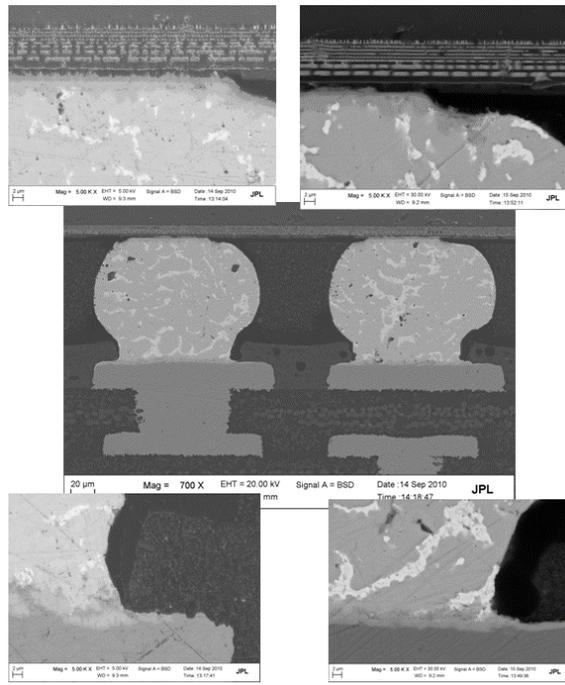


Figure 17 - Cross-sectional photomicrographs of FCBGA1704 assembly after thermal cycling showing detailed metallurgical features of flip-chip solder balls at the die level.

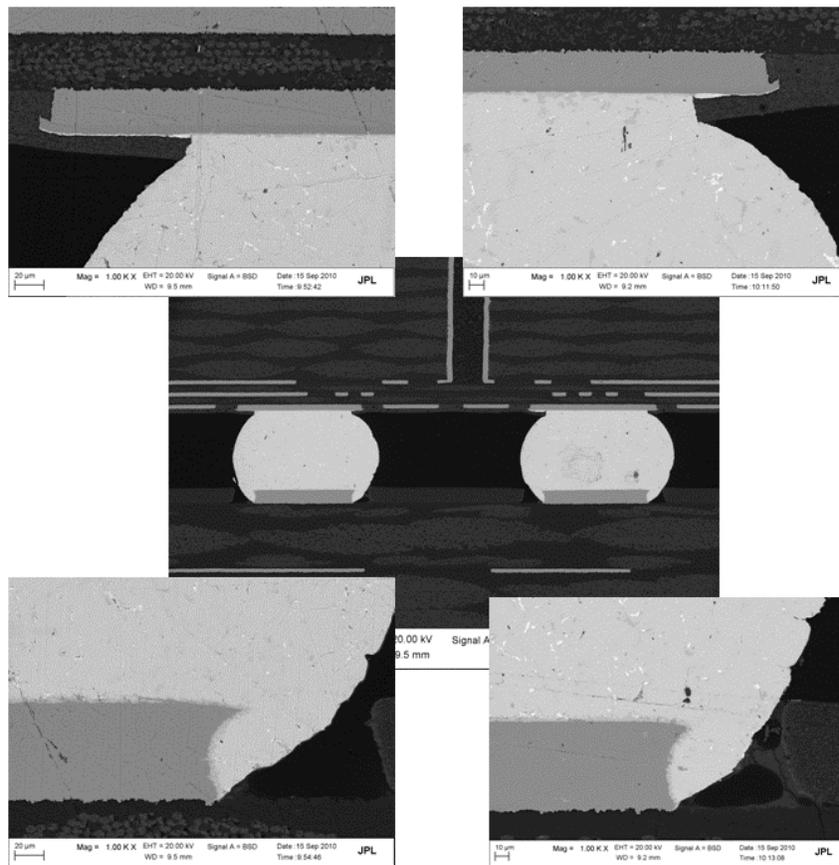


Figure 18 - Cross-sectional photomicrographs of FCBGA1704 assembly after thermal cycling showing detailed metallurgical features of flip-chip solder balls at the package/board level.

Conclusions

The conclusions, based on the results of thermal cycling with different profiles using limited flip-chip ball grid array (FCBGA) 1704 input/output (I/O) and other package assemblies, are as follows:

- FCBGA1704 with 1.0-mm pitch had acceptable solder paste print quality whereas FPGA432 with 04-mm pitch generally had unacceptable conditions.
- FCBGA1704 showed high assembly yield even when a ministencil was used for paste print and/or a rework station was used for reflowing solder paste whereas FPGA432 showed poor assembly yield.
- The two-dimensional (2D) x-ray system used in this investigation revealed shorts and, in some cases, apparent opens for PBGA676 and FPBGA432. It did not reveal, however, a possible open for the only FCBGA1704, which showed daisy-chain open after assembly.
- FCBGA1704 and PBGA676 with 1.0-mm pitch with acceptable quality after assembly showed no daisy-chain resistance failures to 200 thermal cycles under the four different thermal cycle conditions (-55° to $+100^{\circ}\text{C}$, -55° to $+125^{\circ}\text{C}$, and $-125^{\circ}/+125^{\circ}\text{C}$, and thermal shock cycle in the range of -55° to $+100^{\circ}\text{C}$). Results for FPBGA432 are not clear because of initial poor quality.
- FCBGA1704 showed minimum signs of damage after thermal cycling evaluated by cross-sectioning and SEM.
- FCBGA1704 with lead-free solder balls that assembled with tin-lead solder paste showed no apparent signs of segregation between the two solder alloys after thermal cycling evaluated by SEM and EDS mapping.
- The FCBGA1704 with 1.0-mm pitch located at the center of test vehicle, when subjected to drop loading of 485 g, failed after the first drop. This clearly shows sensitivity of large BGA packages to dynamic loading and high deflection deformation.
- The two-dimensional (2D) x-ray system used in this investigation did not reveal the level of solder damage or opens detected by daisy chain after thermal cycling.

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References

- [1] International Electronics Manufacturing Initiative (iNEMI), Research Priorities, 2005, pp. 11, www.inemi.org.
- [2] Fjelstad, J., Ghaffarian, R., and Kim, Y.G., *Chip Scale Packaging for Modern Electronics* (Electrochemical Publications, 2002).
- [3] Ghaffarian, R., "Chip Scale Package Assembly Reliability," Chapter 23 in *Area Array Interconnect Book*, eds. K. Puttlitz, and P. Totta (Kluwer Academic Publishers, 2002).
- [4] Ghaffarian, R., "BGA Assembly Reliability," Chapter 20 in *Area Array Packaging Handbook*, ed. K. Gilleo (McGraw-Hill, 2004).
- [5] Ghaffarian, R., "Characterization and Failure Analyses of Lead-Free Solder Defects," Chapter 10 in *Lead-Free Solder Interconnect Reliability*, ed. D. Shangquan (ASM International, 2005).
- [6] Ghaffarian, R., "Area Array Technology for High Reliability Applications," Chapter 16 in *Micro-and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging*, ed. E. Suhir (Springer, 2006).
- [7] Ghaffarian, R., "Reliability of PWB Microvia for High Density Package Assembly," *International Journal of Materials and Structural Integrity*, 2008, Vol. 2, No. 1–2, pp. 47–63.
- [8] Ghaffarian, R., "Thermal Cycle Reliability and Failure Mechanisms of CCGA and PBGA Assemblies with and without Corner Staking," *IEEE Transactions on Components and Packaging Technologies*, June 2008, Vol. 31, Issue 2.
- [9] Ghaffarian, S. Bagheri, H. McCormick, and I. Sterian, "Reliability of Lead-Free and Tin-Lead Solders for PBGA Assemblies," IMAPs RF Packaging Workshop, San Diego, 16–18 September 2008.
- [10] Bankeem, V.C., Ramkumar, S.M., Ghaffarian, R., "Thermal Shock and Drop Test Performance of Lead-Free Assemblies with No-Underfill, Corner-Underfill, and Full-Underfill," *The Proceedings of 60th IEEE Electronic Components and Technology Conference*, Las Vegas, NV, June 1–4, 2010.
- [11] Ghaffarian, R., "Area Array Package Trends and Assembly Reliability Failures for Tin-lead and Lead-free Solders," *Components for Military and Space Electronics Conference (CMSE)*, Los Angeles, CA, Feb. 11, 2010.
- [12] Evans, J.W, Evans, J.Y., Ghaffarian, R., Mawer, A., Lee, K., and Shin, C., "Monte Carlo Simulation of BGA Failure Distributions for Virtual Qualification," *ASME*, Hawaii, 1991.