Backplane Architecture High-Level Design

White Paper-Issue 1.0

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The backplane is the key component in any system architecture. The sooner one considers the backplane's physical architecture near the beginning of a project, the more successful the project will be. This white paper introduces the concept of a backplane High Level Design document and demonstrates the principle using a fictitious system architecture as an example.

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BACKPLANE ARCHITECTURE HIGH-LEVEL DESIGN

The backplane is the key component in any system architecture. The sooner you consider the backplane's physical architecture near the beginning of a project, the more successful the project will be. For any new backplane design, I always recommend starting with a High Level Design (HLD). It helps you capture your thoughts in an organized manner, and later provides the road map to follow for detailed design of the backplane. It also facilitates concurrent design of the rest of the system by other design disciplines.

For me, the HLD information is usually captured in a series of PowerPoint slides; but any other graphical based tool could be used. If it is already in PowerPoint, then drawings can easily be exported to a Word document. Later on in the design process, the drawings in the HLD document are reused in a more formal design specification document. The figures and illustrations, used in this white paper, are a perfect example of documentation reuse.

In the appendix, you will find an example of a backplane HLD document using PowerPoint. It is based on a fictitious system architecture used to demonstrate the principle.

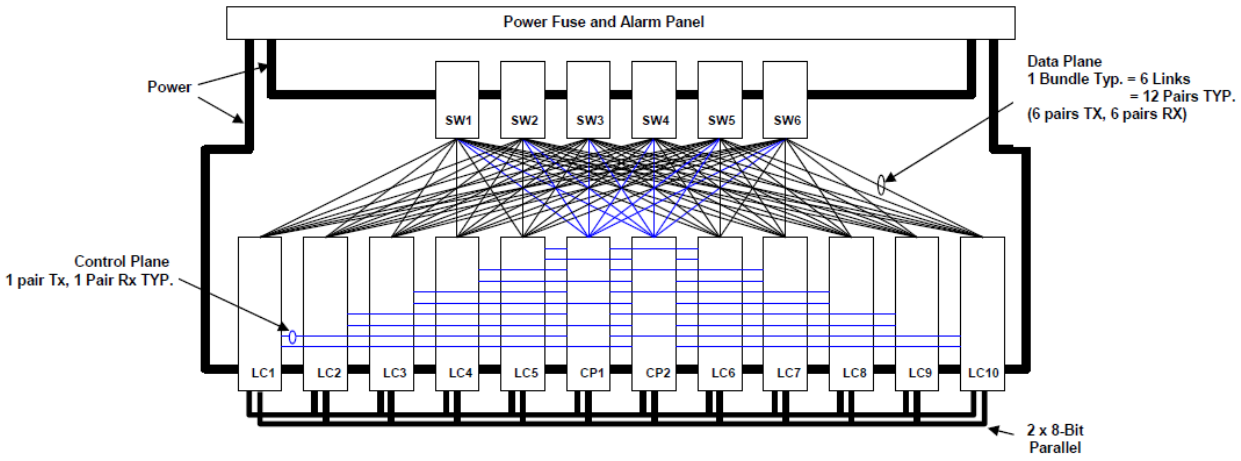


Figure 1 System high-level block diagram example.

Figure 1 is the system high-level block diagram we will use as reference. The architecture is a multi-star system with six fabric switch cards, two control processors and ten line cards. It is an example of what you might receive from the system architect at the beginning of a project.

One of the first things I do is capture the system architecture in a series of functional block diagrams. Each block diagram details how the respective circuit packs, or other components of the system, interconnect to one another; complete with the number of signal I/Os for that function.

Figure 2 is the system data path block diagram. It shows one possible way of how you would arrange the circuit pack blocks as they appear in a shelf and viewed from the front. Whenever possible, I like to arrange the blocks this way in all the block diagrams, because it presents a consistent look and feel throughout the documentation; from mechanical views; to connector placement; to route planning.

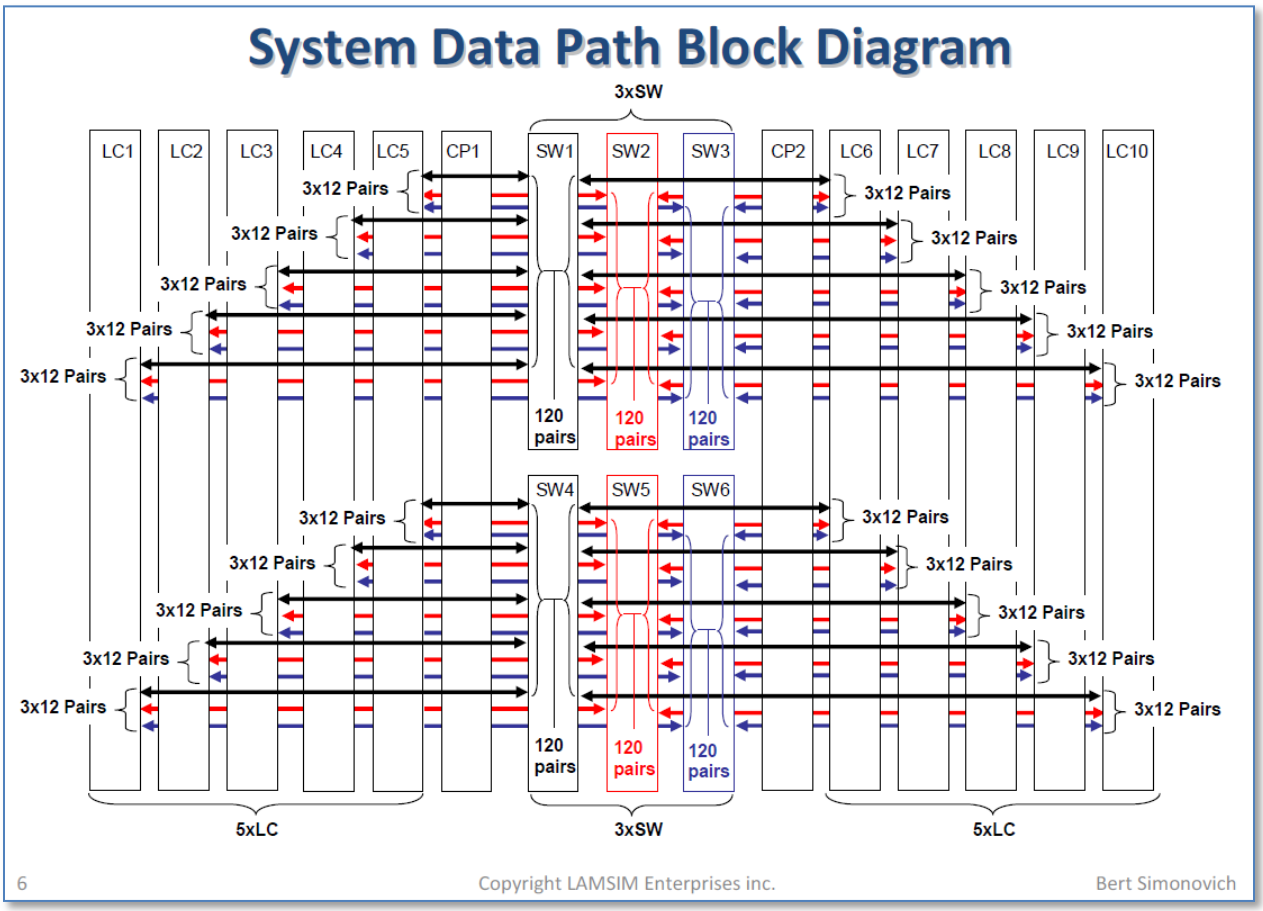


Figure 2 System data path detailed block diagram example.

The six switch cards (SW1-6) are half height fabrics, as recommended by the system packaging architect. Each switch card connects in a star configuration to ten line cards (LC1-10) using a bundle of six links, where one link consists of one transmit and one receive pair.

The control path block diagram is shown in Figure 3. It shows each control processor (CP1,2) driving one link of GigE to each line card and switch card in a star configuration. Also shown is the redundant low speed 8-bit parallel maintenance bus connecting each line card to both control processors.

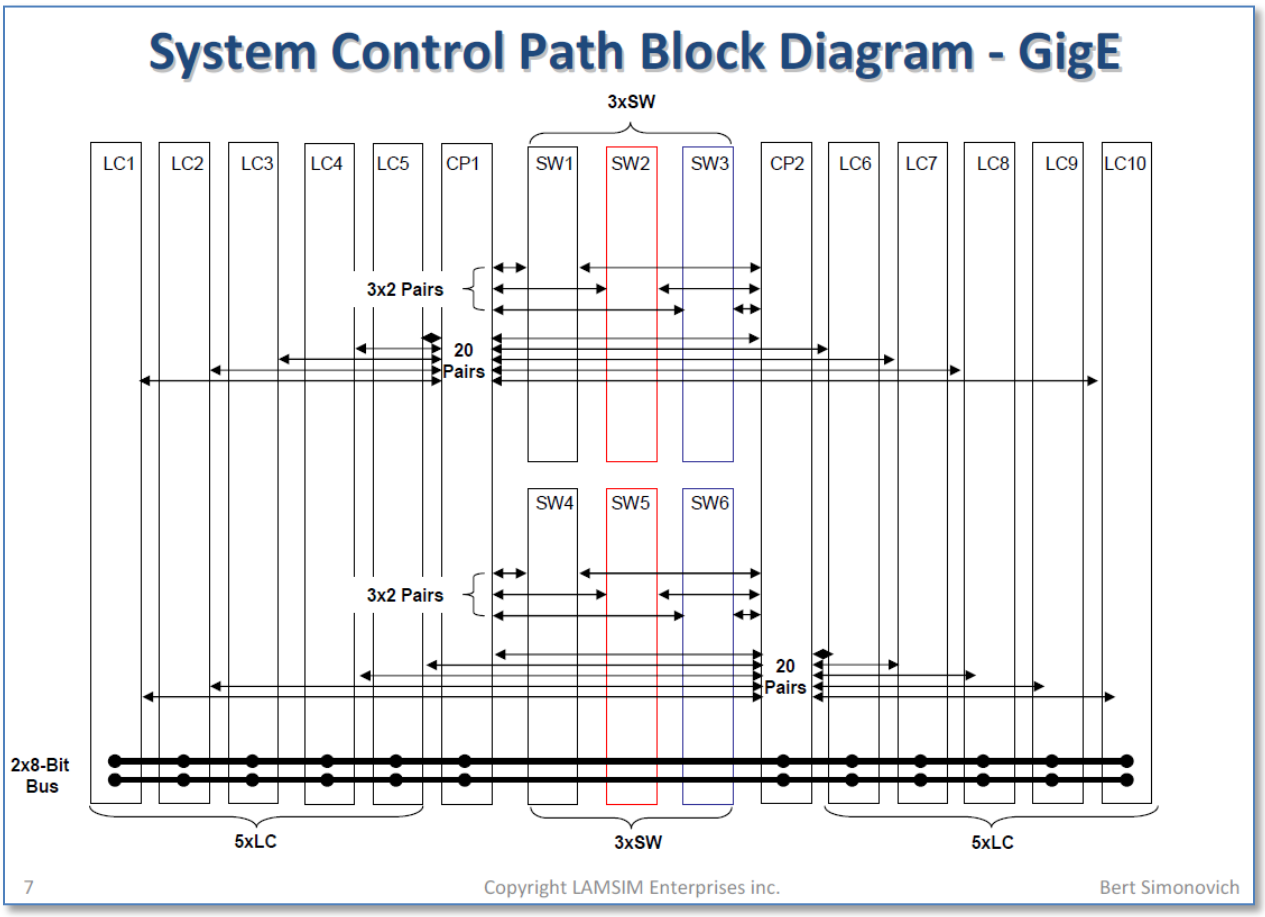


Figure 3 System control path detailed block diagram example.

This process continues until all functional blocks are captured. In our fictitious example, we have only shown two detailed block diagrams. In a real system, there will be more functional blocks to describe; like cooling control, power distribution, and alarms.

Preliminary Route Planning

After all the functional block diagrams are completed, a preliminary route planning exercise usually takes place. The idea here is to gain some intuition for the final routing strategy, and to uncover any hidden issues early that may surface down the road.

This is the most crucial step in any backplane design. Usually at this stage of the project, the system packaging architect is busy developing the shelf packaging concept. He (or she) is looking for feedback on connectors and card locations, so he can complete the common features drawing. This drawing defines all the x-y coordinates of all connectors and other mechanical parts on the backplane.

Figure 4 is an example of a preliminary routing plan strategy. The composite drawing shows the control plane, data plane, and maintenance bus. Each color represents two routing layers. The heavy black lines correspond to the high-speed data path bundles; routed completely from SW1 and SW4 to LC1-10. Notice

the partially routed heavy red and blue lines follow the exact same route plan as the heavy black lines, except they terminate to the respective color-coded SW cards. The beauty of this comes later; during the actual routing of the backplane. Because the routing is identical, except for the source and destinations, it is a simple copy and paste exercise to replicate the routing on five of the six layers. The only editing required is at each end of the links; a huge time saver when routing the final layout.

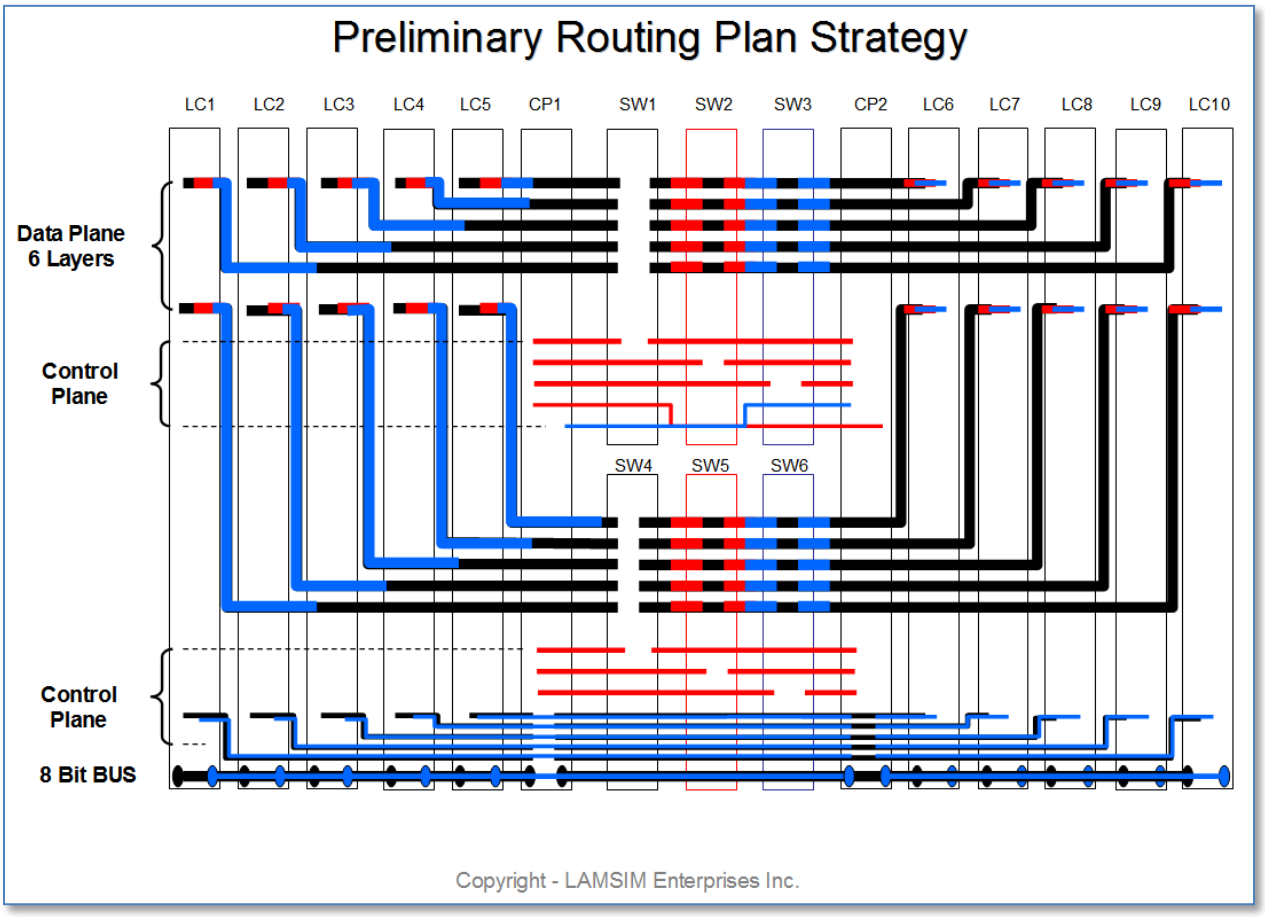


Figure 4 Preliminary route plan example. Each color represents two routing layers.

By choosing to bookend the six switch card array with the control processors, we are able to route the control plane tracks in the middle of the backplane, and on some of the same layers as the data plane routing. Any other location of these CP cards, would more than likely result in extra layers on the backplane, or cause routing issues on the line cards.

At this point, we are pretty confident the pack-fill arrangement of cards in the shelf will not pose any issues to the final routing. We can relay this information back to the mechanical architect, so he can move to the next step and start capturing the common features drawing.

Once the preliminary route plane is complete, a pin-list summary for each circuit pack is compiled using an Excel spreadsheet. The pin-list summarizes the minimum number of pins needed per circuit pack for the function. Later, it helps to drive the selection and number of connectors.

After completing the preliminary route planning exercise, and pin-list summary, you will gain a sense for:

- the number of routing layers you will need
- circuit pack connector signal grouping and partitioning
- connector selection criteria for density
- minimum vertical routing channel space needed between connectors
- worst case topologies for signal integrity analysis
- card-card pack-fill location in the shelf

Later on in the HLD process, and after the actual connectors have been selected and placed on a scaled common features drawing, a more detailed route planning exercise takes place.

Backplane Connector Selection

Large companies invest a lot of money and time to qualify a connector family. There is always strong pressure to reuse connectors from one system design to another because of cost. Qualifying a new connector is no trivial task. It takes a significant development effort to model, characterize and test the connectors. If you try to qualify a new connector, at the same time as designing a new system, you run the risk of delaying the overall program if serious issues develop along the way. Sometimes though, reusing the same connector just won't cut it. For whatever the reason, one day you will be forced to look at other connectors.

Choosing the right connector for any new system is the most important aspect for any backplane design; regardless if it is reuse of a previous connector, or looking at new ones. The connector is the lifeblood of the backplane because it ultimately drives minimum slot pitch and circuit board height. It must be capable of supporting current and next generation high-speed signaling standards, and be robust enough to withstand multiple insertions. Factors such as pin density, pin pitch, pairs per row, overall size, skew, and crosstalk are examples to consider in this process.

All modern high-speed connector families, available in the market today, are designed with differential signaling in mind. For backplane applications, there is a male and female portion of the connector. The male portion, also known as the header, is usually assembled on the backplane, and the female is assembled on the circuit pack.

The male portion is a collection of straight pins; organized in rows and columns, and pressed into a plastic housing. Sometimes metal shields are used, between rows or columns, to mitigate crosstalk. The ends of the pins, inserted into the backplane, are usually compliant pin technology. They are meant to press-fit into the via holes. Soldering connectors into a backplane is almost never done; mainly due to the requirement of reparability in the field. Compliant pins, when pressed into via barrels, are more reliable than soldering because they provide a better gas tight seal, and thus, prevents any oxidation from forming.

The female half is usually a right angle connector; which allows the circuit pack to plug in perpendicular into the backplane. Sometimes straight versions are available for mezzanine applications; where the circuit pack plugs in parallel with the backplane.

A series of spring contact pins are assembled into wafers, and later assembled into plastic housings; with a preset number of wafers per connector. Often shields are included to mitigate crosstalk. To keep costs to a minimum, a single wafer design is used in multiple connector configurations. To increase pin density, a series of connectors are assembled, side-by-side, onto boards.

Most connector vendors label their connectors as columns and rows as shown in the left half of Figure 5. The columns are the wafers containing the number of pins per wafer. When the circuit pack plugs vertically into the backplane, the connectors are viewed as if they were rotated by ninety degrees. Because of this, it is more practical to re-label the connector, as shown in the right half of the figure, when creating the symbols for the PCB layout.

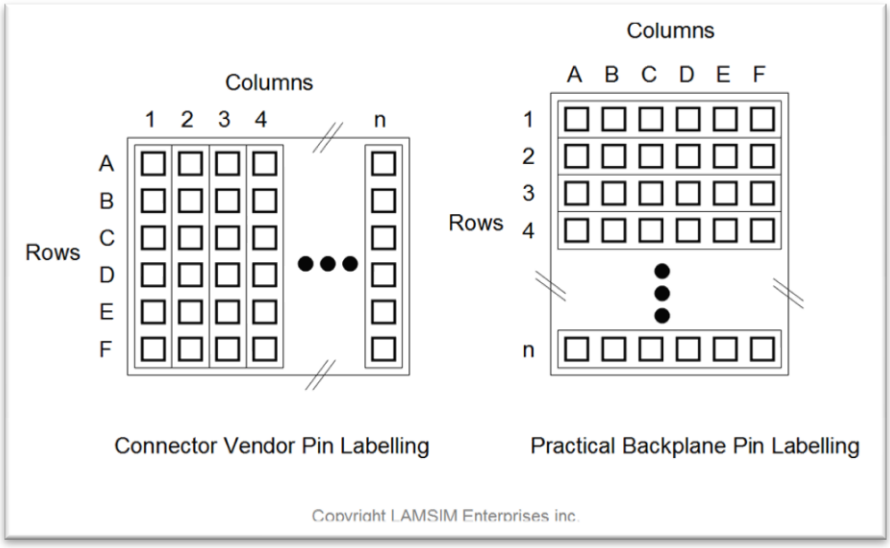


Figure 5 Vendor connector pin labeling vs practical pin labeling example.

Figure 6 is an example of two PCB footprints. Each one illustrates the pair arrangements of two different kinds of connector designs. Normally, there are ground pins separating the pairs, but they are not shown here for clarity. The most common configuration has the pairs arranged within the same wafer row as shown on the left. I like to call this an “edge-coupled” footprint. A “broadside-coupled” footprint, as shown on the right, has the pairs straddled between adjacent rows.

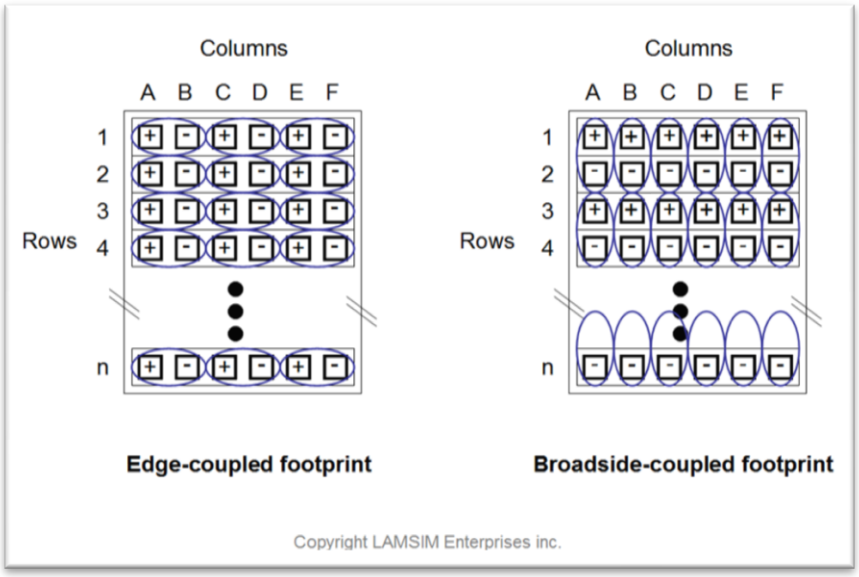


Figure 6 Edge-coupled connector footprint vs broadside coupled connector footprint.

Edge-coupled designs allow tighter coupling of the pairs through the connector due to the physical construction of the wafers making up each row. Shielding between rows is easier because they can be built in as part of the wafer assembly. On the down side, there is usually a small amount of skew between the positive and negative pins. Because of this, you need to make up the difference in the PCB routing, by extending the length of track going to the shortest pin-path of the pair.

As systems demand more and more functionality in less and less space, broadside-coupled designs allow for a higher pair density per linear inch, compared to edge-coupled designs. On the down side, extra layers are required to break out from the connector footprint, and inter-pair shielding can be more complicated; leading to higher cost. Shrinking bit times, due to increasingly higher bit rates, demand that you pay close attention to intra-pair skew throughout the channel. Intra-pair skew causes mode conversion; leading to signal degradation, and increased EMI. Maintaining equal intra-pair skew through the connector is a big plus.

When you break out of the connector, the rule of thumb is one layer for every differential pair. For example, a four-pair-per-row connector will need four layers if you break out in one direction only; two layers if you break out symmetrically each side.

After reviewing how the high-speed serial link data path bundles break out from the switch card in Figure 4, we see that two pairs route to the left and two pairs route to the right. This implies a four-pair-per-row connector is optimum for minimum layer count.

Based on this assessment, and from past experience, the connector I chose for this design example is a Tyco “Tin-man” four-pair-per-row connector as shown in Figure 7. It is a recent addition to Tyco’s family of high speed connectors and is rated up to 10GB/s.

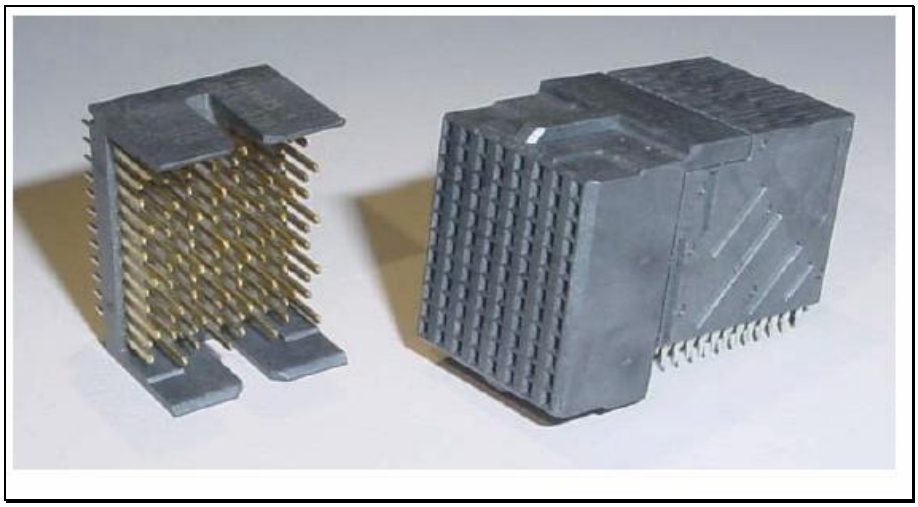


Figure 7 Tyco Tin-man 10GB/s connector.

Figure 8 shows the tin-man footprint breakout pattern and pin assignment chosen for the switch card. For pin groups, the convention I like to follow throughout the document is red for Tx, and blue for Rx wherever possible. Here, the red tracks are one layer, and the blue tracks are another layer.

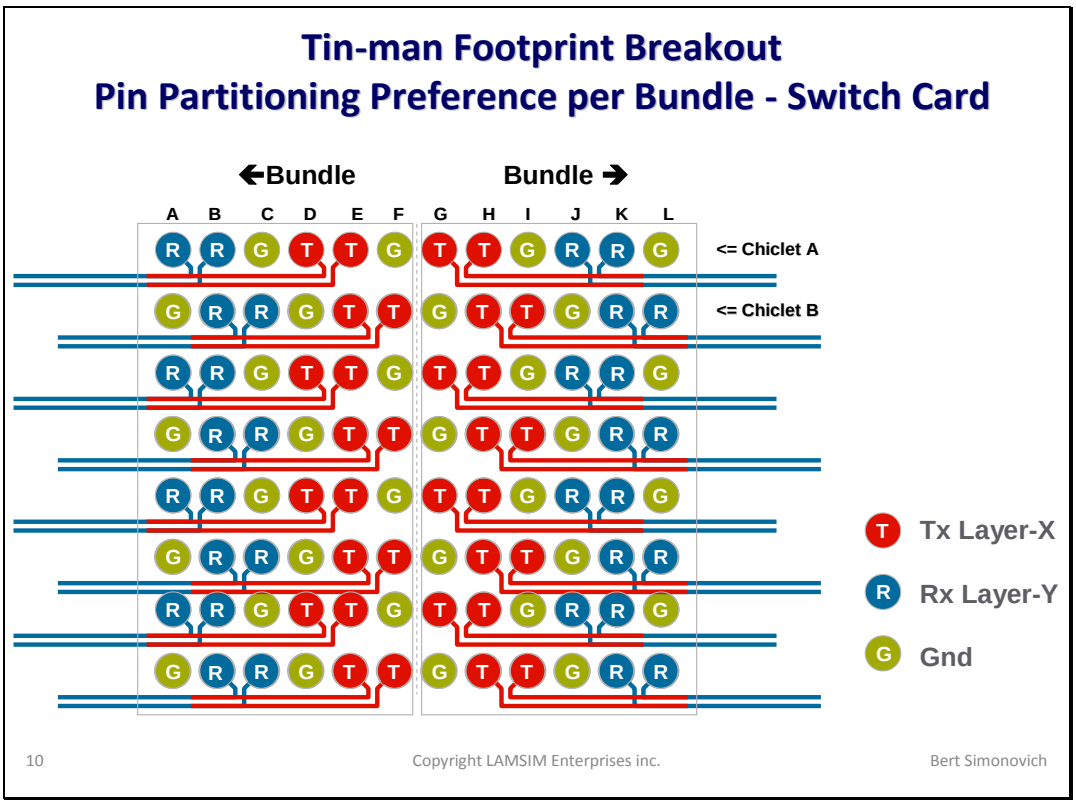


Figure 8 Tin-man connector footprint and breakout for Switch Card.

Differential Pair Trace Geometry

Backplanes, by their nature, are large structures and generally have fairly long track lengths. At high frequencies, the AC resistance increases due to skin effect losses of the copper traces. Because of this, we usually try to have the widest trace as is practically possible. They are often wider than you would normally have on circuit packs.

The row-to-row pitch, and via hole size of the connector footprint, determines the maximum trace width for horizontal routing through the connector field. Figure 9 illustrates the horizontal routing space available through the Tin-man connector footprint.

Anti-pads are the cut-outs in the planes allowing the plated via hole to pass through without shorting. To minimize excess via capacitance, and make vias as transparent as possible, we usually try to maximize the anti-pad size; but still allow reasonable sized traces to route through the channel and be covered by a reference plane.

After doing some sensitivity analysis on trace loss, and via impedance, due to anti-pad dimensions, we end up with a reasonable solution. In this case, the best differential pair geometry is 7-9-7 mils; where 7 mils is the trace width and 9 mils is the space between them.

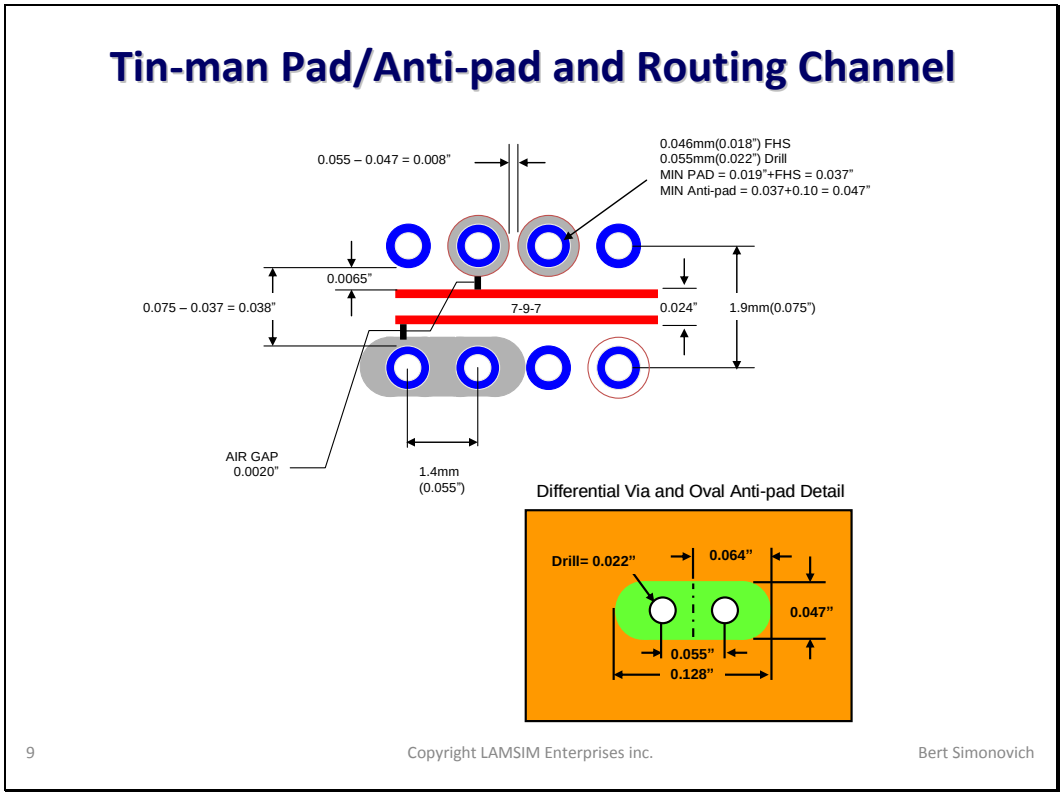


Figure 9 Determining horizontal routing channel through Tin-man connector field

Preliminary Stack-up

In any high-speed serial link architecture, the data plane links are the most critical signals. They are the ones that usually define the total number of routing layers for the final PCB stack-up. When we include four layers, for redundant power distribution, to the six routing layers, the minimum number of layers for the backplane will be eighteen layers as shown in Figure 10. To meet the target differential impedance of 100 Ohms, a 2D field-solver is used to solve for the dielectric thicknesses between reference planes.

The right half of the figure gives counter-bore details. Also known as back-drilling, it is a procedure used to minimize via stubs, which is a killer for multi-gigabit serial links. After the PCB has been fully fabricated, the pre-defined via holes are drilled again to a predefined depth with a larger drill bit; removing the plating of that portion of the hole. The counter-bored depth is usually specified to stop one layer before the signal layer to keep, as long as it is 8 mils or better. For our stack-up, the maximum stub is nominal 9 mils.

Press-fit, or compliant pin connectors, require a minimum depth to make reliable electrical contact, and to maintain mechanical integrity. Because of this, any high speed signal layers, within this minimum depth, will end up having a longer than optimal stub. Traditionally, a PCB stack-up needs a symmetrical construction above and below the horizontal center to prevent warpage during soldering. For thick, passive backplanes, this is not so much of an issue, because there is no soldering of components.

Here we take advantage of an asymmetrical stack-up; stacking all the power layers near the top layer to build up a minimum thickness. When we do this, the six high-speed routing layers are past the minimum depth, and as a result, all vias will have a maximum stub length of 9 mils after counter-boring.

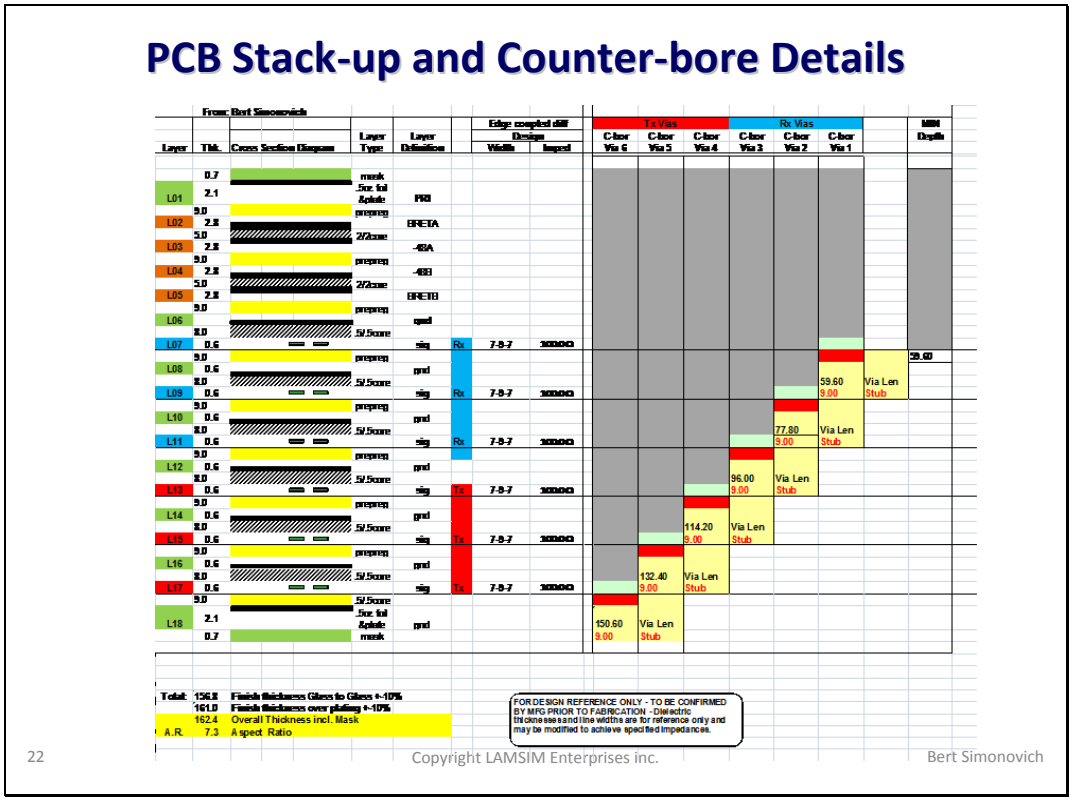


Figure 10 18 layer PCB stack-up and counter-bore details.

Detailed Route Plan

Usually, around this time in the project schedule, the mechanical architect has put together a preliminary common features drawing, showing the preliminary connector placement. For our particular example, the common features drawing would look something like Figure 11.

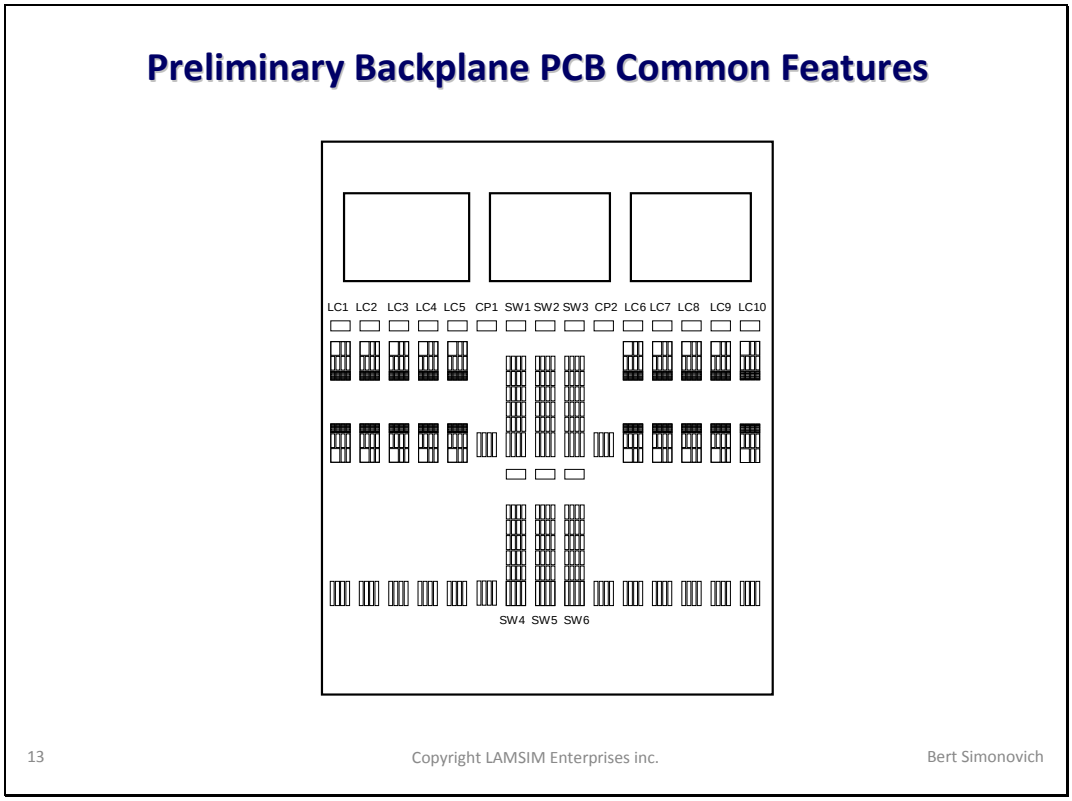


Figure 11 Preliminary common features drawing example showing rough placement of connectors.

We use this drawing as a template to do a more detailed routing plan analysis. By studying the preliminary route plan and pin-list, we can come up with a strategy to organize and partition the signals within the connector, and perform a more detailed routing analysis. This process usually takes a couple of iterations before it is optimum. Eventually, we end up with a more detailed routing plan as summarized in Figure 12.

Each illustration represents two routing layers per drawing. One layer is for Tx and the other is Rx. To minimize crosstalk between Tx and Rx via pairs in the connector footprint, all Rx layers are on the lower numbered layers (shortest vias) as per the stack-up in Figure 10.

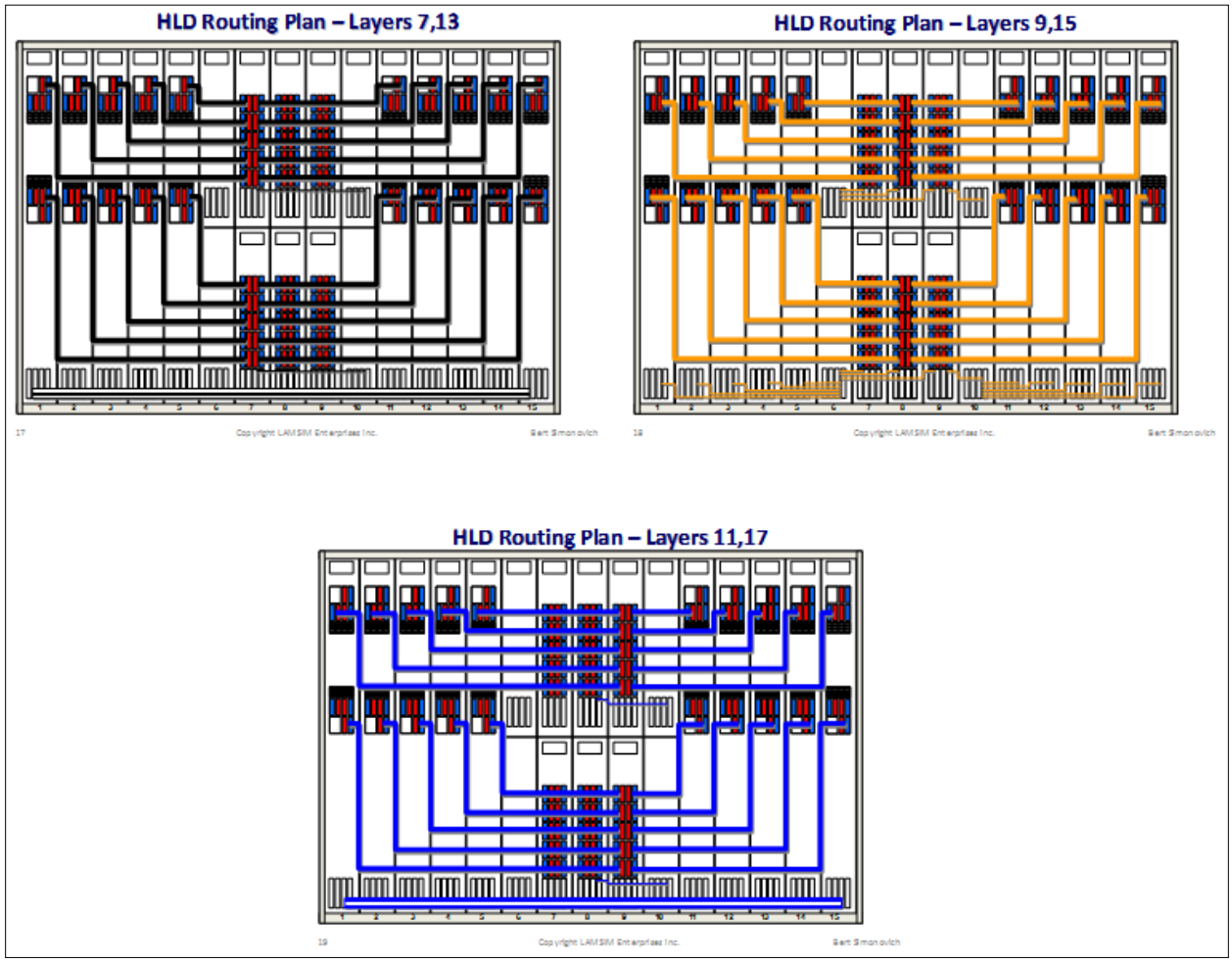


Figure 12 Detailed route plan example

Vertical Routing Channels

Before we sign-off on connector placement and route plan, we need to verify there is enough space between connectors for the vertical routing channels. Otherwise, this may be a deal breaker for the chosen connector; slot pitch; total number of layers; or even the whole system packaging concept. If you do not have enough space here, there will be compromises needed somewhere else to accommodate it. The worst case scenario is doubling the number of layers or choosing a higher cost connector.

An example of vertical routing channel analysis is shown in Figure 13. A 2D field solver is used to help set the minimum pair-pair spacing to satisfy the crosstalk budget. In our case, an inter-pair spacing of 20 mils, gives a backward crosstalk coefficient (Kb) of 0.56%.

The analysis shows we need 278 mils to route six differential pairs of track. Since there is 435 mils available for vertical routing between connectors, there is more than enough space to spread the pairs further apart and reduce Kb.

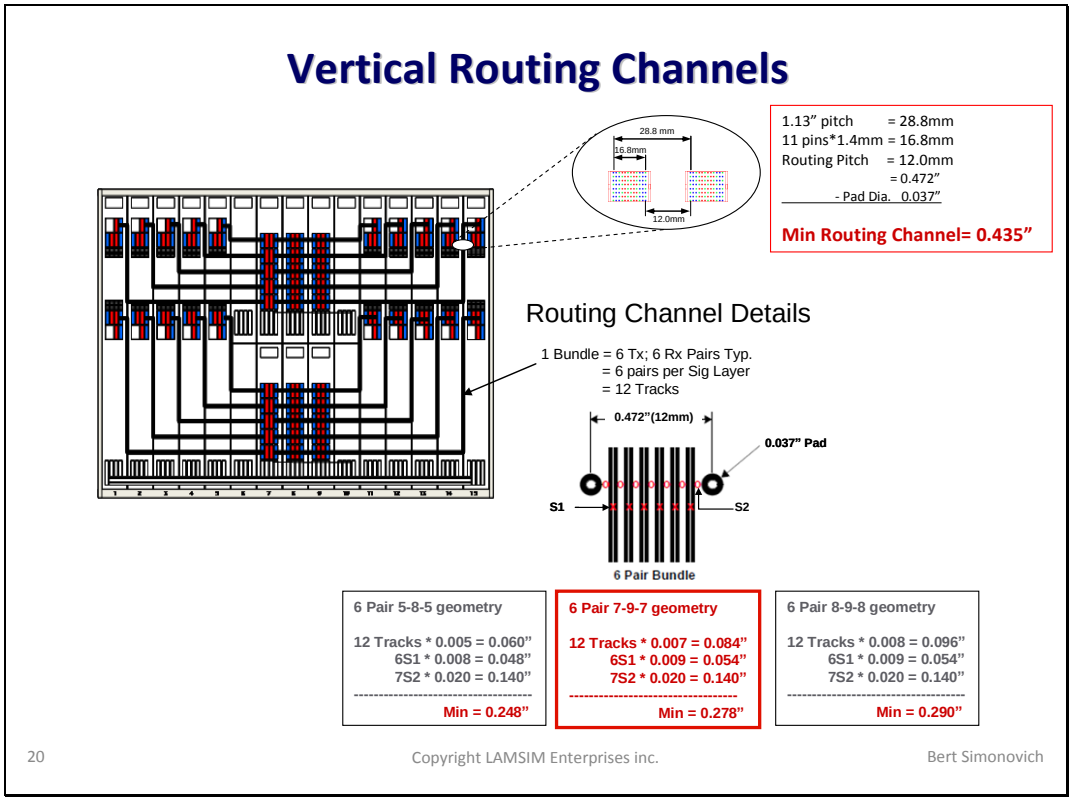


Figure 13 Vertical routing channel analysis example.

Signal Integrity Analysis

Finally preliminary channel simulations must be done before we can sign-off on the backplane physical architecture concept. Now that we have done all the detailed routing analysis, on a scaled common features drawing, we can easily establish several topologies to analyze.

One example of a worst case channel is highlighted in Figure 14. During this stage, we use Manhattan distance to estimate trace lengths. The topology shown assumes 6 inches of tracks on the plug-in cards, and 12 inches for the backplane. To complete the analysis, I normally do a similar topology for each layer for min/max backplane length.

At this point I use equations to calculate impedances for the connector via footprint, and procure connector models from the vendor. The topology is captured and simulated in a circuit simulator; like my favorite, Agilent ADS.

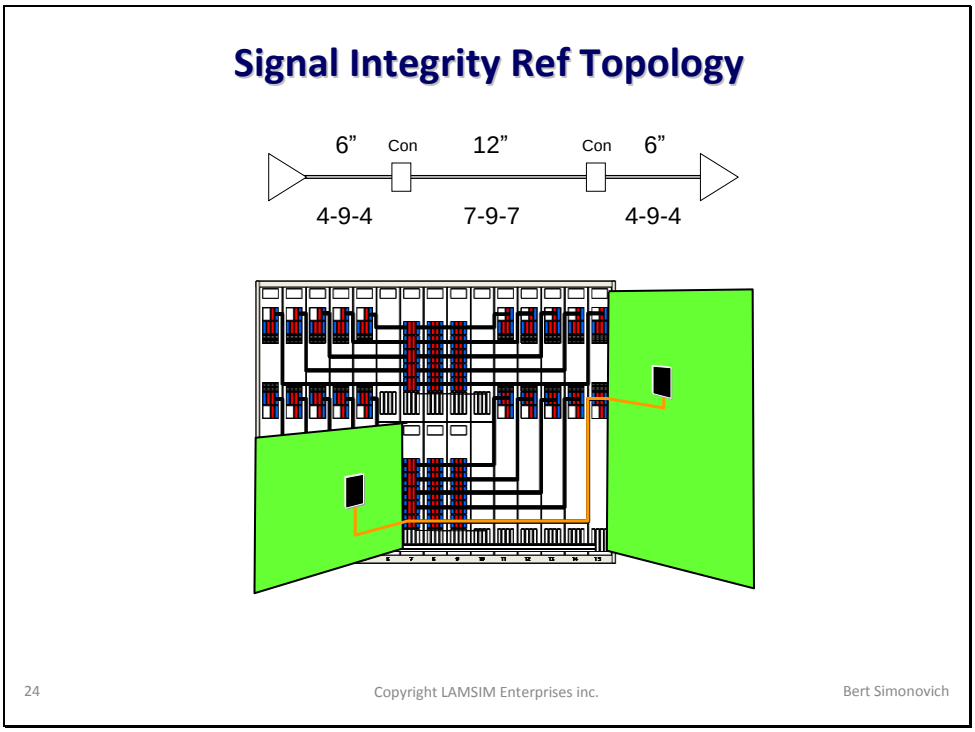


Figure 14 Example of worst case topology for signal integrity analysis.

An example of the circuit topology, and simulation results are summarized in Figure 15. The topology was simulated at 10GB/s. The S-parameters are compared against the IEEE 802.3 10BaseKR spec. You would normally do this for every topology of interest. Later on, during the detailed design phase of the program, I would get 3D models of the vias built and use actual routed lengths from the backplane and circuit pack cards to confirm the design.

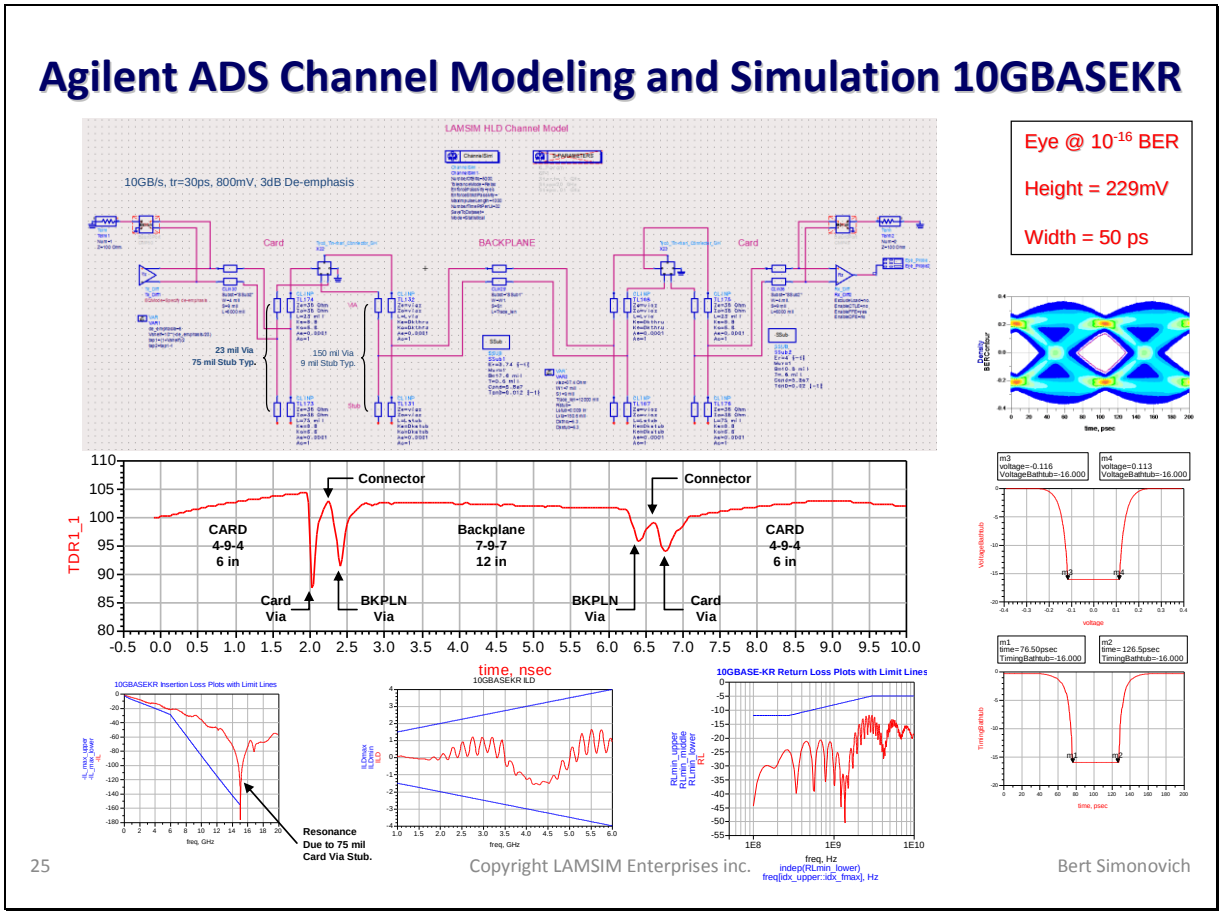


Figure 15 Agilent ADS topology modeling and simulation results example.

Summary and Conclusion

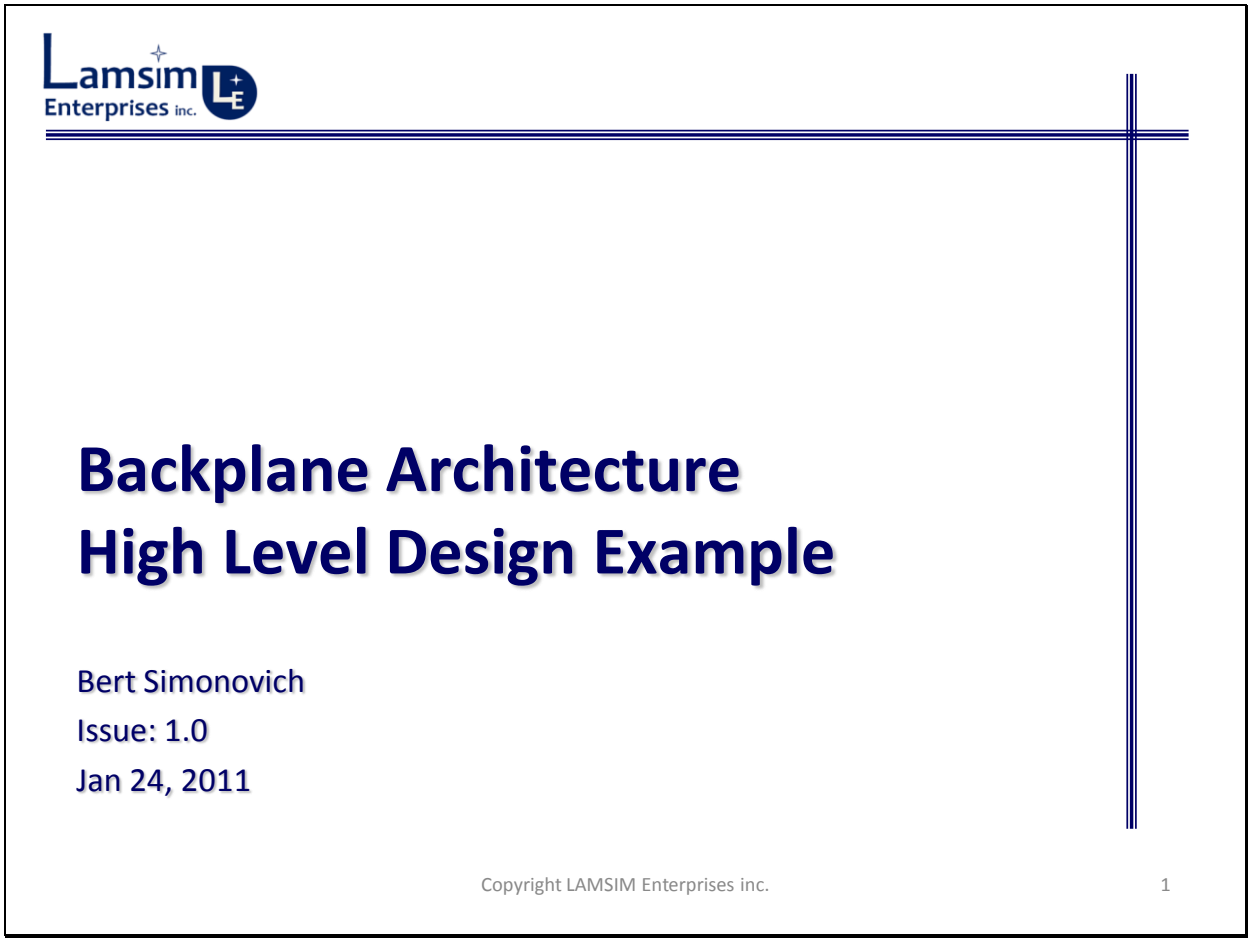
In this sample document, we have demonstrated the principles and merits of a backplane High Level Design methodology used by LAMSIM Enterprises inc. Hopefully by now, you can appreciate the backplane can be a complex beast to design, and get it right the first time. For help with your next high-speed design challenge, contact us through our web site at: www.lamsimenterprises.com .

Bibliography

Lambert (Bert) Simonovich graduated in 1976 from Mohawk College of Applied Arts and Technology in Hamilton, Ontario, Canada as an Electronic Engineering Technologist. Over a 32 year career at Bell Northern Research and Nortel, he helped pioneer several advanced technology solutions into products and has held a variety of R&D positions; eventually specializing in backplane design over the last 25 years. He is the founder of LAMSIM Enterprises inc.; providing innovative signal integrity and backplane solutions. He is currently engaged in signal integrity, characterization and modeling of high speed serial links associated with backplane interconnects. He holds two patents and (co)-author of several publications including an award winning DesignCon2009 paper related to via modeling.

Appendix:

The originals can be found on our web site; www.lamsimenterprises.com.



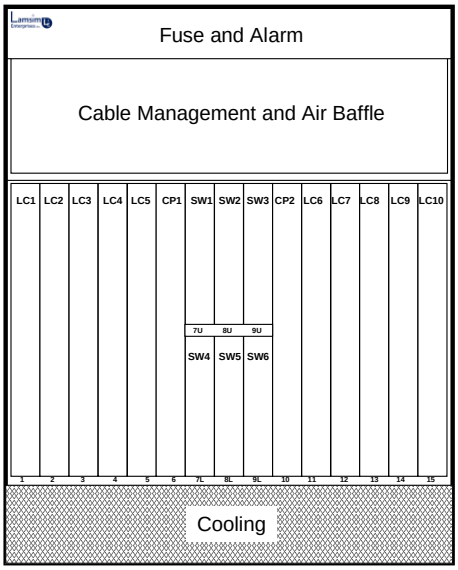
Record of Release

1. Jan 24, 2011: Issue 1.0 - Initial Release.

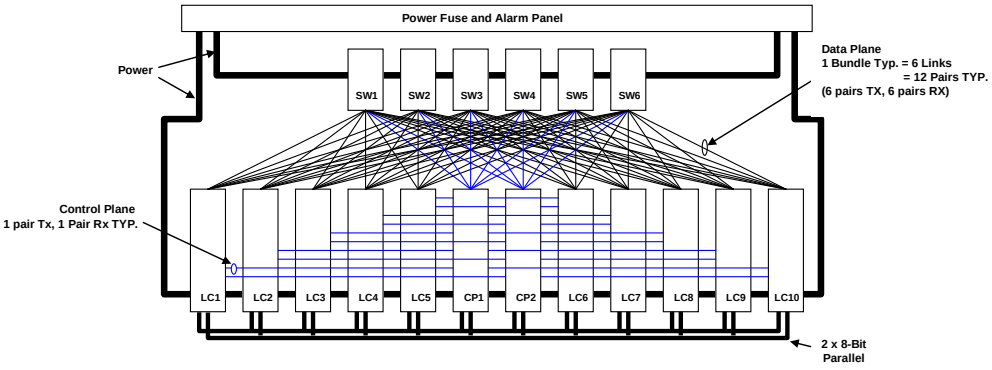
Summary and Caveats

1. This is a sample document intended to demonstrate the principles of Backplane High Level Design Methodology used by LAMSIM Enterprises inc. for a fictitious system architecture.
2. Throughout this document, 1 link = 1Tx&1Rx Pair = 4 Wires.
3. High-speed routing analysis based on TYCO Tin-man connector family.
4. Power distribution and routing analysis not shown since it follows a similar process.
5. Backplane: 18Layer; thickness = 182 mil +/-10%
6. Backplane signal integrity analysis assumes:
   - Plug-in card: 20Layer; Thickness = 114 mil +/-10%
   - 10 GB/s (802.3 10GBaseKR) spec.
   - Backplane via stubs have been counter-bored or back-drilled to minimum 9 mils.
   - Longest Via (150.6 mil); max back-drilled stub (9mil) for Backplane
   - No back-drilling on plug-in cards Shortest Via 3 (23mil); longest stub (75 mil)
   - Plug-in card trace geometry: 4-9-4; Nelco N4000-6
   - Backplane trace geometry 7-9-7; Nelco N4000-13EP

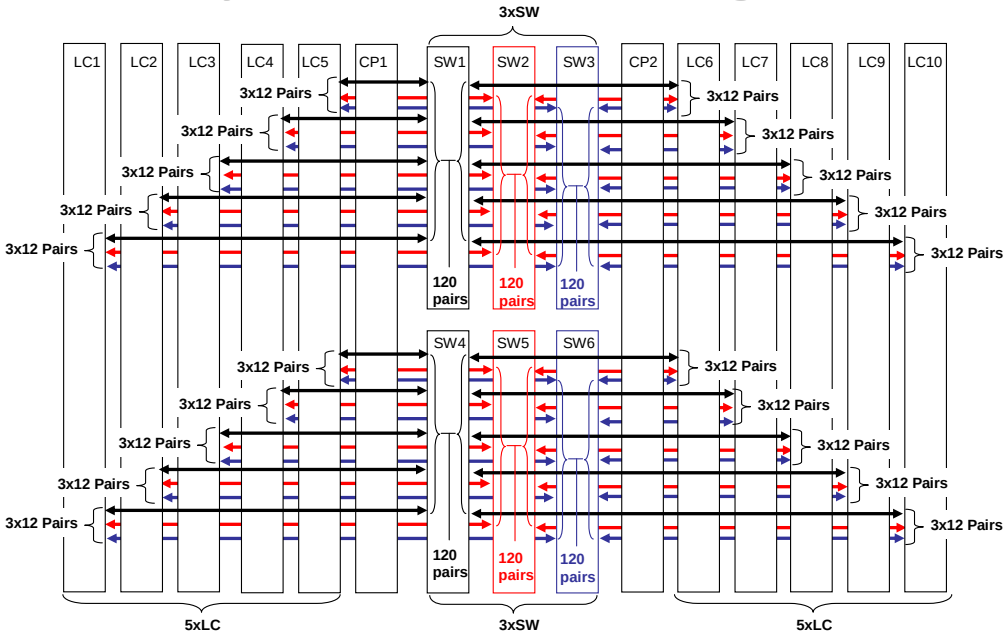
Shelf Slot Numbering and Pack-fill



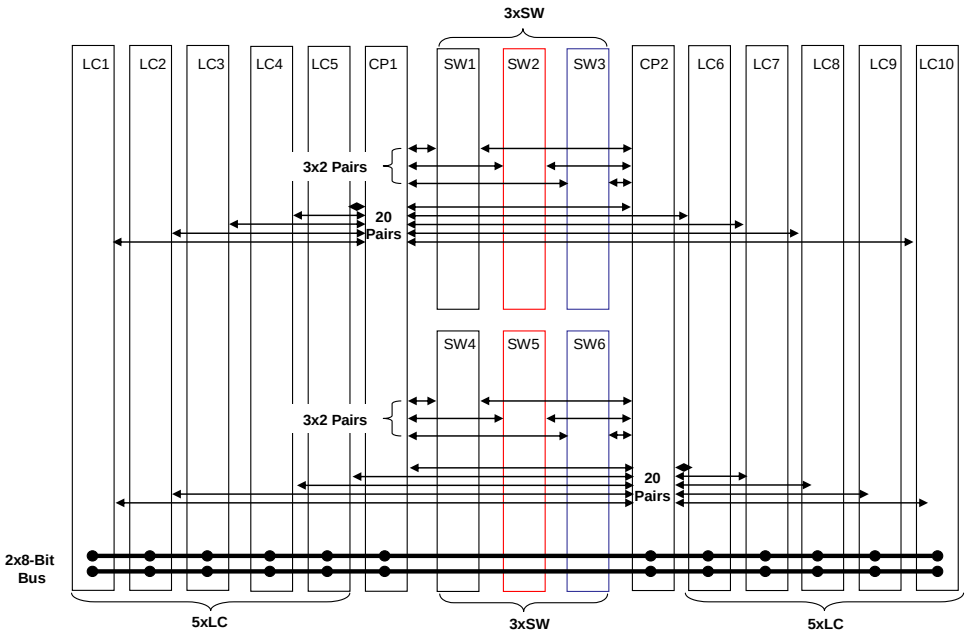
System Block Diagram



System Data Path Block Diagram

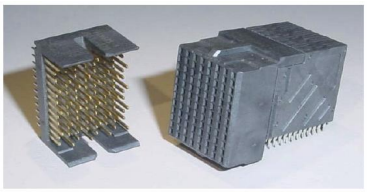


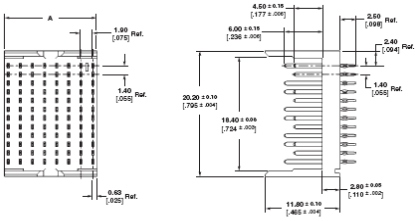
System Control Path Block Diagram - GigE



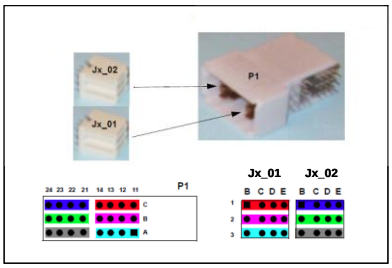
Backplane Connectors

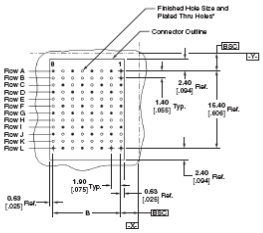
Tyco Tin-Man 4-Pair per Row Connector



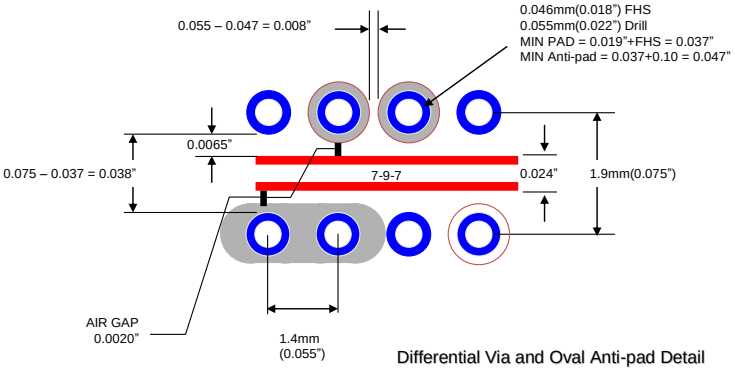


Tyco Power Connector

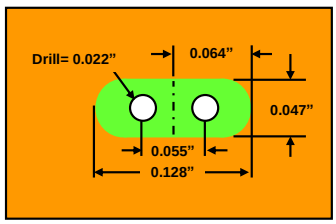




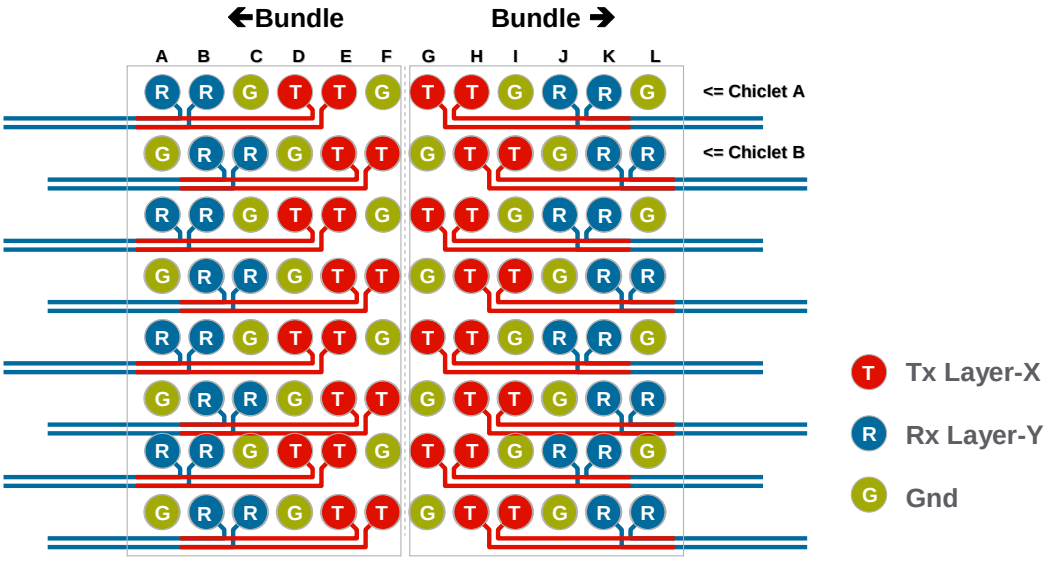
Tin-man Pad/Anti-pad and Routing Channel



Differential Via and Oval Anti-pad Detail



Tin-man Footprint Breakout
Pin Partitioning Preference per Bundle - Switch Card



ETSI (ETS 300 119-4: January 1994)

Dimensions for subracks mounted in miscellaneous racks/cabinets	(NOTE 2)				
H = height	C	n x 25			
W1 = overall width over flanges	C	535 (NOTE 1)		535	
W2 = width	C	450		500	
W3 = mounting centre distance	A	515 (NOTE 1)		515	
R = mounting position	C	12,5 + n x 25		12,5 + n x 25	
S = mounting	A	n x 25		n x 25	
D1 = mounting depth (front)	C	rack 300 deep	rack 600 deep	rack 300 deep	rack 600 deep
		40	75	40	75
D2 = mounting depth (rear)	C	240	470	240	470

NOTE 1: Subracks with dimensions W1 =485 and W3=465 may be fitted into miscellaneous racks (ETS 300 119-3 [4]) by the use of adaptors.

NOTE 2: A = Actual dimension.

Tolerances needed for W3 and S are specified in IEC 917-2-2 (see Annex B).

C = Coordination dimension.

NOTE 3: n = 0, 1, 2, 3...(the value of n can be different for H, R and S).

Definition: A coordination dimension is a reference dimension used to coordinate mechanical interfaces. This is not a manufacturing dimension with a tolerance.

An aperture dimension is a special coordination dimension for a usable space between features.

An actual outside dimension corresponding to a coordination dimension can only decrease.

An actual inside dimension corresponding to an aperture dimension can only increase.

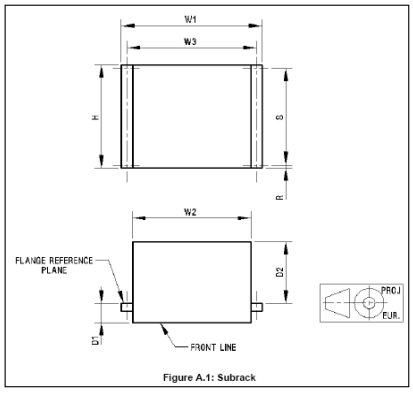
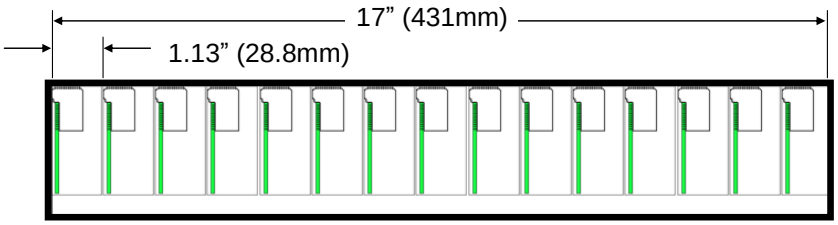


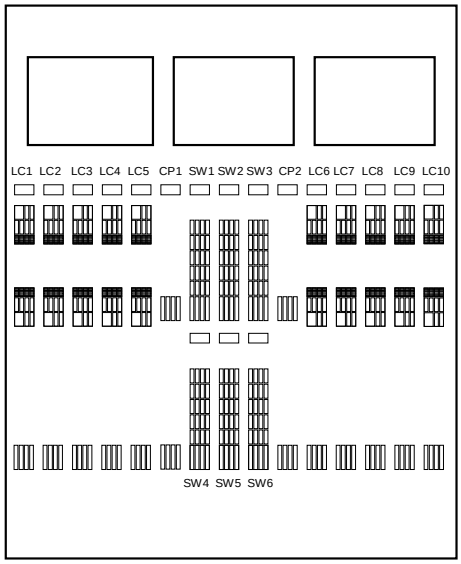
Figure A.1: Subrack

Slot Pitch Determination

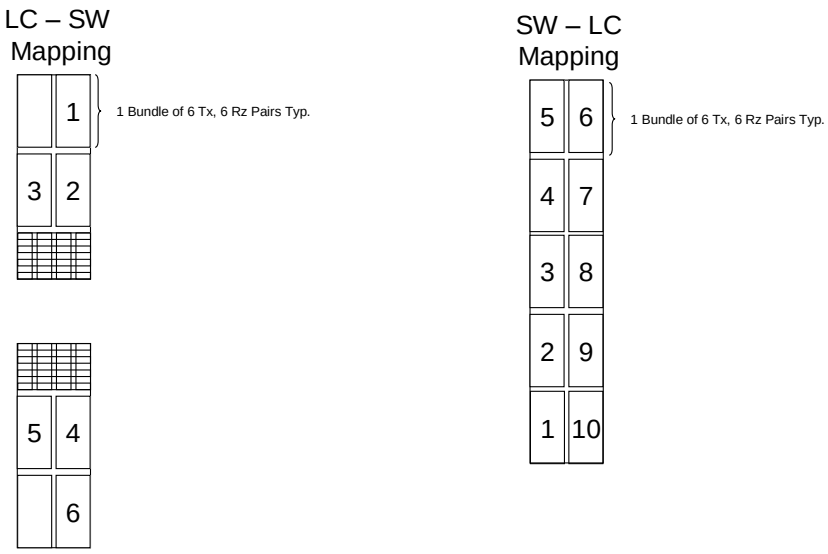


Pitch = 17”/15 cards = 1.13” (28.8mm)

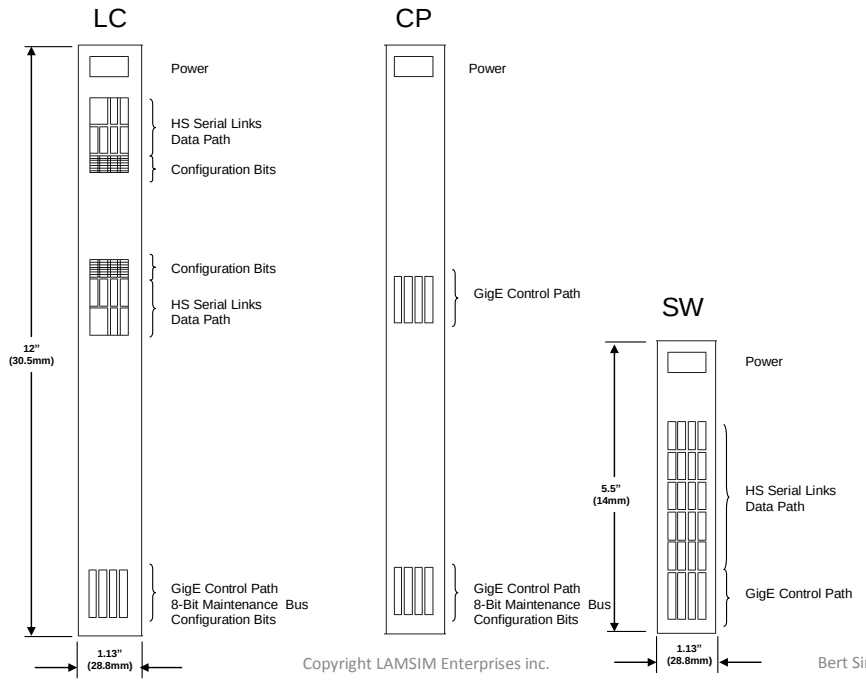
Preliminary Backplane PCB Common Features



Line Card / Switch Card Link Bundle to Slot Mapping



Card Size and Connector Signal Partitioning

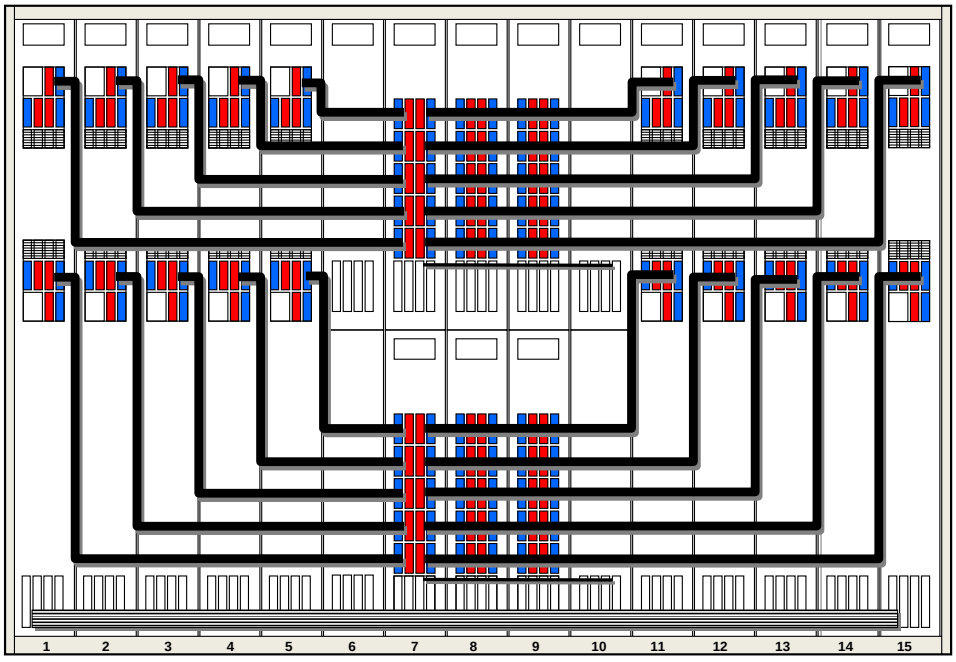


Pin List

	A	B	C	D	E	F	G
1		Circuit Pack					
2	**Function**		**CP**	**LC**	**SW**		
3							
4	HS-Links		0	72	120	pairs	
5	GigE		32	4	4	pairs	
6		subtotal	**32**	**76**	**124**	**pairs**	
7							
8		subtotal	**64**	**152**	**248**	**pins**	
9							
10	Maintenance Bus		16	16	0	pins	
11							
12							
13	Power		24	24	24	pins	
14							
15		**Total**	**104**	**192**	**272**	**pins**	
16							
17							

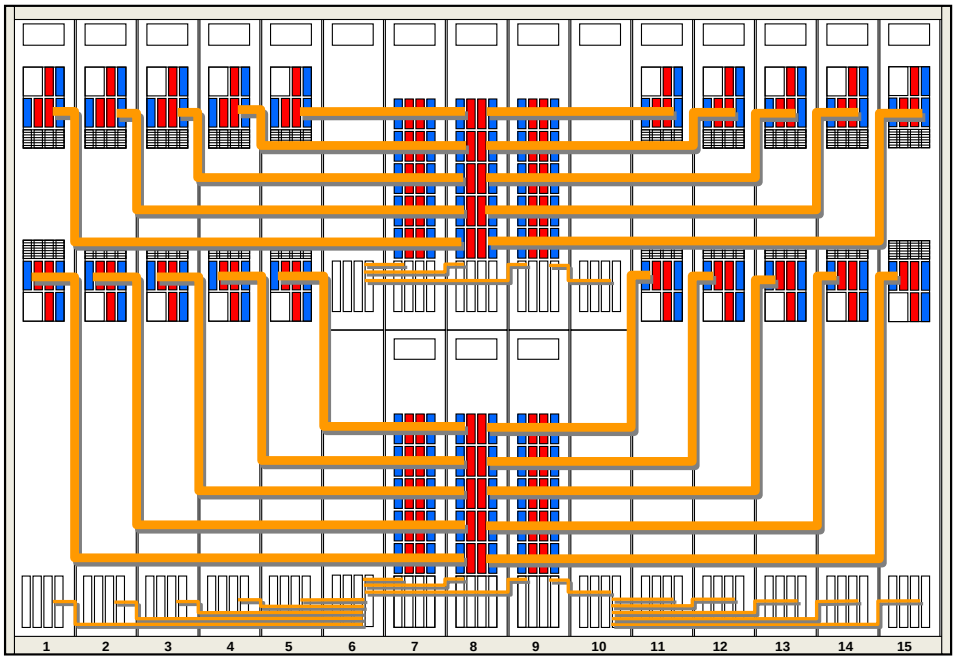
16 Copyright LAMSIM Enterprises inc. Bert Simonovich

HLD Routing Plan – Layers 7,13

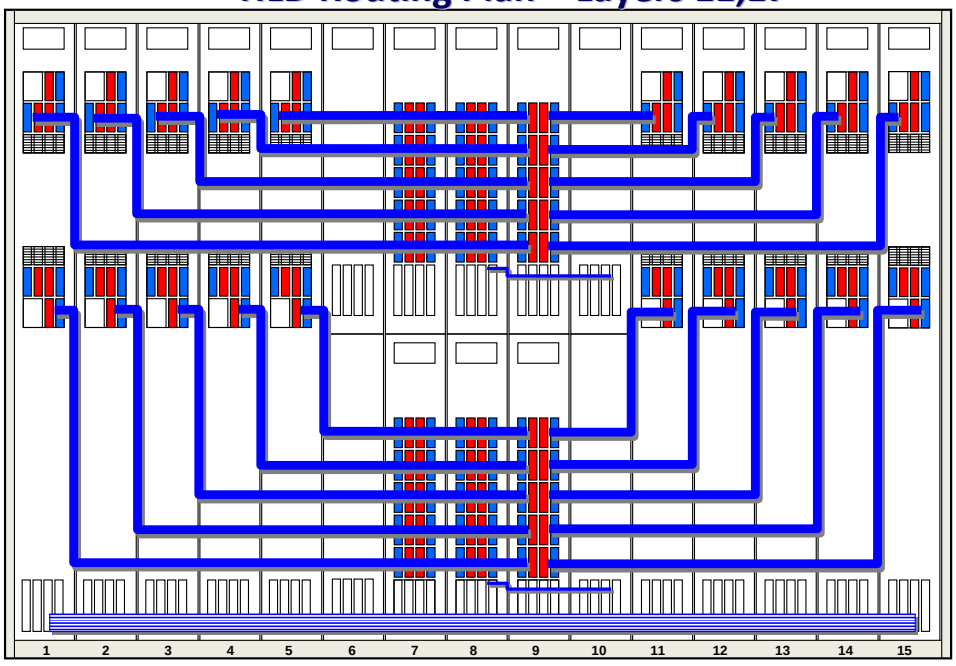


17 Copyright LAMSIM Enterprises inc. Bert Simonovich

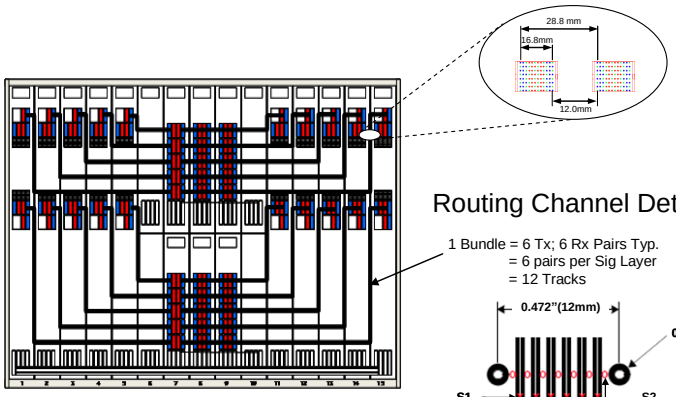
HLD Routing Plan – Layers 9,15



HLD Routing Plan – Layers 11,17



Vertical Routing Channels

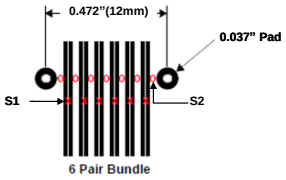


1.13" pitch = 28.8mm
11 pins*1.4mm = 16.8mm
Routing Pitch = 12.0mm
= 0.472"
- Pad Dia. 0.037"

Min Routing Channel= 0.435"

Routing Channel Details

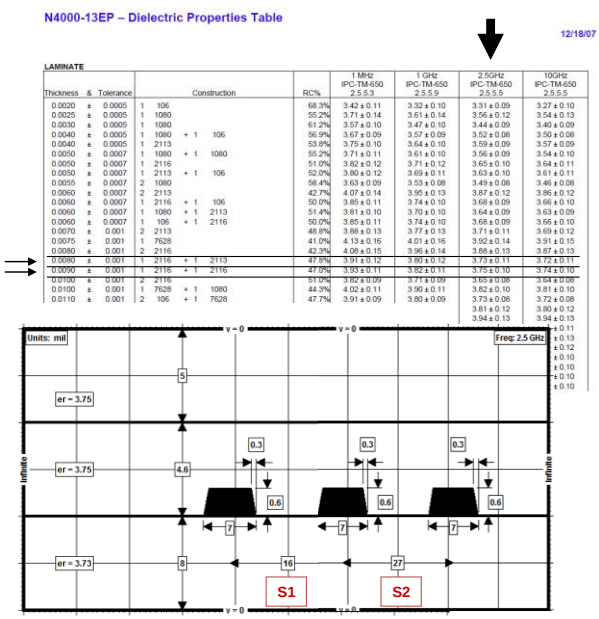
1 Bundle = 6 Tx; 6 Rx Pairs Typ.
= 6 pairs per Sig Layer
= 12 Tracks

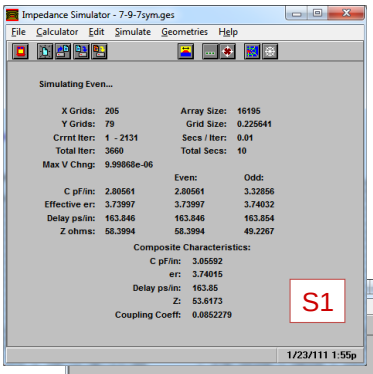


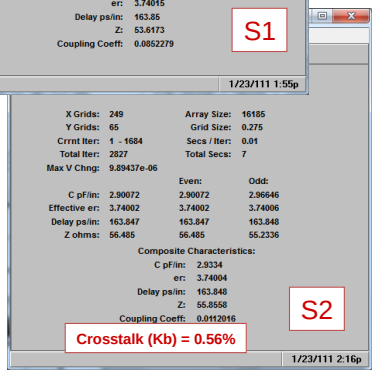
6 Pair Bundle

6 Pair 5-8-5 geometry	6 Pair 7-9-7 geometry	6 Pair 8-9-8 geometry
12 Tracks * 0.005 = 0.060"	12 Tracks * 0.007 = 0.084"	12 Tracks * 0.008 = 0.096"
6S1 * 0.008 = 0.048"	6S1 * 0.009 = 0.054"	6S1 * 0.009 = 0.054"
7S2 * 0.020 = 0.140"	7S2 * 0.020 = 0.140"	7S2 * 0.020 = 0.140"
Min = 0.248"	Min = 0.278"	Min = 0.290"

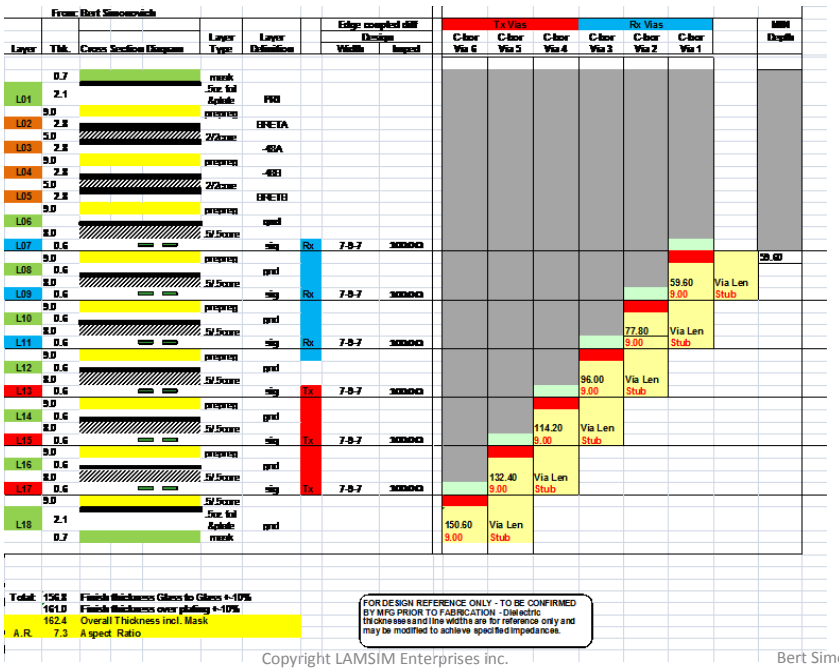
Backplane 7-9-7-20-7-9-7 Differential Pair Geometry





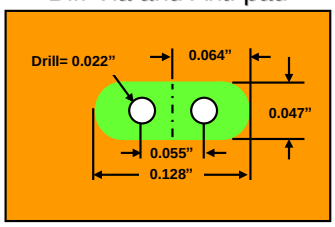


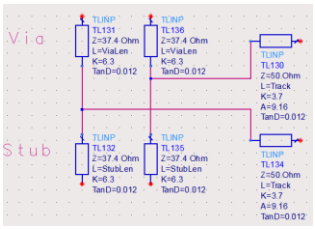
PCB Stack-up and Counter-bore Details

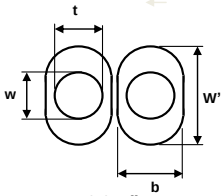


Tin-man Backplane Via Impedance and Model

Diff Via and Anti-pad







s = 0.055”
b = 0.064”
W’ = 0.047”
r = ½(0.022”)
w = 0.022”
t = 0.022”
Dk_{avg} = 3.74

$$Zvia \cong \frac{60}{\sqrt{Dkavg}} \times \sqrt{\ln\left(\frac{s}{2r}+\sqrt{\left(\frac{s}{2r}\right)^2-1}\right)\times\ln\left(\frac{W'+b}{w+t}\right)}$$

$$\cong \frac{60}{\sqrt{3.74}} \times \sqrt{\ln\left(\frac{0.055}{0.022}+\sqrt{\left(\frac{0.055}{0.022}\right)^2-1}\right)\times\ln\left(\frac{0.047+0.064}{0.022+0.022}\right)}$$

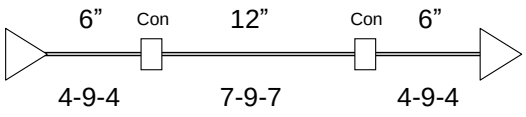
$$Zvia \cong 37.4\Omega$$

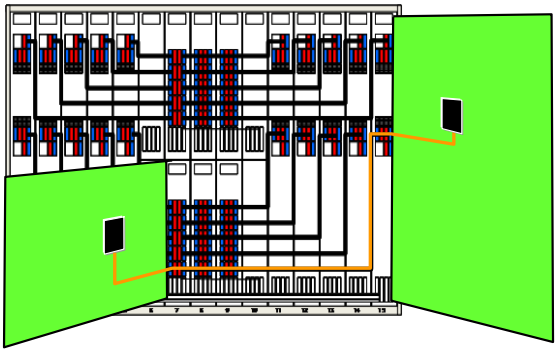
$$Dkeff \cong Dkavg \times \frac{\ln\left(\frac{s}{2r}+\sqrt{\left(\frac{s}{2r}\right)^2-1}\right)}{\ln\left(\frac{W'+b}{w+t}\right)}$$

$$\cong 3.74 \times \frac{\ln\left(\frac{0.055}{0.022}+\sqrt{\left(\frac{0.055}{0.022}\right)^2-1}\right)}{\ln\left(\frac{0.047+0.064}{0.022+0.022}\right)}$$

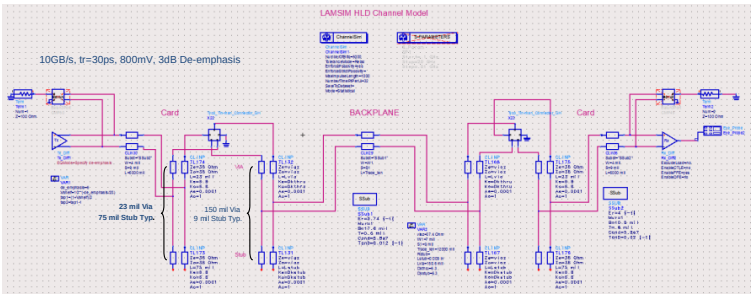
$$Dkeff \cong 6.33$$

Signal Integrity Ref Topology





Agilent ADS Channel Modeling and Simulation 10GBASEKR



Eye @ 10^{-16} BER

Height = 229mV

Width = 50 ps