Comparison of ROSE, C3/IC, and SIR as an effective cleanliness verification test for post soldered PCBA

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Abstract

Purpose – The purpose of this paper is to evaluate and compare the effectiveness and sensitivity of different cleanliness verification tests for post soldered printed circuit board assemblies (PCBAs) to provide an understanding of current industry practice for ionic contamination detection limits.

Design/methodology/approach – PCBAs were subjected to different flux residue cleaning dwell times and cleanliness levels were verified with resistivity of solvent extract, critical cleanliness control (C3) test, and ion chromatography analyses to provide results capable of differentiating different sensitivity levels for each test.

Findings – This study provides an understanding of current industry practice for ionic contamination detection using verification tests with different detection sensitivity levels. Some of the available cleanliness monitoring systems, particularly at critical areas of circuitry that are prone to product failure and residue entrapment, may have been overlooked.

Research limitations/implications – Only Sn/Pb, clean type flux residue was evaluated. Thus, the current study was not an all encompassing project that is representative of other chemistry-based flux residues.

Practical implications – The paper provides a reference that can be used to determine the most suitable and effective verification test for the detection of ionic contamination on PCBAs.

Originality/value – Flux residue-related problems have long existed in the industry. The findings presented in this paper give a basic understanding to PCBA manufacturers when they are trying to choose the most suitable and effective verification test for the detection of ionic contamination on their products. Hence, the negative impact of flux residue on the respective product's long-term reliability and performance can be minimized and monitored effectively.

Keywords Flux, Printed circuits, Electric charge, Contamination

Paper type Technical paper

Introduction

Increasing complexity of the printed circuit board assembly (PCBA) process has resulted in an increase in residue-related problems. The ambiguity of how clean is clean after an effective washing process has been an ongoing challenge in the industry for three decades (Tautscher, 1978). Recently, there has been a consistent increase in electrical shorts from dendrites induced by residue contamination that migrates during service, resulting in the failures of microelectronic circuitry. In response to increasing field failures attributable to dendrite growth, the microelectronics community has deployed more resources for the study of dendrite growth. Owing to the miniaturization of microelectronics, even dendrites of about 50 μm in length have become a reliability concern. It has been widely reported in the literature that, there are essentially four basic ingredients needed to grow dendrites and to subsequently cause electrical failures in the PCB circuitry and these are:

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Soldering & Surface Mount Technology
23/2 (2011) 85–90
© Emerald Group Publishing Limited [ISSN 0954-0911]
[DOI 10.1108/09540911111120159]

The authors would like to thank YY Yeap from Jabil Penang Plant 1 for her assistance in providing all of the IPC standard technical specification references, as well as Dr Mike Bixenmen of Kyzen Corporation who helped in reviewing and proof reading the manuscript. In addition, technical analysis was also supported in part by Jabil Penang's Plant 2 failure analysis laboratory.

Received: 24 May 2010
Revised: 14 October 2010
Accepted: 19 October 2010

1 electrical bias (as low as 1.5 V);
2 corrosive material;
3 moisture; and
4 time.

Dendrites grow on a PCBA by way of a plating process where a conductive and corrosive residue (flux) provides the current path between a cathode and an anode. Voltage travels along this new, unintentional current path and the dendrites begin to grow. Since the four basic ingredients required for dendritic growth are influenced by several environmental, design, material and process variables, no reliable mitigation strategies to combat this problem are available at present (Lee *et al.*, 2006; Southworth *et al.*, 2008; Konrad, 2009).

With the understanding that it only takes four basic ingredients for a dendrite to grow, the possibility of its migration can be minimized by eliminating one or more of the basic ingredients, as shown below:

1 Remove voltage from the PCBA, which is typically impossible.
2 Prevent the exposure of a PCBA to moisture and/or humidity. This can be accomplished by either controlling the PCBA's environment (not always possible) or by conformally coating the PCBA, which ironically requires a clean surface for proper adhesion.
3 Remove the conductive residue (flux).
4 Minimize the exposure time.

Basically, option three appears to be the easiest one to control and it has been commonly approached by most of the electronic assembly industries. This is evident from the growing number of assemblers cleaning their assemblies after reflow and wave to remove undesirable flux and other conductive residues picked up during board fabrication, from components, and during the assembly processes (Konrad, 2009).

As removing the conductive residues can slowdown dendrite growth, it is important to know whether or not the implemented wash process successfully eliminates such conductive residues. There are a number of cleanliness tests commonly used within the industry, but there is little consensus as to which test is the best for the quantification of printed wiring board contamination and its correlation to the respective long-term reliability performance of the products. Although most manufacturers refer to the IPC for industry standards and compliance, unfortunately, a generalized chart listing contamination levels for a specific flux and process does not exist (Weekes, 2001). It is the focus of this paper to review the various cleanliness test methods such as resistivity of solvent extract (ROSE), critical cleanliness control (C3), ion chromatography (IC) analysis, and surface insulation resistance (SIR). Our evaluation findings for PCB contamination using ROSE, C3, and IC analysis are presented. All the results were compared and detection limits for the different test methods are discussed.

Test method review – ROSE (Omegameter 600SMD)

The ROSE testing is accomplished using an Omegameter 600SMD. Prior to the ROSE test, the Omegameter is chemically calibrated to eliminate all possible measurement inaccuracy. The test samples are tested in accordance with IPC-TM-650, method 2.3.26.1 using a 10-min test time, a pin grid array area in 100 ml of solution, and a solution concentration ratio of isopropanol: deionized water (DI) = 75 percent: 25 percent (IPC-TM-650, n.d.; IPC J-STD-001D, 2005).

Cleanliness criteria documented in section 8.3.6.3 for ionic residues (manual method) in IPC J-STD-001D for assemblies soldered with ROL0 or ROL1 fluxes, state that surface contamination shall be less than 1.56 $\mu g/cm^2$ or 10.07 $\mu g/in^2$ NaCl equivalent ionic or ionizable flux residue. However, when another flux is used, contamination shall not exceed a limit to be established by the manufacturer or by the user. Even though it may have been supported by historical data, the latter pre-set specification is subjected to the manufacturer's process control limit variances.

Test method review – C3 test

Bauer (n.d) from Fine Point Inc. had commented extensively on the use of a C3 tester to determine the PCBA cleanliness based on the localized current leakage detected on its surface. The C3 test can be performed on the production floor to determine whether a residue located at a critical area is corrosive or benign and it gives an immediate response to PCBA cleanliness problems. This test has been designed to assess the process cleanliness in relation to the type and level of residues that are able to be brought into solution in critical areas, namely as pad-to-pad or hole-to-hole on a functioning assembly. The extraction process has been designed to achieve effective ionic residue removal using a heated solvent delivery system which consists of three stages:

1 Solution heating/delivery to the extraction site.
2 Soak and ionization time.
3 Aspiration of solution to a collection cell.

This extraction cycle will be repeated nine times to effectively remove the surface residues from an area of 0.1 in^2 that will generate approximately 2.0 ml of extraction solution to be used during the testing and, afterwards, for any desired additional elemental or ionic contents analysis.

Current leakage due to corrosive residues left on a PCBA is detected during electrical testing. Using a sacrificial Y-pattern electrode immersed in the extraction solution, a 10 V bias is applied to the electrode and an internal timer is started to measure the time it takes to achieve a leakage event. The C3 tester measures the change in leakage current across an electrode gap caused by the solubilized residues in the extraction solution. A current leakage occurrence is determined based on the threshold limit of 500 μA that has been set and established using a combination of SIR and IC data from Foresite's 12 years of research. The electrical measurement is determined by assessing the time it takes for the extraction solution and the 10 V biased electrode to reach a 500 μA event. The ionic contamination detection mechanism established is based on the theory that the more corrosive or conductive the residue, the faster it will achieve a current leakage and vice versa. Since corrosive or conductive residues will create short run times and benign or insulative residues will take longer and electrical test runs that are less than 60 s are identified as dirty samples.

Test method review – IC analysis

In the past 15 years, IC has increased in usefulness in detecting ionic contaminants in semiconductor-related solids, liquids, and gases. More stable column resins and better concentrator columns have enabled the detection of challenging matrices such as corrosive and oxidative chemicals, small parts, and gases at ppb level (Vanatta, 2001). A commonly used test method is carried out in accordance to the IPC-TM-650, section 2.3.28 description.

Typical residues that are of special interest to the electronic industry are primary anion residues: chloride (Cl^-), bromide (Br^-), and weak organic acids (WOA). These residues often originate from solder paste and wave flux activators, as well as from solvents and rosin. Whether or not these residues left on the assemblies are good or bad depends on their corrosiveness (Weekes, 2001; Munson, 2001).

A review of the literature shows that the acceptance limits prior to running an evaluation are 2.0 μg/in^2 for chloride and 3.0 μg/in^2 for bromide for a bare PCB and 5.0 μg/in^2 for chloride for a soldered assembly. It is recommended that the chloride content be kept below 2.5 μg/in^2 and the bromide content below 5.5 μg/in^2 for no-clean bare PCBs. As for the washed units, most of the manufacturers are quite comfortable with chloride and bromide levels to be below 8.0 and 15.0 μg/in^2, respectively. In addition, for bare boards fabricated with a cold plating process, such as silver or palladium, it is recommended that bromide levels are under 10.0 μg/in^2, where the level of bromide is attributed to the fire retardant material in the laminate and solder mask. As a completely complexed (chemically) material, the bromine is not detrimental and poses little electrochemical risk to assemblies. The relatively low level of bromide indicates that the fabricator did not use a brominated hot air solder leveling flux. Similarly, WOAs such as adipic or succinic acid, which serve as activator compounds in many no-clean fluxes, are considered benign and are therefore not a threat to the long-term product reliability, as long as the deposition density (micrograms per unit area) of these acids does not exceed certain threshold levels. Fully reacted WOAs can act as insulators and thus, even at levels as low as 10.0 μg/in^2, they can potentially create a high contact resistance on devices such as switches (Munson, 2001; Pham, 2007).

Test method review – SIR test

The SIR test is used to determine the impact of solder fluxes and flux residues on the reliability of electronic assemblies by measuring the resistance between two surface conductors in response to an electrical bias in a humid environment. The SIR test that is commonly applied has a data acquisition system that uses a nominal 1 MΩ resistor (1x10^6) in each of its circuit pathways. These current-limiting resistors serve three primary purposes (Weekes, 2001):

1. to preserve dendrite formations that grow during the test;
2. to protect the data acquisition system from large currents; and
3. to prevent a short circuit on one pattern from "robbing" the current from the remainder of the board.

The SIR test is performed in a high-temperature and high-humidity environment, as outlined in IPC J-STD-004B (2008). The IPC J-STD-004B methodology specifies that SIR testing is performed in accordance to IPC-TM-650, section 2.6.3.3, at 85°C/85 percent RH, with an applied polarizing bias of 45-50 V DC and a reversed bias of 100 V DC test voltage. This is conducted as a seven-day test (168 h) in which a "pass" will require SIR values of $10^8\,\Omega$ from day 4 (96 h) onwards. The electrical bias applied during the SIR test allows for the testing of electrochemical migration, where ionic species can migrate under the influence of the electric field. In addition, the high humidity (85 percent RH) at which the test is carried out also provides a sufficiently conducting path for the metal ions to migrate to the cathode, hence, forming dendrites. It is due to the accelerated stress environment that SIR test samples have to complete and, as such, it is well accepted by all of the industry's assemblers as an industry standard for product reliability compliance.

Experimental

Tests were carried out on actual production boards with dimensions of 11 in.x14 in. and components with different standoff heights. Each board was populated to its maximum component density (4,236 components for bottom side and 1,198 components for top side). Cleanliness tests "design of experiments" were conducted in three different wash machines and with three different conveyor speed settings (1.0, 0.3, and 0.1 m/min), while the other cleaning parameters remained the same. The wash machine conveyor belt speed was purposely adjusted to produce different PCBA cleanliness levels for the ROSE, C3 test and IC analysis evaluation studies. Since ROSE and C3 instruments were readily available on-site, an evaluation study was done in detail applying both available tests.

To verify the cleaning process effectiveness, the extracted solution for the evaluation run using the 0.1 m/min conveyor belt speed wash process was selected for testing, as well as the IC analysis, at a certified external laboratory. SIR testing was not performed for the discussion in this presented paper, due to its unavailability at the time of cleaning process evaluation. Listed in Table I is the actual temperature and pressure achieved with a tolerance of ± 1°C for temperature and ± 2 psi for pressure. Incoming DI water temperature was controlled at 55°C and 9.09 MΩ water resistivity.

Results and discussion

Upon completion of each wash process with different conveyor belt speeds for different experiments, prying inspection was performed at two specific quad flat pack no-lead (QFN) component locations, namely CRD U118 and U121. It can be clearly seen from Figure 1(a) that flux residue was found below the QFN component at CRD U118 when it was pried off. This result clearly shows that the wash process at 1.0 m/min is ineffective at removing all the flux residues. At the same time, Figure 1(b) and (c) do not show any visible flux residue entrapped underneath the QFN component, an indication that the wash process run at 0.3 and 0.1 m/min, respectively, successfully removed all the undesirable flux residue at the same location. Similarly, when visual inspection was performed at CRD U121 (QFN with the same part number as U118 mounted at a different location on the same PCB), flux residues were found underneath the component as shown in Figure 2(a) and (b) for the PCBA wash at conveyor belt speed of 1.0 and 0.3 m/min, respectively. However, Figure 2(c) shows that wash process at a conveyor belt speed of 0.1 m/min was still effective in removing the undesirable flux residue at CRD U121.

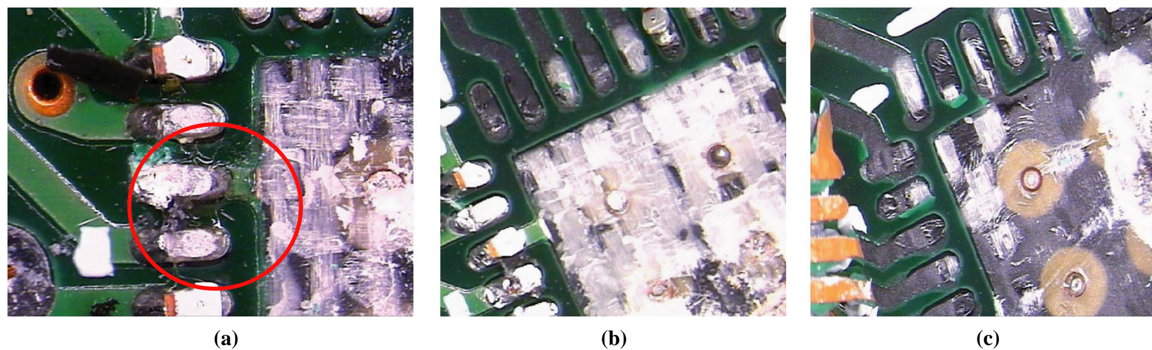
Table II shows the ROSE and C3 test results for different wash processes with conveyor belt speeds of 1.0, 0.3, and 0.1 m/min, respectively. All the evaluated boards passed the ROSE test successfully. In fact, when the obtained ROSE test result at $< 1.0\,\mu$g NaCl/in^2 was compared to the IPC J-STD-001D defined criteria at $< 1.56\,\mu$g NaCl/cm^2 (or equivalent to $< 10.07\,\mu$g NaCl/in^2) and Jabil Penang Site's defined value of $< 7.0\,\mu$g NaCl/in^2, evaluated samples passed the ROSE

Table I Parameter setting for wash machine

	Upper and lower pre-wash	Wash	Rinse zone	Final rinse zone	Dryer A	Dryer B
Temperature, °C	55	55	55	50	120	120
Pressure, psi	60	60	60	40	N/A	N/A

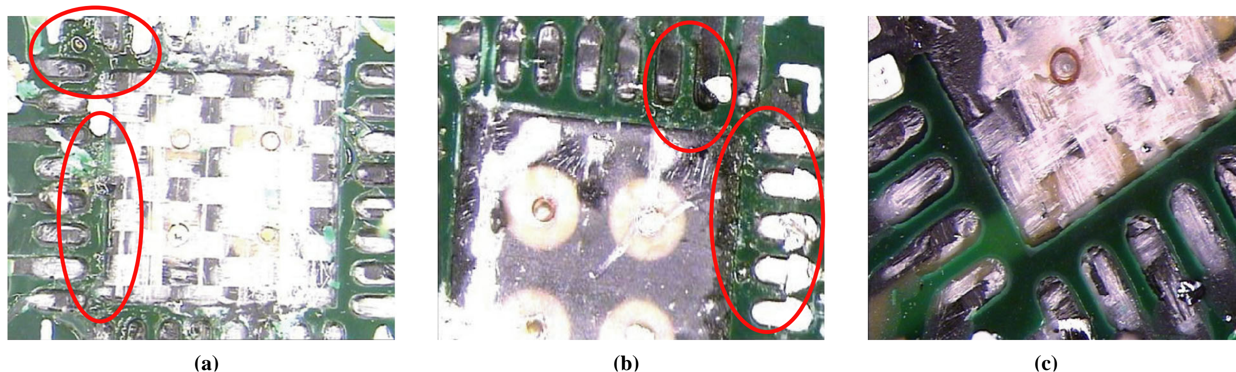
Note: N/A – not applicable

Figure 1 QFN component at CRD U118, completed wash process at respective conveyor belt speed of (a) 1.0 m/min, (b) 0.3 m/min, and (c) 0.1 m/min



(a) (b) (c)

Figure 2 QFN component at CRD U121, completed wash process at respective conveyor belt speed of (a) 1.0 m/min, (b) 0.3 m/min, and (c) 0.1 m/min



(a) (b) (c)

Table II ROSE and C3 test results for different conveyor belt speed wash process

DOE (belt speed) (m/min)	Omega meter (ROSE) test (μg NaCl/in^2)	Extended C3 test (μA within 180 s) U118	U121
1.0	0.4	93.5	*500.0* (failed)
0.3	0.8	415.5	*501.0* (failed)
0.1	0.6	116.5	160.0

Notes: IPC J-STD-001D specification for Omega meter test: <10.07 μg NaCl/in^2; industry recommendation specification for C3 test: <500 μA within 60 s (Bauer (n.d.))

test with a huge buffer tolerance. Contrarily, the QFN at CRD U121 did not pass the C3 test as expected for samples washed with conveyor speeds at 1.0 and 0.3 m/min, respectively. The initial sample lasted only 8.3 s, while the latter lasted 40.4 s before the detected current leakage had reached or surpassed the pre-set 500 μA event.

One possible explanation for both the test discrepancies is that these two tests provide two totally different types of results in different units of measurement and hence it is very difficult to compare the results of these two techniques. The ROSE test only measures the solvent's ability to conduct electricity, which can be related to the total amount of ionic material present in a huge reservoir of solvent solution containing alcohol and water. The solvent solution was obtained when the whole piece of PCBA was soaked in it for a finite period of time during the ROSE test. The test measures only the average value of resistivity of the ionic contaminants extracted from the entire PCBA area. Thus, this method only provides a process indicator, gives no insight into what contaminants are present and whether or not they are actually harmful to product functionality and long-term reliability (Munson, 2006). As for the C3 test, it is designed to analyze a 0.1 in^2 area of circuitry by providing a localized cleanliness reading. The system measures the localized current leakage across the electrode generated by the pure water in addition to the residues extracted from the board surface during the "cleaning" or extraction cycle. This test measures the time required to achieve 500 mA leakage current across the anode

and cathode separated by a finite distance. The criteria for a "pass" is based on an arbitrary time of 1 min, set by Foresite, the designer of the C3 system.

It is evident from the above discussion that ROSE provides a general measurement from the entire PCB while C3 gives results from the contaminants extracted from a very small localized spot. When the C3 test was performed on a QFN component at CRD U118 and U121, it was actually a localized cleanliness test. Hence, the C3 test is expected to give better detection sensitivity as compared to the ROSE test at a particular location having a cleanliness problem.

The Table III IC result reveals that, for both the samples that had passed the C3 test, they passed the IC requirement as well, except for sodium ionic content, which was higher than the recommended limit from Foresite. As there is no specific criteria mentioned under the IPC requirement with regard to specific ionic contaminant levels that are permissible on the surface of a cleaned assembly, IPC J-STD-001D defined criteria at $< 1.56\,\mu g$ NaCl/cm^2 (or equivalent to $< 10.07\,\mu g$ NaCl/in^2) for ionic or ionizable flux residue on a cleaned assembly was referred to as a guideline for discussion.

The obtained IC result was in good agreement with the C3 test result. Since all other ionic contaminants were detected at trace levels, except for sodium, minor current leakage as detected in the C3 test is reasonable and it may be partially contributed to by the detected ionic contaminants which are considered a corrosive material that can induce an undesirable current path. The well-correlated C3 test and IC result have shown that a 0.1 m/min conveyor belt speed wash process is effective in cleaning the flux residue under both U118 and U121 QFN components. The ionic contaminants detected in the IC analysis were insignificant to cause a possible electrochemical migration incident.

In view of the fact that the miniaturization of microelectronics and that, respectively, lower component standoff heights will be an inevitable trend in the industry, the ROSE test alone may not be sufficient to detect any possible contaminants that are present in a small volume at a specific location for a sensitive electronic circuit designed with smaller and more complex advanced components. Even though the C3 test provides a good localized measure of the conductivity of ionic contaminants, it should be complemented with techniques such as IC to determine the nature of the ionic contaminants and SIR to determine the propensity for electrical insulation failures from the ionic residues.

Conclusions

It is well documented and accepted that the current industry practices for ionic contamination detection are basically based on ROSE, modified ROSE, and IC analysis with standard extraction techniques. With the consideration that IC analytical equipment may not be readily available on-site for most of the electronic industry manufacturers, ROSE and modified ROSE will often be the only option available as a cleanliness verification test. As electronic circuit sensitivity continues to increase with smaller and more complex component designs, the potential for field failures attributed to ionic contaminants will increase concurrently. With the awareness that there is great risk for flux residues to be entrapped below low standoff components, the most commonly applied industry recognized methods for ionic cleanliness verification may have overlooked the contaminants that are present in small volume when considering the entire board. These contaminants may actually be localized at a sensitive area of circuitry, where they can react with moisture and applied voltage to create a system failure (Munson, 2005).

Based on the data presented, it is obvious that localized entrapped flux residues can create big problems for microelectronic assemblers, especially for assemblies that required high level of cleanliness. Knowing the fact that it is becoming more difficult to clean water soluble fluxes under lead-free conditions, while at the same time it is nearly impossible to clean no-clean assemblies under lead-free processing conditions, it will be proactive to selectively couple the C3 test with the ROSE test on the production floor to ensure that cleanliness monitoring, particularly at critical areas of circuitry that are prone to product failures and residue entrapment are not overlooked.

Table III IC analytical results for CRD U118 and U121 with a 0.1 m/min conveyor belt speed wash process

	U118	U121	Foresite recommended value[a]
***Anions*, μg/in^2**			
Fluoride, F^-	0.119	0.741	N/A
Chloride, Cl^-	0.255	0.833	6.0
Nitrite, NO_2^-	0.019	0.081	3.0
Bromide, Br^-	0.104	0.038	12.0
Nitrate, NO_3^-	0.181	0.599	3.0
Phosphate, PO_4^{3-}	N/D	N/D	3.0
Sulphate, SO_4^{2-}	0.669	0.948	3.0
***Cations*, μg/in^2**			
Lithium, Li +	N/D	0.004	3.0
Sodium, Na +	3.590	5.441	3.0
Ammonium, NH_4^+	0.056	0.132	3.0
Potassium, K +	0.029	0.200	3.0
Magnesium, Mg2 +	N/D	N/D	N/A
Calcium, Ca2 +	0.180	0.349	N/A
Weak organic acids, WOA	N/A	N/A	25.0
Total	$\geq$5.273	$\geq$9.407	N/A

Notes: [a]Foresite recommended ionic level, available online at: www.es-technology.cn/test.asp?ClassID =13&ID =15; N/A – not available and N/D – Not detected

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Kong Hui Lee received his Doctoral Degree in Material Chemistry from University Putra Malaysia (UPM) in 2007 with research project involving the use of advanced material (semiconductor) for wastewater treatment. Kong Hui Lee has authored and published several scientific articles, and has on-going collaboration research work with UPM Chemistry Department. He is a Chartered Chemist with Malaysia Institute of Chemistry and an affiliate member of International Unit of Pure and Applied Chemistry and Surface Mount Technology Association. Currently, he is a Principal Reliability and FA Engineer in Jabil Circuit's CISCO Business Unit Development global team responsible for CISCO Business Unit's site-to-site failure analysis and process defects trouble shooting. Kong Hui Lee is the corresponding author and can be contacted at: konghui_lee@jabil.com

Rob Jukna had served in the EMS industry for 20 years. He started his career in Research & Development of new RF products with Sparton in London and Ontario, Canada before he moved into Test Engineering within the company and responsible for company-wide test equipment design and programming. Rob Jukna moved to Jabil Florida in 1997, since when has taken care of Jabil's sites various Test and Quality Engineering functions. Five years later, he was assigned to lead Jabil's expansion in Test Technology Research & Development by adding inspection to the list of tests that should be used for product defects coverage. At the same time, he also researched on the correlation between the inspection equipments error and the manufacturing equipments operation. Currently, Rob Jukna is a Senior Manager of Applied Technology responsible for a large business unit within Jabil. His main focus is on various test and inspection processes that help to reduce cost and increase product quality.

Jim Altpeter began his career in 1977-1993 at Ford Motor Company Electronics Divisions as a staff Manufacturing Engineer and Technical Specialist. Jim Altpeter has authored and presented technical papers on inert gas soldering to IEEE, EPA and Industry Cooperative Ozone Layer Protection in which he received the Henry Ford Technology Award for the elimination of Freon cleaning of circuit assemblies via the development of no-clean soldering within an inert gas environment. Additionally, a US Patent No. 4,942,997 was awarded for the successful design and development of a solder flow well process for reflowing multi-pin components to and from printed circuit assemblies. Since joining Jabil Circuit in 1996, Jim Altpeter has held several positions within the USA including Manufacturing Engineering Manager, Technical Program Manager, and Business Unit Manager. Currently, Jim Altpeter is the Manufacturing Engineering Manager responsible for Jabil Circuit in Shanghai, China.

Kantesh Doss is a well-recognized expert in the industry, with extensive experience in optimizing lead-free assembly processes, no clean assembly processes and materials, cleaning technology and materials, reliability testing (60/85, 85/85, HALT, HASS, thermal cycling, drop, and thermal shock), and reliability prediction modeling. Kantesh Doss received his PhD in Materials Science and Engineering from State University of New York at Stony Brook with emphasis on Electrochemistry and Corrosion. The topic of his PhD dissertation was "A new model for the passivity of stainless steels". Dr Kantesh Doss holds a US Patent on laser assisted wet etching of copper conductors. Dr Kantesh Doss has authored several technical papers and chaired technical sessions in international conferences and has also chaired key IPC standardization committee meetings. Dr Kantesh Doss, as the Senior Global Failure Analyst is currently responsible for Failure Analysis Operations at Jabil Circuit in St Petersburg, Florida.

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