

Developments in Electroless Copper Processes to Improve Performance in amSAP Mobile Applications

Stefanie Bremmert, Laurence Gregoriades, Kay Wurdinger,
Thomas Vágó, Tobias Bernhard, Frank Bruning, Roger Massey
Atotech GmbH, Berlin

Abstract

With the adoption of Wafer Level Packages (WLP) in the latest generation mobile handsets, the Printed Circuit Board (PCB) industry has also seen the initial steps of High Density Interconnect (HDI) products migrating away from the current subtractive processes towards a more technically adept technique, based on an advanced modified Semi Additive Process (amSAP).

This pattern plate process enables line and space features in the region of 20um to be produced, in combination with fully filled, laser formed microvias. However, in order to achieve these process demands, a step change in the performance of the chemical processes used for metallization of the microvia is essential.

In the electroless Copper process, the critical activator step often risks cross contamination by the preceding chemistries. Such events can lead to uncontrolled buildup of Palladium rich residues on the panel surface, which can subsequently inhibit etching and lead to short circuits between the final traces.

In addition, with more demands being placed on the microvia, the need for a high uniformity Copper layer has become paramount, unfortunately, as microvia shape is often far from ideal, the deposition or “throw” characteristics of the Copper bath itself are also of critical importance.

This “high throwing power” is influential elsewhere in the amSAP technique, as it leads to a thinner surface Copper layer, which aids the etching process and enables the ultra-fine features being demanded by today’s high end PCB applications.

This paper discusses the performance of an electroless Copper plating process that has been developed to satisfy the needs of challenging amSAP applications. Through the use of a radical prepip chemistry, the formation, build up and deposition of uncontrolled Pd residues arising from activator contamination has been virtually eradicated. With the adoption of a high throwing power Copper bath, sub 30um features are enabled and microvia coverage is shown to be greatly improved, even in complex via shapes which would otherwise suffer from uneven coverage and risk premature failure in service.

Through a mixture of development and production data, this paper aims to highlight the benefits and robust performance of the new electroless Copper process for amSAP applications

Background

Since the advent of TSMC’s Integrated Fan Out (InFo) package, we have seen the introduction of high density Fan Out Wafer Level Packaging (FO-WLP) into mobile devices. Utilized in recent product releases, this packaging technique has allowed for a combination of the Applications Processor with the Memory, in a stacked Package on Package (PoP) build. Whether all mobile phone suppliers will continue this trend remains to be seen, however, we can assume, that for high end mobile devices, this will result in an ongoing, and potentially large increase in the use of this or comparable direct chip attach devices onto the HDI boards of the future.

One of the major impacts from the increased use of direct chip attach is that for the latest generation of high end HDI boards, we see a reduction to $\leq 30 \mu\text{m}$ line and space (L/S), which, effectively excludes the use of subtractive patterning techniques which have been the mainstay of HDI production until now. Subsequently, the PCB industry has already taken the first steps of moving towards modified Semi Additive Processing (amSAP) and its advanced variant amSAP, in order to achieve this latest requirement (Table 1). As these techniques are commonly used with IC substrate production, the resulting HDI boards are becoming known as Substrate Like PCBs (SLP)

Table 1 – Comparison of Subtractive, MSAP and amSAP Process and Capability

	Subtractive	MSAP	amSAP
Cu clad thickness (um)	2 – 9	2 – 5	< 3
Electroless Cu thickness (um)	0.35 – 0.5	0.35 – 0.5	1
Flash Cu thickness (um)	2 – 5	1 – 3	---
Panel plating thickness (um)	15 – 20	---	---
Pattern plating required	No	Yes	Yes
Etch resist	Dry film or LER	---	---
Cu to be etched (μm)	17 – 29	4 – 10	< 3
Achievable L/S (um)	> 35	> 30	> 20

The MSAP technique has been adopted first as it meets the current need for 30um L/S , but as we can see from Table 2, this will very quickly be followed by the need to push L/S requirements further towards 20um, and this cannot be achieved without the adoption of amSAP.

Table 2 - Critical Factors within the HDI Roadmap

	2015	2016	2017	2018	2019	2020
μ Via Diameter (μm)	70		50		40	
μ Via Aspect Ratio	0.8			0.9	1.0	
μ Via Pad Diameter (μm)	200	140	140	130	120	100
Min L / S (μm)	35 / 35		25 / 25		20 / 20	
Cu Thickness (μm)	15	12	10			8
BGA Pitch (μm)	350	300		250	200	
Technology	Subtractive		MSAP/amSAP		amSAP	

While process chemistry readily exists for both MSAP and amSAP, there are a number of technical issues that require review in order to maximize the benefits available from both production techniques. This paper focuses on the issues associated with the electroless Copper deposition processes, and aims to show the advantages gained through the adoption of a revised and newly developed chemical process.

Technical Issues for Electroless Copper Processes

Palladium Residues and Etch Defects

Figure 1 shows a generic electroless Copper process, which typically consists of a “desmear” to remove excess resin after laser drill, a “pretreatment” step to clean and condition the Copper, resin and glass reinforcement, followed by the “activation and electroless Copper” deposition itself. As can be seen, after etching the inner layer Copper to ensure good adhesion, there is a predip followed by an Activation, or Catalyst step.

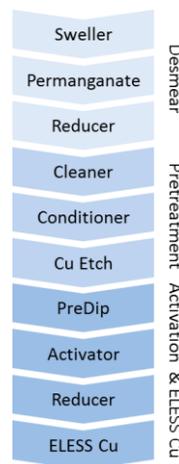


Figure 1. Generic Electroless Copper Process

This seemingly innocuous predip has a number of critical tasks, namely, to remove any residual Copper Oxides on the inner layers resulting from inadequate or poor etching, to ensure good coverage with the Palladium (Pd) based activator, as this will clearly impact the quality of the final Copper layer, and finally to act as a physical buffer to protect the activator solution from contamination, which may lead to unacceptable precipitation of the costly Pd catalyst.

However, even when utilizing horizontal process equipment which is understood to offer reduced solution drag in from previous process steps compared to traditional vertical tools, it is virtually impossible to eliminate contamination of the activator solution by the predip. As such it is essential that the predip chemistry be either, as chemically inert towards the activator solution as possible, and/or that the activator be sufficiently robust so as to remain unaffected by the possible levels of predip it will encounter.

As the L/S separation decreases, the Copper to be removed during the etch step also decreases, and while there has always been a tendency to “over etch” in order to accommodate plated Copper thickness variations and ensure a clean track to track separation, with tracks <20um in width there is more risk of unacceptable width reduction as well as undercut. This may seem irrelevant to the predip step, but as the predip can lead to Pd precipitation and uncontrolled deposits onto the PCB, and

with Pd acting as an etch inhibitor, there is a clear concern that a predip used successfully for subtractive manufacturing techniques is not suitable for one based on amSAP.

Figure 2, shows a short circuit resulting from Pd residues arising from contamination of the activator with predip, and in order to minimize the occurrence of such “Pd shorts” it is clear that a new predip-activator combination needs to be developed for amSAP applications where over etching cannot be tolerated

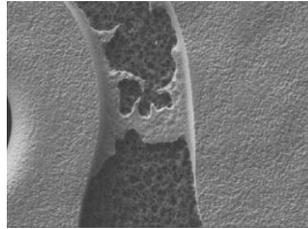


Figure 2 - Etch Short Resulting from Pd Residues in the Activator

Electroless Copper Process Improvements

As shown in Table 2, the PCB roadmap for mobile applications shows a general reduction in microvia diameter, which will also come with a reduction on surface Copper thickness in order to achieve the desired reduction in trace width.

For these to occur, there are 3 major developments needed within the Electroless Copper step itself.

Total Surface Copper Thickness Has to Decrease

Within most PCB processes, the gains achieved in line and space capability can be associated with reductions in the Copper thickness needing to be etched away after plating. We can see from Table 1 that for circuits constructed using amSAP, at approximately 25% of the total layer needing to be removed, the electroless Copper thickness is an important factor when looking to increase line and space capability.

Uniformity of the Deposited Copper Layer Has to Improve

As pointed out above, the thickness of the total Copper has a direct impact on the line and space capability of the process. With the electroless Copper typically providing 25% of the total thickness, any variations within that layer must be minimized as they can lead to etch distribution issues and ultimately Copper residues. While this can be compensated for through over etching, this is not desirable with reducing trace width, as it also risks the occurrence of heavy undercut which can lead to full track lift and open circuits. In view of this, it is essential that high end electroless Copper processes must offer tangible improvements in their deposit thickness distribution.

Increased Throwing Power

While it is clear that Electroless Copper has to become thinner and more uniform in order to improve etch capability, this must not be achieved at the cost of other critical parameters.

With microvias being the typical layer interconnects in HDI applications, it is essential that the reliability of these joints not be compromised, and simply reducing the deposited surface Copper thickness risks this. Throwing Power (TP) is an expression comparing the deposited surface Copper thickness, with that deposited at the bottom of a microvia, and ideally should be 100% as this represents the same thickness at both locations. Unfortunately, it is typical for most Copper processes to exhibit TP figures below this, meaning that the surface deposit is often 50-70% thicker than that at the base of the microvia. While this can be tolerated in subtractive processes, it must be improved for amSAP techniques, as the reduced electroless Copper in the microvias risks reliability issues due to poor coverage and subsequent weakness and faults within the electrolytic Copper. This is further compounded by the shape and quality of the microvia themselves. Figure 3 shows extremes of microvia shape that are “regularly” achieved in production environments, -while one image is an almost classical shape with smooth tapered sidewalls, the other is far from ideal and shows rough side walls, glass protrusion into the via and large wedges located at the base of the interconnect. In order to achieve reliable interconnects, next generation deposition processes must have sufficient, and improved throwing power in order to ensure that such microvias are fully and reliably covered with Copper.

While the above points are essential when considering electroless Copper processes for amSAP production, there are other factors that can be considered as beneficial.

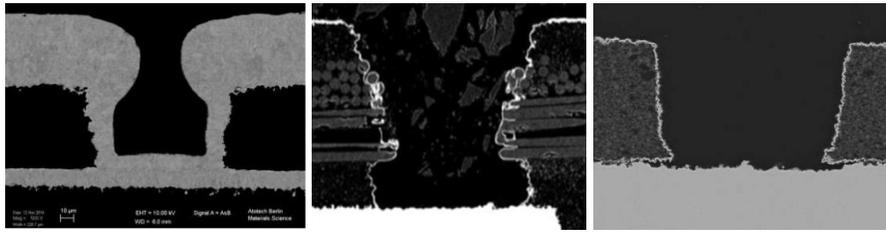


Figure 3 – Variation in Micro Via Shape

Dry Film Adhesion

With the adoption of SAP, or any of its modified variants, PCB producers move away from the traditional panel plate processes and into ones based on pattern plating. As such it is essential that the photoresist has sufficient adhesion to withstand the electrolytic plating process. While modern dry films inherently contain adhesion promoters, it is typical to apply some form of chemical treatment to roughen the Copper surface prior to dry film lamination in order to further increase photoresist adhesion. When using a panel plate process this is no issue as there is sufficient electrolytic Copper in both the microvias and any through holes to accommodate the mild etches these adhesion promoters usually require. However, for amSAP, the microvia is only coated with the electroless Copper layer, so any etching process risks removal of that electroless Copper, and while there are no-etching adhesion promoters available, etching processes are sometimes replaced with a simple acid rinse to remove oxides and clean the Copper surface prior to dry film lamination. As such, it is essential that any electroless Copper surface for SAP or amSAP must not only be able to tolerate exposure to mild acid cleaners, but must do so without any reduction in dry film adhesion

Nano voids

Voids have been a known concern within the electronics industry as a whole for many years, however, over recent years, there has been a slowly increasing awareness of what are now becoming termed as nano voids. Classed as a void <10nm in diameter, it is unclear if nano voids are a completely new phenomenon, or if they have always been present, and we now simply have better analytical tools that are able to detect them. But the fact remains, nano voids exist, and we should aim to understand them, identify if they are a real reliability concern, and if so reduce or ideally remove them from our PCBs.

Wherever there are interfaces between metals or even an alloy of metals, there is a potential risk for voiding to occur, Figure 4 shows a band of nano voids formed within an electroless Copper layer at the interface with the laminate Copper. Although there is growing awareness of nano voids, their detection and examination only started recently and their significance is therefore still poorly understood.

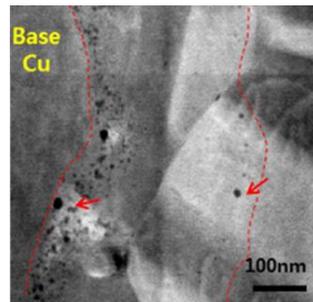


Figure 4 – Nanovoids

As highlighted previously, there are a number of process improvements required across the electroless Copper process as a whole, and following a targeted program, a new process has been developed that offers best compatibility with modern amSAP techniques.

Performance of New Processes

Pd Precipitation Arising from Predip Contamination

In order to minimize Pd particle build up within the process equipment as well as directly onto the PCB surface, it is essential to minimize the precipitation within the activator bath arising from contamination with the predip solution

In order to determine the impact on the precipitated particle count due to contamination of the activator with the predip, a solution was prepared in order to contain 100% of the predip concentrate within the activator solution. This solution contained 225ml activator concentrate, 150ml predip concentrate and sufficient water and NaOH as required to achieve the target pH and 1L of total solution volume. Samples were heated to normal operating conditions and then held for 6 weeks in

order to simulate production conditions. It should be noted that 100% drag in, ie 250ml predip dragged into 250ml of activator is far in excess of what would occur during normal operating conditions, and is used solely to accelerate and highlight any precipitation.

Prior to particle count and analysis, all sample solutions were stirred for 5 minutes, and then diluted to a ratio of 1:10 of their original concentration to avoid capillary blockages during measurements.

All samples were analyzed using a Beckman Coulter Multisizer 4 fitted with a 30um capillary suitable for measuring particles in the 0.6-18um diameter range and a 100um diameter to identify particles greater than 20um in diameter.

3 Sample solutions were prepared and measured

Activator contaminated with reference predip (Red in Figure 5)

Activator contaminated with newly developed predip (Green in Figure 5)

Activator contaminated with DI Water (Blue in Figure 5)

As can be seen from Figure 5, 6, and Table 3

All samples contained particles, with minimal numbers being greater than 10um in diameter and the majority of particles being smaller than 3um in size.

The activator solution contaminated with the newly developed predip solution contains substantially fewer particles than that using the reference predip.

There does not seem to be a solid relationship between the contaminating solution and the mean particle diameter, with all solutions exhibiting a mean particle size of approximately $2.9 \pm 0.2\mu\text{m}$ in diameter

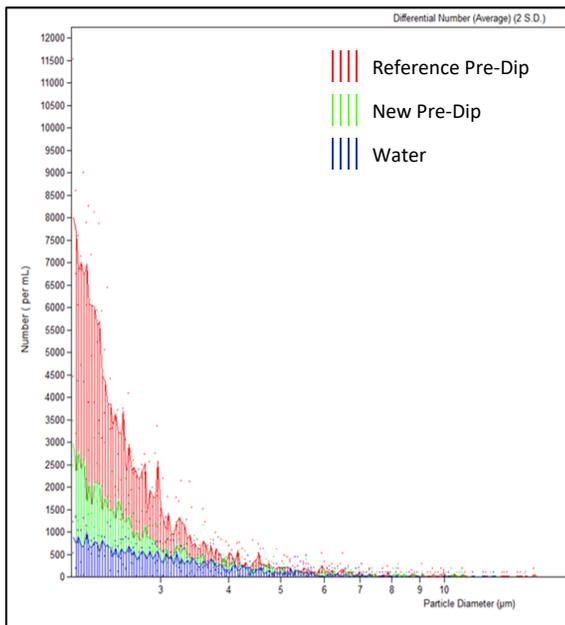


Figure 5 – Particle Count Charts for Contaminated Activator Solutions

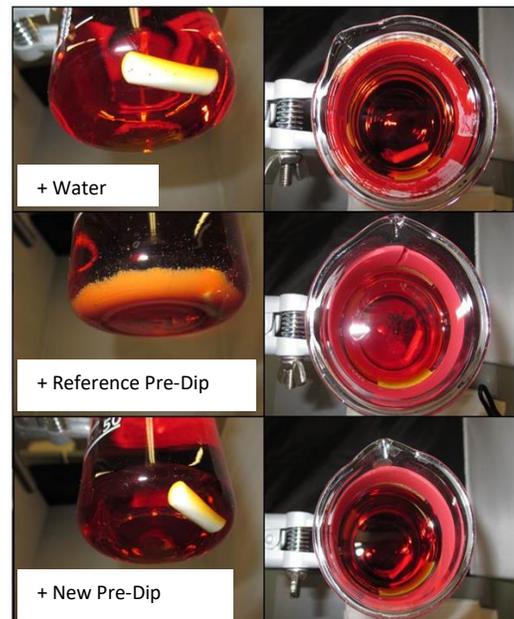


Figure 6 – Images of Test Solutions

Table 3 - Particle Count Data for Contaminated Activator Solutions

Activator contaminated with	Total Particle Count per ml Solution	Mean Particle Size (um)	Standard Deviation (um)
DI Water	34000	3.11	1.14
Reference Predip	168200	2.72	1.03
New Predip	68000	2.87	1.46

Changes in predip can impact the coverage of the resin and glass filler within a dielectric system. This can be readily checked using what industry terms a “backlight test”, in which a specific test coupon is electroless plated and cross sectioned, so as to allow areas of incomplete coverage to be detected as bright spots when viewed over a strong light source.

Backlight tests were performed using a number of dielectric systems, with both the reference predip and newly developed predip solution in combination with a market representative electroless Copper Solution.

From Figure 7, we can see that performance is comparable for both predip solutions across all dielectrics examined.

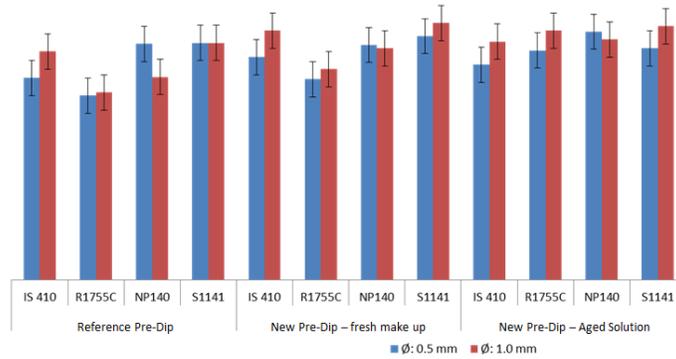


Figure 7 – Backlight Test Results Using Reference and New Predip Solutions

Finally, using data collected through production level testing, where only the predip solution was exchanged for the newly developed solution, we can confirm that the new predip, actively decreases the occurrence of Pd induced shorts/residue

Table 4 – Production Test Date for New Predip

	Reference Predip	New Predip	
Sample Size (units)	22008	14952	Test 1
Defects Detected	1202	383	
Defect Rate	5.46%	2.56%	
Sample Size (Production Lots)	1	1	Test 2
Defect Rate	8.50%	2.18%	
Pd Shorts/panel	1.5	0	Test 3
AOI Scan time (600pnl)	360 min	180 min	

Increased Throwing Power for Electroless Copper Solution

Throwing Power (TP) is an expression comparing the deposited surface Copper thickness, with that deposited at the bottom of a microvia, and ideally should be 100% or greater as this represents the same thickness at both locations. Historically, the locations for the measurements have been those represented by the red arrows in Figure 8, however, over recent years there has been a tendency to report values based on the marked with blue arrows as this as seen as more challenging and accounts for poor via shape with large wedges formed at the target pad. While it is open to discussion as to which method is better, more representative, or indeed even most relevant, it is acknowledged that methods do vary depending on application and in many cases the PCB producer. As such, this report uses data from both methods, with the “red” method being referred to as “Method 1” and the newer “blue” method as “Method 2”

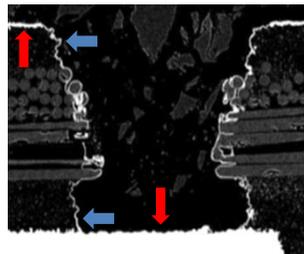


Figure 8 – Throwing Power Measurement Points

Using a variety of drilled microvias, which represent the wide variety of via qualities, we can see from Figures 9 and Table 5 that the newly developed electroless Copper bath offers consistent Copper deposition into the microvias, even where complex via shape exists, with improved throwing power compared to the reference Copper baths tested.

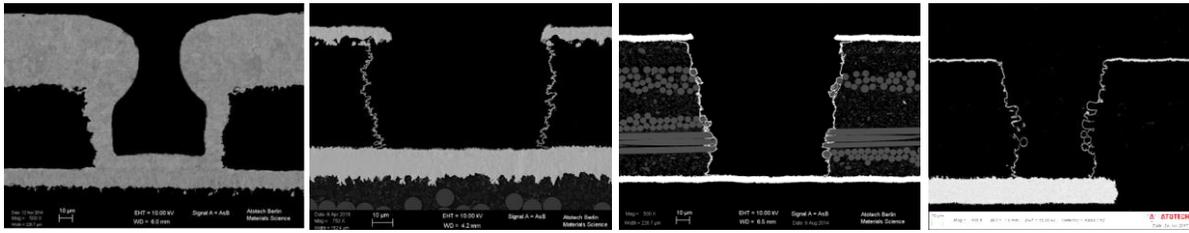


Figure 9 – Cross Sections of Micro Vias Plated Using New Copper Bath

Table 5 – Throwing Power Test Results

Test	Method	Via Dia x /Height (um)	Reference Copper Bath			New Copper Bath		
			Surface Cu (um)	BMV Cu (um)	TP (%)	Surface Cu (um)	BMV Cu (um)	TP (%)
1	1	100 x 60	0.45	0.15	33	0.43	0.32	75
2	2	100 x 65	0.30	0.08	28	0.37	0.27	73
			0.35	0.12	34			
3	2	75 x 65	0.18	0.08	45	0.17	0.13	76
4	2	110 x 100	0.38	0.20	53	0.32	0.24	75
5	2	100 x 85	0.82	0.38	46	0.37	0.34	91
			0.71	0.39	55	0.46	0.40	86

Surface Uniformity

Like most PCB processes, the amSAP technique relies on the ability to etch evenly through any surface Copper, so it is essential that any electroless layer deposited must be as even as possible with good thickness uniformity.

For both the reference and new Copper bath, uniformity of the deposit was measured on the both sides of panels processed through horizontal process tools. A total of 300 measurements were taken for each side of the measured panels.

As can be seen from Figure 10 and Table 6, the newly develop bath shows much improved thickness uniformity in the same process tool.

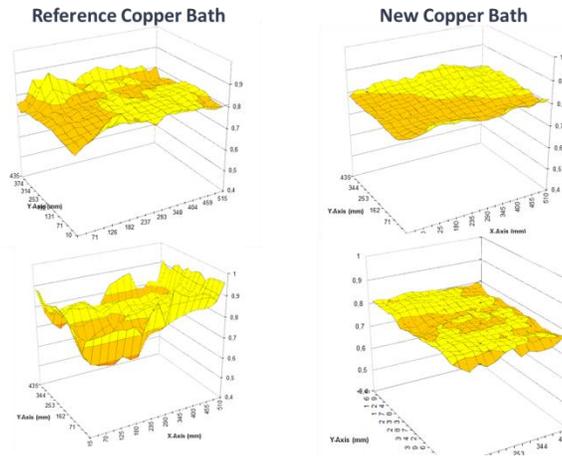


Figure 10 – Copper Thickness Distribution Maps for Reference and New Copper Bath

Table 6 - Measured Copper Thickness for Reference and New Copper Bath

	Reference Copper Bath		New Copper Bath	
	Top Side	Bottom Side	Top Side	Bottom Side
Mean Thickness (um)	0.8	0.80	0.80	0.80
Std Deviation (um)	0.02	0.07	0.02	0.01
Range (um)	0.18	0.32	0.08	0.07

Dry Film Adhesion

Figure 11 shows the amount of dry film features remaining on a test panel surface after developing when the surface has been coated with the reference and newly developed Copper baths. Panels were electroless Copper plated and spray cleaned with a solution of 10 % H₂SO₄. Hitachi RY-3000 series photo resist was dry laminated and the test pattern exposed and developed as per dry film recommendations. After developing the remaining dry film was evaluated using Ultra Violet Microscopy.

As can be seen from Figure 11, the newly developed Copper bath performs comparably with the existing amSAP Copper solution, and is compatible with minimal dry film pretreatment processing.

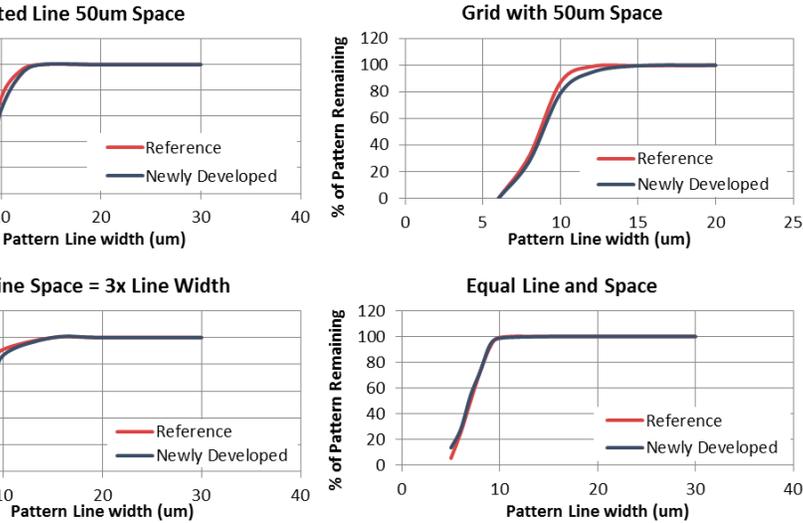


Figure 11 – Dry Film Adhesion Test Patterns and Results

Nano Voids

While there is limited reported understanding of nano voids, there are almost certainly a number of mechanisms which drive their initiation and development, with one likely being thermally induced nano voids that form during heat treatments applied after electrolytic plating. It had been initially considered that such nano voids develop as a result of stress changes occurring within the electroless and electrolytic Copper during heat treatments, however recent investigations have found that the formation of thermally induced nano voids appears to have little or no dependence on internal stress within the Copper layers, or the concentration of the co-deposited Nickel. As such, while the newly developed Copper bath has been optimized to have a controlled internal stress that is sufficient to achieve good adhesion and blistering performance; it is not anticipated to have significant impact in the level of thermally induced nano voids

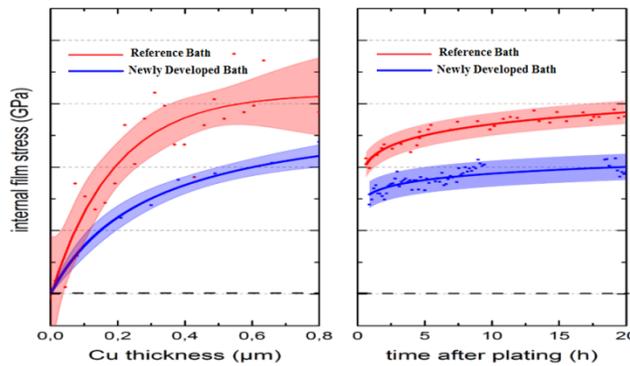


Figure 12 - Internal Stress Measurements for Reference and Newly Developed Bath

For thermally induced nano voids, a mechanism has been proposed where their formation is related to Pd-nanoclusters that form due to undesirable precipitation occurring in the earlier activator step. So it is offered that the new prep discussed previously, is a critical factor when reducing the occurrence of thermally induced nano voids.

Figure 13 shows a micrograph, as well as distribution maps of Ni and Pd taken across the base Cu - electroless Cu - plated Cu interface located at the target pad in a blind microvia. From the micrograph, it is clear that there are a number of concentrations of nano voids within the electroless Copper layer itself, with them being located predominantly around the interface with the base Copper. Two main observations arise as a result of the elemental mapping.

1 – There is a uniform distribution of the co-deposited Ni within the electroless Copper layer itself, with no direct relationship to the nano void location.

2 – There are isolated Pd rich nano clusters, which are coincidental with the location of nano voids

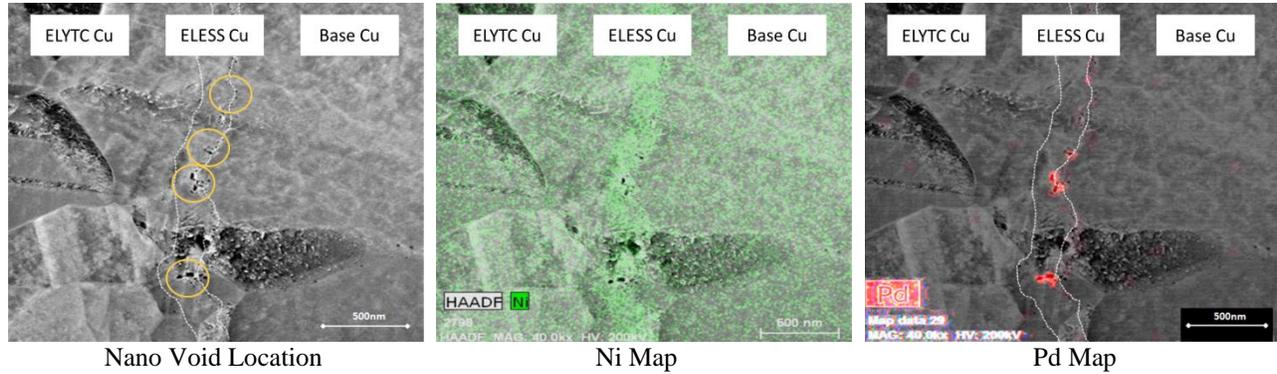


Figure 13 – Nano Void Investigations

Comparisons are made in Figure 14 for the occurrence of nano voids when using both the reference and newly developed predip in combination with the reference and newly developed Copper baths. As can be seen, in both cases, using the newly developed predip has resulted in a reduced occurrence of nano voids within the electroless Copper layer adjacent to the BMV target pad.

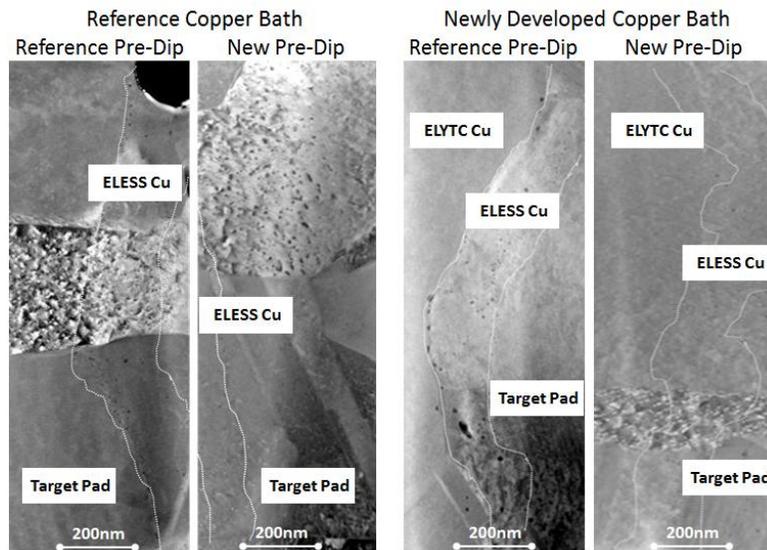


Figure 14 - Nano Void Investigations

Reliability

In order to alleviate initial reliability concerns it is essential that there are minimal defined interfaces between deposited layers of Copper when a “joint” is inspected. Typically this requires that there is a degree of epitaxy between any base or laminate, electroless and electrodeposited Copper. Epitaxy requires that the overlying, or epitaxial layer has a crystal structure and orientation that is similar to that underlying it, with little or no preferred orientation, and ideally there would be perfect epitaxy so that no distinct boundaries or defects can be determined.

Figure 15 shows Focused Ion Beam (FIB) micrographs of electroless and electrolytic Copper layers deposited using the reference and newly developer Copper bath. As can be seen, while there are instances where the 3 metal layers can be seen clearly with the reference electroless Copper, the newly developed Copper bath exhibits almost ideal epitaxy with both the underlying substrate and the overlying electrodeposited Copper

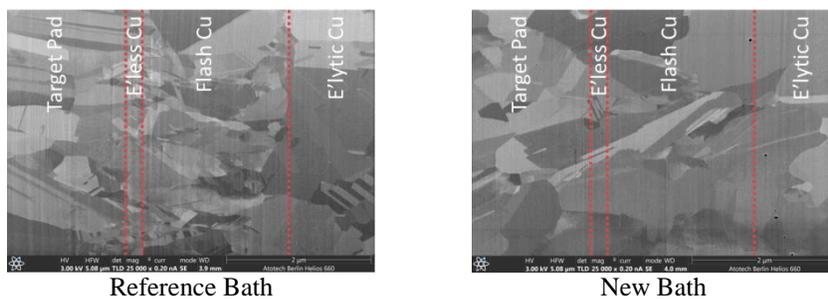


Figure 15 – FIB Showing Improved Epitaxy with Newly Developed Copper

Continuing to look at the reliability requirements typical to the PCB industry, it can be seen from Table 7 that the newly developed Copper bath is more than capable of passing such demands and is suitable for use in a wide range of electronic applications

Table 7 – Reliability Test Data for Newly Developed Copper Bath

Test Type	Method	Conditions	Test Criteria	Defect rate	Result
Solder Shock/Float	IPC TM 650.2.6.8	6 x 10 sec @ 288°C	No ICD during inspection	0	Pass
	Based on IPC TM 650.2.6.8	9 x 10 sec @ 326°C		0.55%	Pass
Cu-Cu Adhesion (BMV)	Internal Quick Via Pull	75, 100, 125, 150um Dia BMV	Target Pad Lift	0	Pass
Interconnect Stress Test	Based on IPC TM 650 2.6.26	2000 cycles 150°C/ T _R	Resistance Change <3%	Mean ΔR 0.9%	Pass
Thermal Cycling	Based on IPC TM 650 2.6.7	1000 cycles -40/+125°C (15/15min)	Resistance Change <3%	Mean ΔR < 0.295%	Pass

Summary

With the wider adoption of advanced IC packages, including Wafer Level Packaging, the demands being applied to Printed Circuit Boards continues to increase. Latest generation mobile handsets have adopted such packages and this has led to PCB designs beyond the capabilities of the existing subtractive HDI techniques. In order to meet these design criteria, high end HDI products have developed into what are being termed Substrate Like PCBs, which are manufactured using MSAP and/or amSAP techniques.

Due to the fine line requirements in combination with filled microvias, these techniques require a shift from panel plating techniques into those based around pattern plating. An integral part of any pattern plate process is the electroless Copper “seed” layer that is applied to the PCB prior to electrolytic plating. In this paper we have discussed the technical issues that arise when utilizing existing chemical processes for the electroless Copper deposition, and highlight the performance of newly developed solutions for future SLPs constructed using amSAP techniques.

Based on a novel prepip chemistry that actively reduces Pd precipitation and the occurrence of the resulting Pd shorts, in combination with a new electroless Copper bath that has been shown to enable improved microvia coverage with excellent surface uniformity, the new process solutions overcome the technical issues that exist and offer a reliable process suitable for current and future mobile device designs.