Drop impact reliability of edge-bonded lead-free chip scale packages

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A B S T R A C T

This paper presents the drop test reliability results for edge-bonded 0.5 mm pitch lead-free chip scale packages (CSPs) on a standard JEDEC drop reliability test board. The test boards were subjected to drop tests at several impact pulses, including a peak acceleration of 900 Gs with a pulse duration of 0.7 ms, a peak acceleration of 1500 Gs with a pulse duration of 0.5 ms, and a peak acceleration of 2900 Gs with a pulse duration of 0.3 ms. A high-speed dynamic resistance measurement system was used to monitor the failure of the solder joints. Two edge-bond materials used in this study were a UV-cured acrylic and a thermal-cured epoxy material. Tests were conducted on CSPs with edge-bond materials and CSPs without edge bonding. Statistics of the number of drops-to-failure for the 15 component locations on each test board are reported. The test results show that the drop test performance of edge-bonded CSPs is five to eight times better than the CSPs without edge bonding. Failure analysis was performed using dye-penetrant and scanning electron microscopy (SEM) methods. The most common failure mode observed is pad lift causing trace breakage. Solder crack and pad lift failure locations are characterized with the dye-penetrant method and optical microscopy.

1. Introduction

Mobile and handheld electronics devices such as digital cameras, cell phones, and personal digital assistants (PDAs) are prone to be dropped in their lifetime. The drop event may result in failure of solder joints inside these devices. Recently the European Union (EU) Restriction of Hazardous Substances (RoHS) and other countries' lead-free directives banned the use of lead in consumer electronics products. Thus, it is critical to understand and quantify the drop test reliability of lead-free solder joints.

There has been a significant amount of research done in the last few years on drop impact reliability [1–10]. The JEDEC standard JESD22-B111 [11] for the board level and related standards [12,13] for the subassembly level have been developed for drop testing handheld electronics. The fundamental mechanics of board level drop testing was studied by Wong et al. [14]. Several studies have been done to improve the reliability of lead-free solder joints by adding micro-alloying additives [15,16] or lowering Ag content [17].

Underfill materials were originally developed to improve the solder joint reliability of ball-grid array (BGA) and flip chip packages during temperature cycling. Recently studies have shown that underfill can improve drop test reliability as well [18,19]. However the application of underfills increases both the cost of production and assembly cycle times in manufacturing and must be considered against the drop test reliability improvements. To reduce the costs of underfill application, corner bonding and edge bonding processes have been developed. The reliability of corner-bonded CSPs has been investigated [20,21]. However, to the authors' knowledge, the drop impact reliability of edge-bonded CSPs has not yet been reported.

This paper presents the drop test reliability results for edge-bonded 0.5 mm pitch lead-free chip scale packages (CSPs) on a standard JEDEC drop reliability test board. Drop test reliability of CSPs with and without edge-bonded underfill are quantitatively compared. Failure analysis was performed using dye-penetrant and scanning electron microscopy (SEM) methods.

2. Test vehicle design and assembly

The test vehicle was designed according to the JEDEC standard [11]. Fifteen CSPs were soldered to the FR4 material test board with a dimension of 132 mm by 77 mm and a thickness of 1 mm. The 12 mm by 12 mm CSP component has a 0.5 mm pitch with 228 solder joints. The CSP component has internally daisy chained connections with an input and output trace located at one package corner as shown in Fig. 1. The boards have electroless nickel immersion gold (ENIG) surface finish on non-solder mask defined (NSMD) pads, while the components have electro-plated

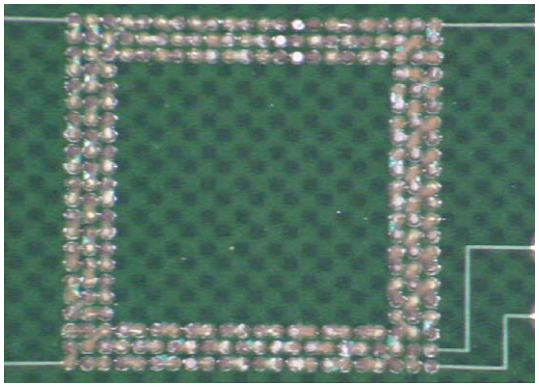

Fig. 1. CSP component and its I/O traces.

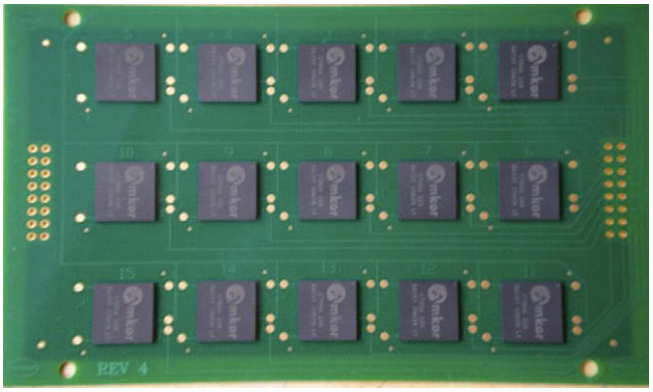

Fig. 2. Assembled test vehicle with components.

nickel–gold surface finish on solder mask defined (SMD) pads. The solder ball compositions in the CSP component are Sn3.0Ag0.5Cu (SAC305). The assembled test vehicle is shown in Fig. 2.

A SAC305 lead-free no-clean solder paste (Type 3) was stencil printed by a printing machine through a 100 μm (0.004 in.) thick electro-polished stencil with 300 μm (0.012 in.) square apertures. Solder paste height and volume were optically observed by a paste inspection machine to ensure high printing quality before the component was placed by a component placement machine. A reflow oven with nine heating zones and one cooling zone was used for solder reflow. The reflow oven processing was done in air using the reflow profile shown in Fig. 3.

Post-assembly cross-sectioning and SEM analysis showed good solder joints with some small voids as shown in Fig. 4. Visual and X-ray inspection show shiny, round and well collapsed solder joints with no bridging.

The test boards were divided into three cells; edge-bonded components with a thermal-cured epoxy, edge-bonded components with a UV-cured acrylic, and components with no edge-bonding. The edge-bond was applied on all four package corners by machine after solder reflow as shown in Fig. 5. The cured edge-bond had an average length of 3.81 mm (0.150 in.) along each side of the package with an average fillet leg length of 1.2 mm (0.039 in.), following the material manufacturer's recommended application for 12 mm CSPs. It should be pointed out that though both the edge-bonding process and the corner bonding process are two special cases of underfill applications, the edge-bonding process is different from the corner bonding process. In the corner bonding process, the adhesive is applied underneath the package corners *before* BGA or CSP packages are placed and reflowed. In the edge-bonding process, the adhesive is applied along the package edges *after* the BGA or CSP packages are placed and reflowed.

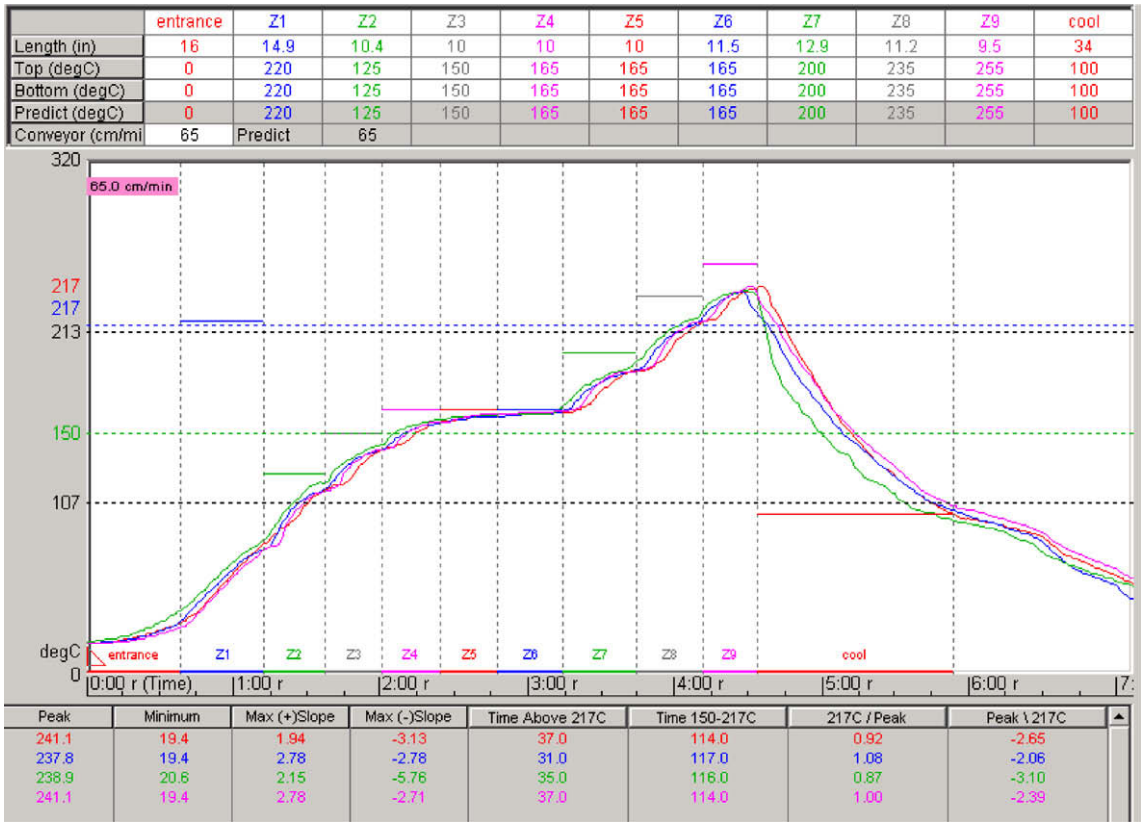

Fig. 3. Solder reflow profile.

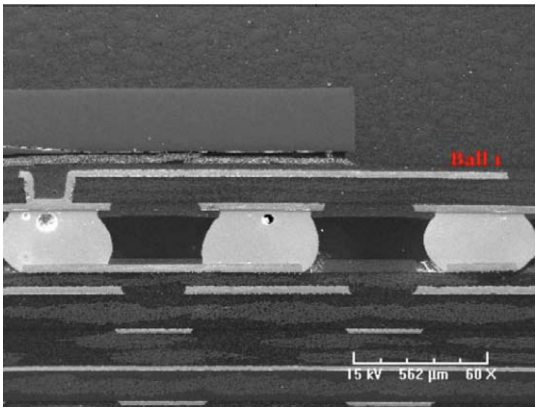

Fig. 4. SEM of solder joints after assembly.

Fig. 5. An edge-bonded CSP.

Note that the edge-bond epoxy/acrylic does not flow underneath the BGA, and does not cover the entire length of the edge but just the corners.

3. Drop test methodology

The drop tests were conducted using a Lansmont M23 TTSII shock test system, which applies a single half-sine shock impact pulse to the test vehicle for each drop. For this study the test vehicle board was mounted above the drop table in a horizontal position with the components facing downward which is the most severe orientation for board deflection [11,22]. The board was supported by four standoff poles with 8 mm diameter and 12 mm height located near the board corners.

Three impact pulses conditions were chosen from the JEDEC recommendations [12]: 900 Gs, 1500 Gs, and 2900 Gs, with 0.7 ms, 0.5 ms, and 0.3 ms durations, respectively. These acceleration profiles are equivalent to the JEDEC conditions F, B, and H. For each drop height and impact surface condition, the average result of two accelerometers was used as shown in Fig. 6. Both the acceleration peak and pulse duration were maintained within 10% of nominal for all tests. One deviation was made from the JEDEC standard in that the gap between the shoulder screw head and the board surface was controlled to within 100 µm rather than the specified 50 µm [11]. This was because washers with right thickness were unavailable during the experiment. The standard shoulder screws were not used because the standoff drill pattern had one corner off true axis by a very minor amount (it was leaning inward), but it caused enough spacing loss between the diameter of the board drill holes to the shoulder screw that we had binding on the board at rest. We eliminated that binding by using screws with smaller shoulders which widened that tolerance. A high-speed camera was used to observe the difference in deflection and behavior of our setup versus the tightly-constrained shoulder screws (binding screw to hole). We concluded that our setup is appropriate and expected that the deviation had insignificant effect on the results of drop test reliability.

The test vehicles were split into three groups as shown in Table 1. There are a total of seven no edge-bonded boards and eight edge-bonded boards. Among these seven no edge-bonded boards, three were assigned at 900 Gs, three at 1500 Gs, and one at 2900 Gs. Four edge-bonded boards with thermally cured epoxy were split into two boards at 1500 Gs and the other two at 2900 Gs. Four edge-bonded boards with UV-cured acrylic were split into two boards at 1500 Gs.

4. Failure detection system

A high-speed dynamic resistance measurement system was designed using a National Instruments (NI) analog-to-digital (A/D)

Table 1
Number of boards per drop test variable cell.

Edge-bonding (Gs)	No.	Thermal cured epoxy	UV-cured acrylic
900	3	0	0
1500	3	2	2
2900	1	2	2

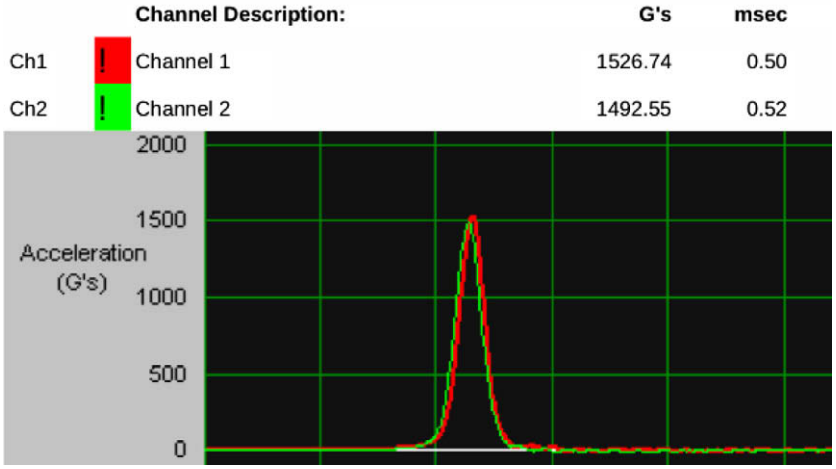

Fig. 6. Input acceleration pulse of 1500 Gs to 0.5 ms, JEDEC condition B.

converter, a desktop computer, and a voltage divider network to evaluate the resistance of the component daisy chain during the drop impact at a sampling frequency of 50 kHz with 16-bit accuracy. The sampling rate of the system provides 50 sample points per millisecond for each channel (50,000 samples per second), so that several samples are taken during the initial shock pulse (a minimum of 15 samples are captured during the 2900 Gs 0.3 ms pulse). The primary deflection time of the board and first harmonic vibration frequency in a 1500 Gs drop are near 4 ms and 240 Hz, respectively [23]; with a 50 kHz sampling frequency this system provides more than 200 samples during the first board deflection cycle. During each drop the test system records 1 s of data points from the fifteen components and saves the data for later analysis. A simple and proven method of achieving dynamic daisy-chain resistance measurement at near real-time was used [24]. The daisy chain is placed in a DC series circuit with a static resistor (R_s) of known value (in this case 100 Ω) to construct a voltage divider circuit as shown in Fig. 7. The measurement system records the voltage (V_c), divided across the component resistance and static resistance. The voltage (V_c) relates to the resistance of the daisy chained solder connections (R_c) by Eq. (1), where V_{DC} is the DC voltage source set to 5 V. As the component electrically fails, the resistance rises ($R_c \to \infty$) and the system registers a rise in voltage ($V_c \to V_{DC} = 5$ V).

$$R_C = \frac{V_c \cdot R_s}{V_{DC} - V_c} \tag{1}$$

A flexible multi-conductor shielded cable consisting of 25 wires with 20 American Wire Gauge (AWG) was used to connect the test vehicle. The outer diameter of the cable is 16.8 mm (0.66 in.). The 16 wires (15 channels and one common ground) connecting to the PCB were unbundled approximately 76 mm (3 in.) away from the board. The wires were soldered directly into the plated through-holes on the short side of the board. The cable wire bundle is secured to the drop tester base plate to prevent loading against the solder connections during impact. We did a study to investigate the effect of the cable on the peak acceleration of different locations on the board. The results showed that long-looped cable would reduce the acceleration peak of the impact on the board and change the symmetry of acceleration distribution on the board. The conclusions from this study were that any cable attached to a PWB in drop test conditions should be restrained without excessive hanging weight (not looped) and should be lightest possible but still be able to provide reliable through-hole solder joints.

The failure criterion used for the high-speed dynamic resistance measurement system is taken directly from the JESD22-B111 standard [11]: a 100 Ω resistance in the component daisy chain at any time during the drop impact or subsequent vibration is considered a failure, and the failure must be repeated in at least three out of five successive drops. Since a 100 Ω static resistor and 5 V DC supply voltage are used, the failure condition of 100 Ω is the equivalent of measuring 2.5 V on the component daisy chain. The electrical continuity of the cable-to-board through-hole solder joints is verified at regular intervals during and after drop testing to eliminate false positive failures due to broken cable connections. The initial resistance of the components and test vehicle traces combined were recorded before testing and were in the range 1.0–3.5 Ω. The component location and printed circuit board trace length on the test vehicle affects the initial resistance since all trace lengths are not identical.

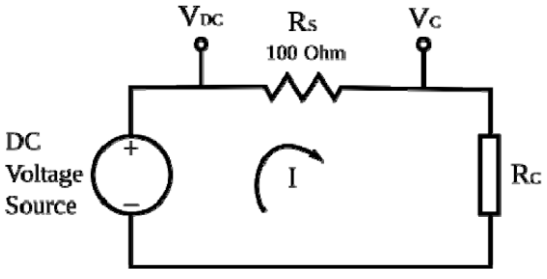

Fig. 7. DC series voltage divider circuit.

The dynamic resistance measurement system is able to detect intermittent failure which may have insignificant resistance change when the board is at rest but a significant change during board deflection. Fig. 8 shows an intermittent failure detected by the high-speed data acquisition system during the board deflection and vibrations; the 5 V peaks shown indicate high resistance discontinuities in the component daisy-chain.

5. Results and discussion

5.1. Reliability data

The number of drops-to-failure for each component location and test board without edge-bonding are shown in Table 2. In the table, each column represents one board except the first column. The first row is the input acceleration condition used for that board and the second row is the total number of drops the board was subjected to. As expected it is clear that higher G-levels typically result in lower number of drops-to-failure. Every component except C10 in a board without edge-bonding failed after 50 drops

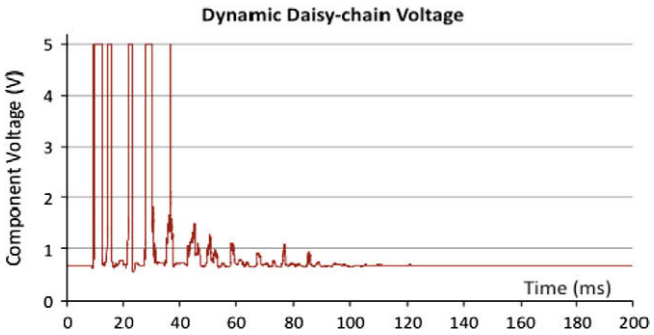

Fig. 8. Intermittent failure detected by the high-speed dynamic resistance measurement system, 10,000 data samples shown in a 0.2 s window.

Table 2
Drops-to-failure of components without edge-bond.

Accel (Gs)	900	900	900	1500	1500	1500	2900
Drops	75	75	100	70	40	60	50
Component							
C1				37	29		7
C2							25
C3	62				14	33	4
C4	26	26	34	26	6	23	4
C5							5
C6					21	35	3
C7					19		42
C8	28	44		50	3	13	7
C9					30		21
C10							
C11					5		11
C12	16	6	43	13	2	6	4
C13	15	11	40	9	1	5	2
C14					21	32	38
C15							50

when subjected to 2900 Gs. Most of the components without edge-bonding fell off the board after less than 20 drops.

The data also shows that the component location plays a significant role in the drop test reliability. The components in rows C4, C8, C12, and C13 tend to fail the earliest and most frequently. It should be pointed out that the number of drops-to-failure varies significantly between different boards for the same component location. That means that there is a large variation in the reliability of drop testing.

The drops-to-failure data for edge-bonded boards are reported in Table 3. The total number of drops for each board is listed in row 2, and the edge bonding material (either thermal-cured epoxy or UV-cured Acrylated Urethane) is listed in row 3. It is clear that edge-bonding improves the drop test reliability significantly by comparing the highlighted columns in Table 3 (2900 Gs) to the last column of Table 2 (also 2900 Gs). Eight components failed on a board without edge-bonding after 7 drops when subjected to 2900 Gs as shown in Table 2, while the first eight failures occurred for the four boards with edge-bonding after 36, 44, 100, and 133 drops, respectively, when subjected to 2900 Gs as shown in Table 3. That indicates that the four edge-bonded boards show a 5–8 times reliability improvement for an input acceleration of 2900 Gs over the none edge-bonded board. This result is a slightly increase in reliability improvement over that reported for corner bonding, a 3–4 times improvement [20,21].

5.2. Effect of component location on drop test reliability

The issue of component location has been shown in a number of studies to be critical; the stress and strain in solder joints, and their failure rate, is partially dependent on the component location on the board [25,26]. It has been reported that the maximum acceleration location occurs at the board center and is much higher than the input acceleration profile [25,27]. However, the maximum board strain occurs under components along the board edges and near the supports [26]. Therefore, it is necessary to analyze the reliability data in context of component location.

The components on the board are recommended by JEDEC to be divided into 6 groups (denoted A–F) that are expected to have similar failure rates due to the symmetry of their locations [11]. The JEDEC defined component group locations are shown in Fig. 9, and for this study the cable of the dynamic resistance measurement system is always soldered in through-holes at the board edge near component 6.

Cumulative failure plots for solder joints with edge-bond subjected to 1500 Gs with 0.5 ms duration impact and 2900 Gs with 0.3 ms duration impact are shown in Fig. 10 and 11, respectively. Reliability analysis was performed for each component location group based on the JEDEC board grouping (A–F). In this analysis, the reliability data of both edge-bonded materials were combined because it seems that there was no significant difference in the drop test reliability between the epoxy edge-bond and acrylic edge-bond. The results show that groups E and F failed at the fastest rate. Groups A–D have similar failure rates, with B showing the fastest failure rates of among those four component groups.

6. Failure analysis

Two failure analysis methods were used to investigate the failure locations and the failure modes: (1) dye-penetrant and (2) cross-sectioning Scanning Electron Microscopy (SEM). After analyzing 60 components on four boards that were dye penetrated, five failure modes have been identified: (1) pad cratering, (2) input/output (I/O) trace fracture, (3) solder cracking near the board side, (4) daisy chain trace fracture, and (5) solder cracking near the component side. Fig. 12 summarizes the percentage of each failure mode on the 60 components analyzed.

Pad cratering is the dominant failure mode for these test vehicles in drop impact; 83.3% of the components exhibited pad cratering. Pad cratering is defined as cracking in the thin resin rich region underneath the copper pads and traces as shown in Figs. 13–15. The resin crack has also been reported by Mattila et al. [28] and Chong et al. [29]. The pad cracking was commonly seen for boards with and without edge-bonding. Note that some components had multiple failure modes so that the total percentage shown in Fig. 12 is more than 100%.

The second most common failure observed was I/O trace/pad breakage. Fig. 16 shows a single CSP component pad location with all four corners where corner #2 has two traces running outward from the component. These two traces are the daisy-chain I/O connections. Traces connected to the other three corners lead to test pads and are not part of the daisy chain. The orientation of every package on the test vehicle is the same, with corners #1 and #2 parallel to the short board axis, corners #2 and #3 parallel to the long board axis, and the orientation of the trace layout is also the same for each. Due to resin crack under the copper pad, the transition of the trace to the I/O pad may be the weakest point, which may cause copper trace/pad cracking [30]. The frequency of this

Table 3
Drops-to-failure of components with edge-bonded.

Accel (Gs)	1500	1500	1500	1500	2900	2900	2900	2900
Drops	325	350	279	355	190	170	175	173
Edge-bond	Epoxy	Epoxy	Acrylic	Acrylic	Epoxy	Epoxy	Acrylic	Acrylic
Component								
C1						151	66	61
C2		342	276		133	127		119
C3	80	292	33	101	70	72	12	103
C4	236	255	257		63	16		100
C5						36	73	91
C6		55				44	37	60
C7						35	69	158
C8	201			85	113	20	84	83
C9				292		25	29	124
C10			277			12	59	
C11		193	178	103		65	38	
C12	66	76	52	162	53	24	23	16
C13	61	129	73	77	42	13	18	14
C14		232				42	44	120
C15	107		268		44	22	25	90

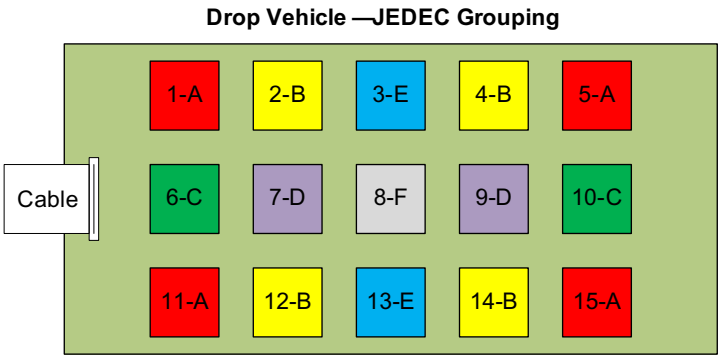

Fig. 9. Board component group locations.

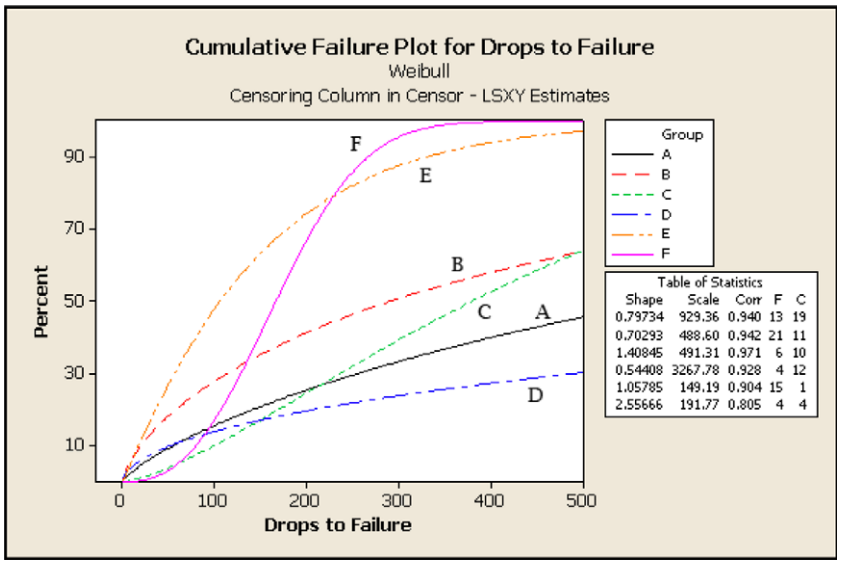

Fig. 10. Cumulative failure plot for drops-to-failure of each group at 1500 Gs with 0.5 ms duration.

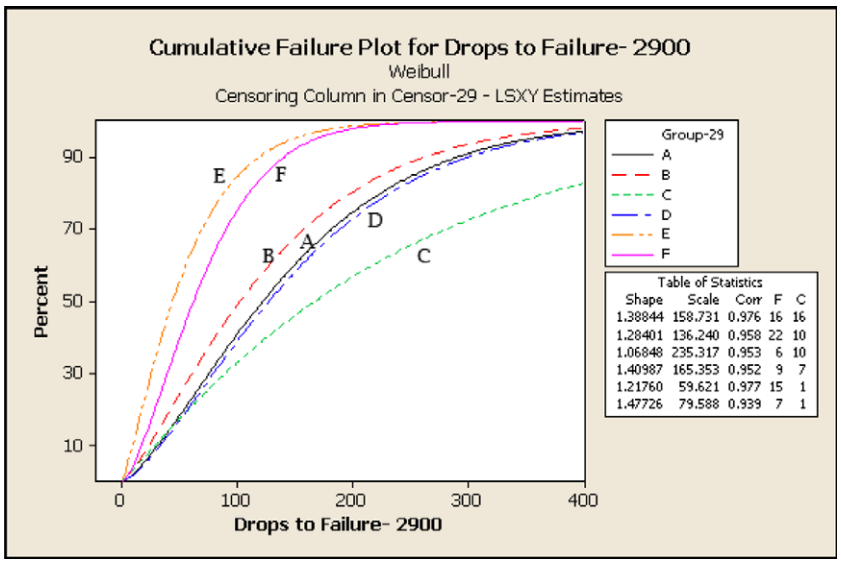

Fig. 11. Cumulative failure plot for drops-to-failure of each group at 2900 Gs with 0.3 ms duration.

failure indicates that if the corner solder joint pads were allowed to lift off the board while maintaining electrical continuity (the daisy chained trace between solder pads may lift up), then the drop impact reliability of the assembly might be overestimated. Similar

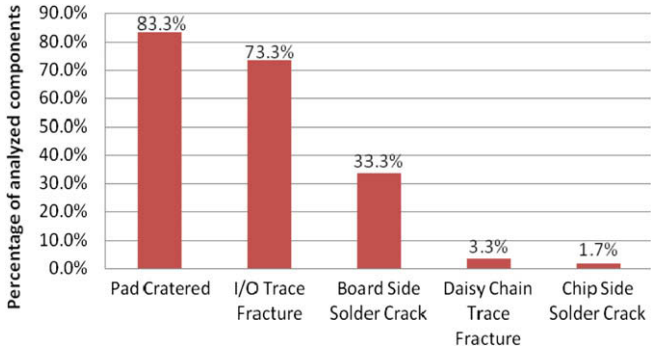

Fig. 12. Summary of observed failure modes

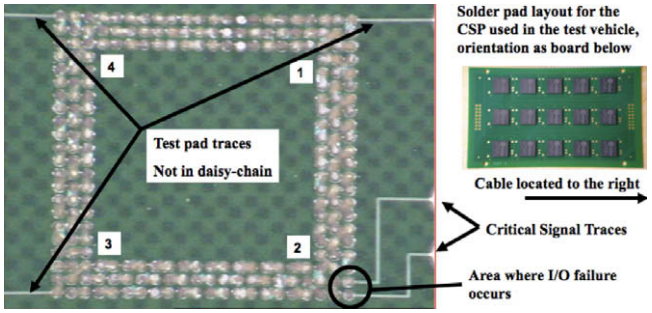

Fig. 16. CSP I/O traces and component orientation.

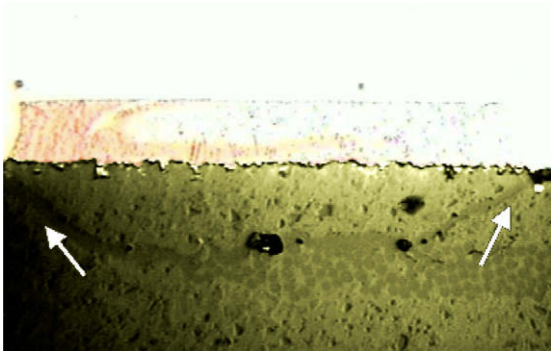

Fig. 13. Cracked resin under the board side pad (dark line), edge-bonded.

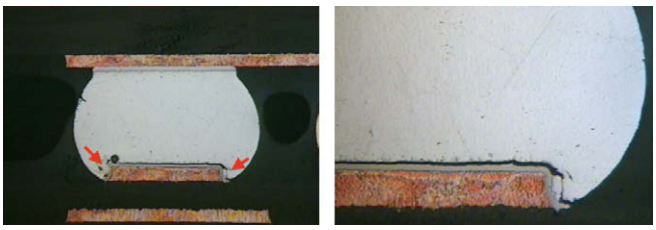

Fig. 17. Solder joint fracture near the board side IMC layer.

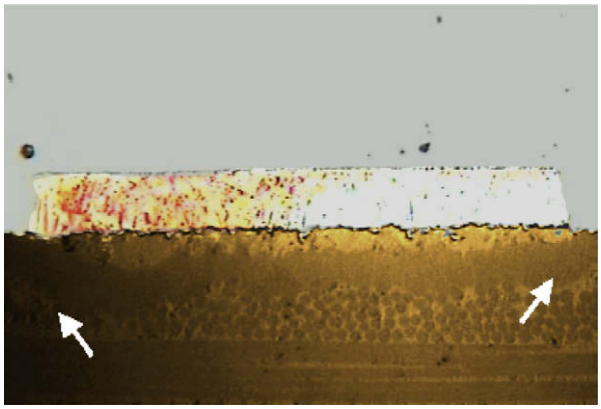

Fig. 14. Crack in board resin underneath pad (thick dark area), no edge bond.

failure mode of broken traces has been reported by Chong et al. [29]. A test vehicle utilizing typical PWB layout for CSPs in electronic devices, such as traces to vias rather than pad to pad daisy chains, may be more appropriate for evaluating board level drop impact reliability. To avoid trace failures, it is recommended to follow the guidelines of JESD22-B113 [31] such as implementing fillet where trace enters the pad and routing the trace out from pad at an angle.

The third failure mode was solder joint fracture. Fig. 17 shows a fracture near the board side intermetallic layer. Solder fracture failures were observed primarily at the board side and only two solder failures were found at the component side.

To investigate whether failure modes differ at different component locations, the failure modes and the component locations were mapped for the 60 components in four boards and shown in Figs. 18–21. The fill color in each device interior indicates the stage of failure: green is not failed, cyan is transitional failure (minor resistance change), orange is temporary discontinuity, and red is permanent discontinuity. The individual solder joints are indicated in the array around each device with failure mode: white squares are not failed, black squares indicate pad crater, red squares indicate solder crack near the board side, and yellow squares indicate solder crack near the component side (only 1 is shown). Note that all four boards were drop tested at 1500 Gs peak acceleration, but the drop count varies for each. Figs. 18 and 19 show boards with no edge-bonding applied to the CSPs and Figs. 20 and 21 show boards with edge-bonding applied.

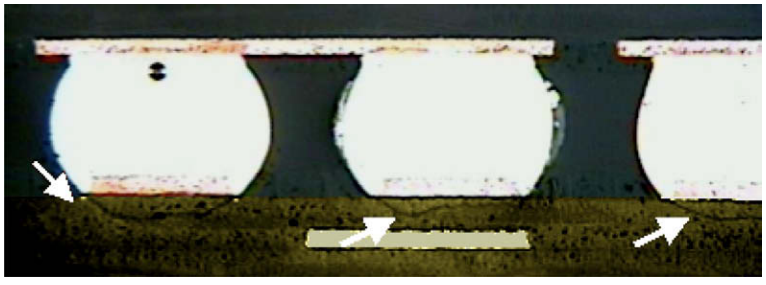

Fig. 15. Cracked resin layer under pads for several solder joints, edge-bonded.

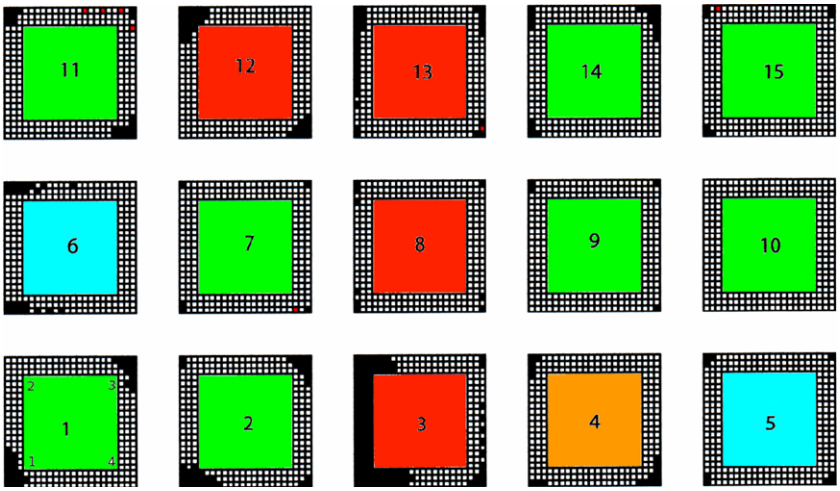

Fig. 18. Failure mode map for none edge-bonded board after 10 drops at 1500 Gs.

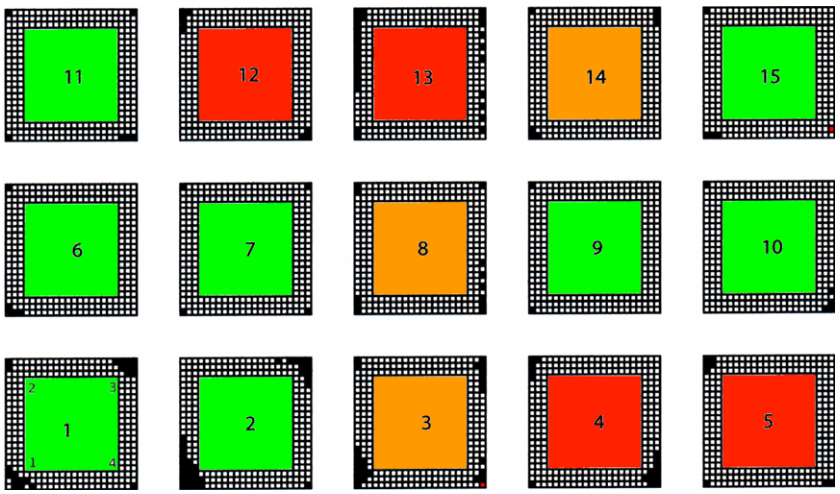

Fig. 19. Failure mode map for none edge-bonded board after 14 drops at 1500 Gs.

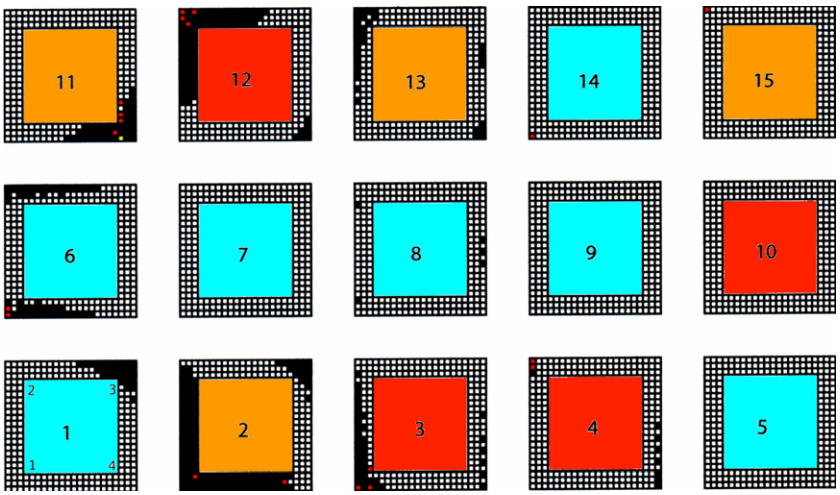

Fig. 20. Failure mode map for edge-bonded board after 279 drops at 1500 Gs.

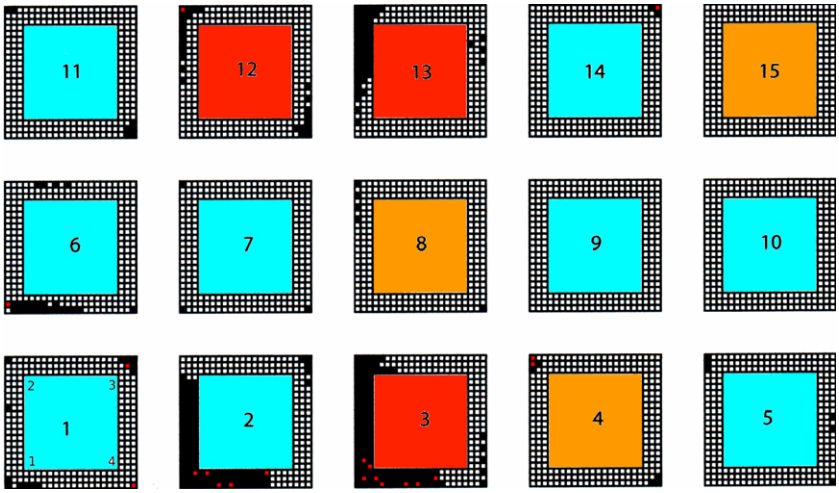

Fig. 21. Failure mode map for edge-bonded board after 325 drops at 1500 Gs.

Table 4
Relationship between electrical failure and resin cracking.

	Electrical failure	
	Yes (%)	No (%)
Resin cracking under pads		
Yes	72	19
No	6	3

It is clear that pad cratering occurred mainly in the corners of the CSPs with the exception of components 3, 8, and 13, where it often happened along the edges. The majority of pad cratering occurred on one side of the board (toward component 6). This may be in part due to the attachment of a cable resulting in asymmetric strain distributions along the board [14].

It should be pointed out that pad cratering does not necessarily lead to electrical failure of solder joints. The relationship between electrical failure and resin cracking for these 60 components dye penetrated is summarized in Table 4. It shows that 72% of components failed electrically and had resin cracking under the copper pad, while 19% of components did not fail electrically but exhibited resin cracking under the copper pad. The remaining 9% of components did not have resin cracking under the copper pad. This indicates that pad lift is a serious issue. It is recommended that board laminate materials be improved.

There are notable differences in the mechanical failure mode between the two edge-bond materials. The epoxy material tends to fracture through the edge-bond material as shown in Fig. 22. More than 20 components that were edge-bonded with the epoxy material, or more than 10% of all the components in the group, dropped off the board during testing. This fracturing was observed

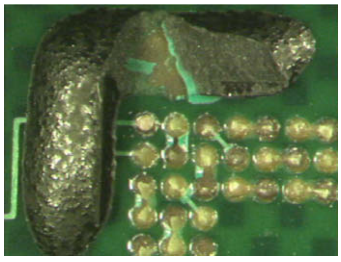

Fig. 22. Fractured thermally cured epoxy edge bond after component fell off in testing.

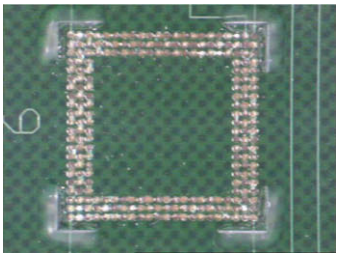

Fig. 23. Four UV-cured acrylic edge bonds on a board after component fell off in testing.

to occur before electrical failure happened. The acrylic edge-bond material did not fracture, but delaminated from the package sides. The acrylic was not observed to be delaminated from the board surface on any components. Fig. 23 shows that four undamaged acrylic edge bonds remained on the board after the component fell off; this was the only component of that group to fall off the board. The properties of these two edge-bond materials are believed to contribute to the difference in the mechanical failure mode; however the effective reliability improvement from applying either of these two materials was statistically similar.

7. Conclusions

This paper reports for the first time the drop test reliability of edge-bonded CSPs. The results show that edge-bonding can significantly improve drop test reliability. The edge-bonded CSPs typically survived 5–8 times longer at 2900 Gs to 0.3 ms drop impacts, and 8–10 times longer at 1500 Gs to 0.5 ms drop impacts. The reliability performances of the two different edge-bond materials were similar while they mechanically failed by different modes. The epoxy material tends to fracture through the edge-bond material while the acrylic edge-bond material did not fracture, but delaminated from the package sides.

The component location plays a significant role in the drop test reliability. Generally speaking, components at the position 8 (JEDEC Group F), and positions 3 and 13 (JEDEC Group E) are more prone to fail, followed by component positions 2, 4, 12, and 14 (JEDEC Group B). A cable or other additional mass attached to a drop test board may change the failure location. Thus, we suggest that the cable effect be considered in a future JEDEC drop test standard.

Higher impact force or G-level typically resulted in lower number of drops-to-failure. But there are large variations in the number

of drops-to-failure between different boards under the same drop conditions. Increasing the number of test boards in future studies is recommended.

Failure analysis showed that pad cratering was the primary failure mode and that this also led to I/O trace cracking on the board side, the second most common failure mode. Solder joint cracking was also observed on the board side near the intermetallic layer, which was the third most common failure mode. The majority of failures occurred at the corners of the packages implying that the corners of the components experience the most stress and strain. The primary failure mode of pad cratering indicates that solder joints may not be the weakest link of the assembly in this study. This suggests that better PCB laminate materials should be used in future drop reliability studies to minimize pad cratering and the laminate specification and testing method should be included in a future JEDEC drop testing standard so that future research results may be more accurately compared.

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References

[1] Lai YS, Yang PC, Yeh CL. Effects of different drop test conditions on board-level reliability of chip-scale packages. Microelectron Reliab 2008;48(2):274–81.
[2] Chong DYR, Che FX, Pang JHL, Ng K, Tan JYN, Low PTH. Drop impact reliability testing for lead-free and lead-based soldered IC packages. Microelectron Reliab 2006;46(7):160–1171.
[3] Lai YS, Wang CC, Yeh CL. Investigations of board-level drop reliability of wafer-level chip-scale packages. ASME J Electron Packag 2007;129(March):105–8.
[4] Syed A, Kim SM, Lin W, Kim JY, Sohn ES, Shin JH. A methodology for drop performance modeling and application for design optimization of chip-scale packages. IEEE Trans Electron Packag Manufact 2007;30(1):42–8.
[5] Qu X, Chen Z, Qi B, Lee T, Wang J. Board level drop test and simulation of leaded and lead-free BGA-PCB assembly. Microelectron Reliab 2007;47:2197–204.
[6] Lall P, Panchagade DR, Liu Y, Johnson RW, Suhling JC. Models for reliability prediction of fine-pitch BGAs and CSPs in shock and drop-impact. IEEE Trans Compon Packag Technol 2006;29(3):464–74.
[7] Liu F, Meng G, Zhao M, Zhao J. Experimental and numerical analysis of BGA lead-free solder joint reliability under board-level drop impact. Microelectron Reliab 2009;49:79–85.
[8] Luan JE, Tee TY, Pek E, Lim CT, Zhong Z. Dynamic response and solder joint reliability under board level drop test. Microelectron Reliab 2007;47:450–60.
[9] Wong EH, Rajoo R, Seah SKW, Selvanayagam CS, Driel WDV, Caers JFJM, et al. Correlation studies for component level ball impact shear test and board level drop test. Microelectron Reliab 2008;48:1069–78.
[10] Chin YT, Lam PK, Yow HK, Tou TY. Investigation of mechanical shock testing of lead-free SAC solder joints in fine pitch BGA package. Microelectron Reliab 2008;48:1079–86.
[11] JEDEC Standard JESD22-B111. Board level drop test method of components for handheld electronic products. JEDEC Solid State Technology Assoc; 2003.
[12] JEDEC Standard JESD22-B104-C. Mechanical shock. JEDEC Solid State Technol Assoc; 2004.
[13] JEDEC Standard JESD22-B110A. Subassembly mechanical Shock. JEDEC Solid State Technol; 2004.
[14] Wong EH, Mai YW, Seah SKW. Board level drop impact – fundamental and parametric analysis. ASME J Electron Packag 2005;127:496–502.
[15] Syed A, Kim TS, Cho YM, Kim CW, Yoo M. Alloying effect of Ni, Co, and Sb in SAC solder for improved drop performance of chip scale packages with Cu OSP pad finish. In: Proc. of 2006 IEEE electronics packaging and technology conference; 2006. p. 404–11.
[16] Pandher RS, Lewis BG, Vangaveti R, Singh B. Drop shock reliability of lead-free alloys – effect of micro-additives. In: Proceedings of 2007 IEEE electronics components and technology conference; 2007. p. 669–76.
[17] Kim H, Zhang M, Kumar CM, Suh D, Liu P, Kim D, et al. Improved drop reliability performance with lead free solders of low Ag content and their failure modes. In: Proceedings of 2007 IEEE electronics components and technology conference; 2007. p. 962–7.
[18] Zhang S, Chen C, Yee S. An investigation on the reliability of CSP solder joints with numerous underfill materials. J SMT 2003;16(3):25–30.
[19] Toleno B, Maslyk D, White T. Using underfills to enhance drop test reliability of Pb-free solder joints in advanced chip scale packages. In: Proceedings of 2007 SMTA pan pacific symposium; 2007.
[20] Liu Y, Tian G, Johnson RW, Crane L. Lead-free chip scale packages: assembly and drop test reliability. IEEE Trans Electron Packag Manufact 2006;29(1):1–9.
[21] Tian G, Liu Y, Johnson RW, Lall P, Palmer M, Islam MN, et al. Corner bonding of CSPs: processing and reliability. IEEE Trans Electron Packag Manufact 2005;28(3):231–40.
[22] Lai YS, Yang PF, Yeh CL. Experimental studies of board-level reliability of chip-scale packages subjected to JEDEC drop test condition. Microelectron Reliab 2006;46(2):645–50.
[23] Marjamaki P, Mattila T, Kivilahti J. Finite element analysis of lead-free drop test boards. In: Proceedings of 2005 IEEE electronics components and technology conference; 2005. p. 462–6.
[24] Luan JE, Tee TY, Pek E, Lim CT, Zhong Z, Zhou J. Advanced numerical and experimental techniques for analysis of dynamic responses and solder joint reliability during drop impact. IEEE Trans Compon Packag Technol 2006;29(3):449–56.
[25] Che FX, Pang JHL, Zhu WH, Sun W, Sun A, Wang CK. Comprehensive modeling of stress–strain behavior for lead-free solder joints under board-level drop impact loading conditions. In: Proceedings of 2007 IEEE electronics components and technology conference; 2007, p. 528–34.
[26] Park S, Shah C,Kwak J, Jang C, Pitarresi J, Park T. Transient dynamic simulation and full-field test validation for a slim-PCB of mobile phone under drop/impact. In: Proceedings of 2007 IEEE electronics components and technology conference; 2007. p. 914–23.
[27] Krist M, Pan J, Farris A, Vickers N. Drop impact dynamic response study of JEDEC JESD22-B111 test board.In: Proceedings of the 41th international symposium on microelectronics (IMAPS'2008), Providence, RI, USA, November 1–6; 2008.
[28] Mattila TT, Marjamaki P, Kivilahti JK. Reliability of CSP interconnections under mechanical shock loading conditions. IEEE Trans Compon PackagTechnol 2006;29(4):787–95.
[29] Chong DYR, Che FX, Pang JHL, Xu L, Xiong BS, Toh HJ, et al. Evaluation of influencing factors of board-level drop reliability for chip scale packages (fine-pitch ball grid array). IEEE Trans Advan Packag 2008;31(1):66–75.
[30] . Vickers N, Rauen K, . Farris A, Pan J. Board level failure analysis of chip scale package drop test assemblies. Proceedings of the 41th international symposium on microelectronics (IMAPS'2008), Providence, RI, USA, Nov. 10–6; 2008.
[31] JEDEC Standard JESD22-B113. Board level cyclic bend test method for interconnect reliability characterization of components for handheld electronic products. JEDEC Solid State Technology Assoc; March 2006. p. 5.