# Effects of Flux and Reflow Parameters on Lead-Free Flip Chip Assembly

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## Abstract

The melting temperatures of most lead-free solder alloys are somewhat higher than that of eutectic Sn/Pb solder, and many of the alloys tend to wet typical contact pads less readily. This tends to narrow down the fluxing and mass reflow process windows for assembly onto typical organic substrates and may enhance requirements on placement accuracy. Flip chip assembly here poses some unique challenges. The small dimensions provide for particular sensitivities to wetting and solder joint collapse, and underfilling does not reduce the demands on the intermetallic bond strength. Rather, the need to underfill lead to additional concerns in terms of underfill process control and reliability. Relatively little can here be learned from work on regular SMT components, BGAs or CSPs.

The present paper addresses the effects of reflow profile, pad metallurgy, and amount of flux on the assembly of flip chips with lead-free solder bumps onto organic substrates. Special attention was paid to the 85.9Sn/3.1Ag/10In/1.0Cu alloy, which has a relatively low melting point of 197$^{o}$C. Good wetting and a robust collapse could, however, not be achieved with flip chip relevant no-clean fluxes developed for eutectic Sn/Pb, even with peak reflow temperatures approaching 250$^{o}$C. In fact, both 95.5Sn/3.5Ag/1.0Cu and 95Sn/5Sb were seen to perform much better at such temperatures. Given the relatively high melting

point of the latter, a Sn/Ag/Cu alloy would seem to offer the more acceptable process windows.

## Introduction

The electronics industry has essentially been built up around lead bearing solders. Lead has been used to form interconnections because of the abundant and cheap supply and because of the physical and chemical properties. Research has, however, repeatedly proven that lead is harmful to human life. The heavy metal is accumulated in the human body under chronic exposition and is capable of harming the blood and nervous system. This has initiated a ban on lead compounds in fuels and in dyes, as well as the replacement of lead pipes used to supply drinking water. So far, limited use of lead has been allowed for lead electrodes in accumulators. The tremendous increase in consumer electronic products with smaller life cycles and recycling of these products at the end of the life cycle have fueled discussions on the use of lead in electronic devices. In principle, at least, lead in electronic devices does endanger humans and the environment through the contamination of groundwater from disposed electronic waste and through the waste-water from flux cleaning with aqueous solutions. The roadmaps outlined by various countries aim at lead-free products in the next five years [Bradley, 1999]. The Japanese roadmap has targeted 2001 as the date for the implementation of lead-free processes. In North America, Original Equipment Manufacturers (OEMs) and Electronics Manufacturing Service (EMS) providers need to prepare processes to deliver lead-free products by 2001 with a ‘target’ of total lead elimination by 2004. In Europe, the Waste from Electrical and Electronic Equipment (WEEE) directive has proposed that the use of lead, mercury, cadmium, hexavalent chromium and halogenated flame retardants be phased out by January 2004 [Haken, 1999]. The WEEE directive is intended to prevent waste generation, promote recovery, encourage recycling, and minimize environmental impact.

The solder volumes used for flip chip assembly tend to be negligible compared to those used elsewhere in an electronic product. However, we cannot count on no-Pb legislation to exempt flip chip, and component manufacturers are busy developing completely Pb-free packages. Also, the integration of a Sn/Pb based Flip-Chip-On-Board process into a no-Pb SMT process would by no means be trivial. Anyway, a Pb-free attachment process also offers potential advantages that are unique to flip chip. Notably, some lead isotopes emit alpha particles which may be harmful to active or near-active circuits [Kang et al., 1999]. In general, both cosmic rays and alpha particles tend to cause soft errors in memory devices. The problem, which becomes more critical with the reduction in cell size in CMOS technology, can be reduced by the use of low-alpha lead but this involves high cost and a somewhat limited supply. Most Pb-free solders should eliminate the contributions from alpha particles completely.

The use of lead free solders does, however, pose a wide range of challenges. The issues are here quite different for leaded devices, area array components and flip chip. The small dimensions involved, make flip chip assembly particularly sensitive to wetting and solder joint collapse, in terms of both selfalignment and soldering [Borgesen, 1999]. Furthermore, while apparently not an issue for eutectic Sn/Pb solder balls of down to 2 mil diameter, the risk of incomplete reflow and solder joint collapse is generally expected to increase with decreasing solder ball dimensions. Alloys that perform well for much larger BGA or CSP balls, particularly when placed in wet solder paste, may thus no longer do so with a smaller amount of no-clean flux of moderate activity at typical flip chip dimensions.

In general, flip chip solder joints should be robust enough to survive transport and handling before underfilling. Also, in spite of the underfill, the joints usually undergo plastic deformation during thermal excursions, i.e. the intermetallic bond strengths at the pad surfaces still have to exceed the ‘bulk’ flow stress. Depending on the alloy and the pad metallurgies, the latter may be higher than for Sn/Pb [Zribi et al., 2001]. Furthermore, even if the bond strength is sufficient, a reduced collapse may enhance the risk of an open connection if the substrate warps during reflow. This can often be accounted for in the substrate pad design [Kondos et al., 2000]. However, an incomplete collapse is also likely to enhance the scatter in the gaps to be underfilled and thus the scatter in the encapsulant edge fillet thicknesses. The latter may seriously affect the statistics of failure in cycling or handling [Borgesen et al., 2000]. Imperfect selfalignment may also put more demands on placement accuracy [Borgesen, 2000].

The performance of eutectic Sn/Pb solder allows for the definition of robust reflow processes with comfortable margins, including peak reflow temperatures 35-45$^o$C or more above liquidus. In comparison, the higher melting points (197$^o$ - 235$^o$C) and reduced wetting properties of most no-Pb alloys invariably leads to a requirement for higher peak reflow temperatures. However, common organic substrates tend to degrade at peak temperatures above about 250$^o$C. The flux reaction rates have been reported to increase with increasing temperature [Lee, 1999]. In another study on the compatibility of lead-free solder alloys with the reflow process, it has been reported that some lead-free alloys have good wetting properties when the reflow temperature is 30$^o$C higher than the liquidus temperature [Huang and Lee, 2000]. These studies have, however, been performed on solder alloys and testing without components [Huang and Lee, 2000]. The narrower process window leads to a need for more careful optimization. Similarly, the simultaneous need for a larger flux volume raises the risk of flux wicking up to the die surface, as well as the effects of flux residues on the underfill, narrowing the flux process window as well. The development of dedicated fluxes, optimized for the alloy of concern, may eventually allow this to be relaxed again. However, more active fluxes often lead to reductions in reliability, and documenting the compatibilities with all relevant combinations of underfill, solder mask, laminate, chip passivation, and contact pad metallurgies is by no means a trivial task.

The present paper addresses no-Pb soldering with no-clean tacky fluxes commonly used for Sn/Pb based flip chip assembly. Three alloys with very different melting points are considered, but emphasis is placed on a Sn/Ag/Cu/In alloy with a melting point of about 197$^{o}$C.

## Experiment

Wetting and solder joint collapse was studied under two substantially different conditions, soldering to a blanket OSP coated copper surface and to individual contact pads on substrates designed to match the die, respectively. In both the cases, the flip chip solder bumps were first dipped into a thin film of a tacky flux on the Thin Film Applicator (TFA) on the GSM placement machine. Numerous different flux film thicknesses between 0.5 and 2.5 mil were considered.

Four different no-clean fluxes (A, B, C, and D) from three different suppliers were investigated. The materials were chosen because they were known to work well for eutectic Sn/Pb on both OSP and Ni/Au coated copper surfaces, and because they would ‘roll’ well on the TFA without forming obvious ‘tracks’ or thickness variations.

After dipping, the bumps were placed on the appropriate contact surfaces and sent with these through an 8-zone Heller full convection oven in a nitrogen atmosphere with about 40 ppm $O_2$. A large number of different reflow profiles with different peak temperatures and times above liquidus were considered. The actual temperature profiles at the die location were all carefully measured with a mole. Depending among other, on the alloy, peak temperatures between 228$^{o}$C and 259$^{o}$C, as well as different times above the liquidus temperature, were considered. However, as the fluxes were developed for eutectic Sn/Pb the initial part of each profile, the ‘soak’, was kept essentially the same.

After reflow, the wet-out of the solder bumps on a blanket Cu(OSP) surface was first measured in a FeinFocus X-ray microscope. Assemblies on actual contact pads were assessed in terms of the solder joint shapes (outlines), the formation of voids, and the electrical resistance of a daisy chain through all the joints. In either case, the assemblies were finally cross-sectioned and the die-substrate gap measured optically.

The following three Pb-free alloys were considered.

The 85.9Sn/3.1Ag/10In/1.0Cu alloy is not a eutectic, but its paste range is small. Its solidus is 194$^{o}$C and the liquidus is 200$^{o}$C. 4 mil tall balls on the test die were soldered onto either blanket OSP coated copper substrates or 1.5 mil thick, 5 mil wide Ni/Au coated copper traces through 5 mil wide solder mask windows. Three different reflow profiles were employed. Profile 1 had a peak temperature of 228°C and a time of 59 seconds above 197°C (Figure 1). Profile 2 had a similar peak temperature, but the belt speed was reduced so that all times were extended by a factor of 1.16. Profile 3 had a peak temperature of 241°C and a time of 71 seconds above 197°C. Three different fluxes (A, B, and C) were considered.

The 95.5Sn/3.5Ag/1.0Cu alloy is near-eutectic and has a melting point of around 217°C. 4 mil tall balls were soldered onto 2 mil thick, 3 mil wide traces through 7 mil wide solder mask windows. Both OSP coated and Ni/Au coated copper traces were considered. Only one flux (D) was tested so far, but different reflow profiles were considered. Peak temperatures were varied between 234°C and 250°C, and times above 217°C between 40 and 110 seconds.

The 95Sn/5Sb alloy has a rather high melting point, 235°C. 4 mil tall balls were soldered onto 2 mil thick, 3.5 mil wide Ni/Au coated copper traces through 6.5 mil wide solder mask windows. In this case another flux (D) which is somewhat similar to, but slightly less active than, flux A was employed. Two different reflow profiles were considered. Profile A1 had a peak temperature of 250°C and a time of 45 seconds above 235°C. Profile A2 had a peak temperature of 259°C and time of 61 seconds above 235°C.

In each case the results were compared to those obtained for die with 4 mil tall eutectic Sn/Pb balls. In this case a standard SMT reflow profile with a peak temperature of about 215°C and 64 seconds above liquidus was employed. These results did not depend on which of the four fluxes was used.

## Results

The Sn/Ag/Cu/In alloy is in principle attractive because of its relatively low melting point. The cost and limited supply of In is not necessarily critical for flip chip applications where the overall solder volume is very small. However, as we shall see, the Sn/Ag/Cu and Sn/Sb alloys tend to wet and collapse more effectively in spite of their much higher melting points.

A minimum requirement of a soldering process is that it allows effective collapse on a blanket substrate where there is nothing to limit the solder wet-out. Figure 2 shows an X-ray image of an 8 mil pitch perimeter array die with eutectic Sn/Pb balls after reflow on a blanket OSP coated copper surface. The 4 mil tall balls had here been dipped in a 1.5 mil thick film of flux D and the ‘assembly’ then sent through a standard SMT reflow profile. We notice a strong wet-out and bridging between the joints. Cross sectioning revealed a standoff of less than 1 mil.

***85.9Sn/3.1Ag/10In/1.0Cu:*** Consider first flux A. The 4 mil tall balls on a test die were dipped in an 0.5 mil thick film of this flux and placed on a blanket Cu(OSP) substrate. The 'assembly' was then reflowed using a peak temperature of 228°C and 59 seconds above liquidus, i.e. Profile 1 (Figure 1). One might expect this to be analogous to a profile with a peak temperature of 214°C for eutectic Sn/Pb. However, in the present case it led to very little collapse, to a standoff of about 3 mil, and no bridging between the joints. Raising the flux thickness to 2 mil did improve on this, leading to some bridging and a standoff of 1.5 mil. Reducing the belt speed to 'stretch' the profile by a factor of 1.16 (Profile 2) had no measurable influence on this. Raising the peak temperature by 13°C (Profile 3) had only a very small effect. Dipping again in a 2 mil thick flux film the balls collapsed to a standoff of 1.4 mil.

Flux B performed largely the same. Figure 3 shows the result of dipping in a 0.5 mil thick film of this flux and reflowing using Profile 3. There was again very little collapse, to a standoff of about 3.1 mil, and no bridging. Figure 4 shows the effect of raising the flux thickness to 2.5 mil. This led to a standoff of about 1.6 mil. Again, the result was not very sensitive to the peak reflow temperature. Figure 5 shows the result for Profile 1 and a flux thickness of 2.5 mil. The standoff was 1.5 mil.

One notable effect of using flux B was the appearance of large voids in the reflowed solder. This phenomenon was not observed for the other two fluxes. Figure 6 shows the result of dipping in a 2.5 mil thick film of flux C and reflowing using Profile 3. This led to some bridging and a standoff of 1.5 mil, like for the other two fluxes. There was, however, no indication of voiding. Reducing the flux thickness to 0.5 mil led to no solder bridging and a standoff of about 3.9 mil, i.e. this flux may be slightly less effective than the other two for such small thicknesses.

In the second part of this experiment the daisy chained die was placed onto electrically testable substrates with 5 mil wide Ni/Au coated copper pads. Dipping the balls into various thicknesses of flux A and reflow soldering according to Profile 1 or Profile 3, generally led to electrically good assemblies, i.e. there was no measurable effect of flux thickness or profile on the electrical resistance. However, the sample size was much too low to reveal defects at the statistical level of concern in manufacturing. Indeed, both flux thickness and profile appeared to affect the solder joint wetting and collapse.

Figure 7 shows a cross section of solder joints achieved by dipping the 4 mil tall balls in a 1 mil thick film of flux A and reflowing according to Profile 1. There is very little collapse, leaving a gap of close to 4 mil between the die and the surface of the contact pad. Raising the peak temperature from 228°C to 241°C, i.e. using Profile 3, appeared to improve this slightly. The gap is reduced to 3.3 mil (Figure 8), but many joints still did not seem to have soldered very well. Effective improvements seemed to require a combination of larger flux thickness and relatively high reflow temperatures. Dipping in a 2.5 mil thick flux film and reflowing according to Profile 1 led to a gap of about 3.1 mil (Figure 9), i.e. a clear improvement over the collapse achieved with a 1 mil flux film and this profile (compare Figure 7). Finally, dipping in 2.5 mil of flux and reflowing according to Profile 3 led to a gap of 3 mil and slight indications of wetting to the vertical sides of the pads as well (Figure 10).

Still, effective wetting and collapse was not achieved for this alloy. For comparison, Figure 11 shows a cross section of eutectic Sn/Pb solder joints achieved with a 1 mil thick flux film and a standard SMT reflow profile. The joints are seen to collapse much more effectively than for Sn/Ag/Cu/In, wetting well to the vertical sides of the pads as well, and reducing the gap between die and pad surface to about 2 mil.

The reduced collapse of the Sn/Ag/Cu/In joints is not necessarily a cause for concern for the present substrate pad design [Borgesen, 2000], although a reduced selfalignment might be. However, even smaller reductions in collapse may have serious consequences for the overall assembly yields with different substrate configurations [Kondos, 2000].

***95.5Sn/3.5Ag/1.0Cu:*** This alloy also proved sensitive to flux thickness and, depending on the pad metallurgy, also to a minor degree on the reflow temperature. As for the pad metallurgy the effects on intermetallic formation and ‘bulk’ solder composition [Zribi et al.] are, however, of greater concern than the effects on the reflow process. All of this will be the subject of forthcoming reports.

For our present purposes Figure 12 shows a cross section of solder joints achieved by dipping Sn/Ag/Cu balls in a 2 mil thick film of flux D, placing them onto Au/Ni/Cu pads and reflowing with a peak temperature of 241$^{o}$C. The resulting gap between die and pad surface is 2.1 mil. We note that the pad dimensions are quite different from those used for Sn/Ag/Cu/In above, so a quantitative comparison with Figure 10 is not straightforward. However, the present Sn/Ag/Cu joints clearly show better wetting under the same fluxing and reflow conditions. Also, Figure 13 shows eutectic Sn/Pb joints on the same type of pads for comparison. The Sn/Ag/Cu joints seem quite similar to these.

***95Sn/5Sb:*** The high melting point (235$^{o}$C) together with the risk of damaging the substrate at high temperatures make for a rather narrow reflow temperature window. However, it is interesting to see that this alloy still offers better wetting good soldering required more flux than for eutectic Sn/Pb. Figure 14 shows a cross section of Sn/Sb solder joints achieved by dipping the 4 mil tall balls in 2.5 mil thick film of flux D, placing them on Au/Ni/Cu pads and reflowing with a peak temperature of 250$^{o}$C (Profile A1). For comparison, Figure 15 shows eutectic Sn/Pb joints on the same type of pads. Overall wetting and collapse are quite comparable. An actual reflow/process window will be reported elsewhere.

## Conclusions

The small dimensions involved makes it difficult to develop an optimized solder based flip chip assembly process without ensuring full collapse of the joints to their equilibrium shape in mass reflow. All three lead free alloys considered here was found to require more flux than eutectic Sn/Pb to ensure this. In fact, the wetting properties of the Sn/Ag/Cu/In alloy were not very good and robust collapse could not be achieved with any of the three no-clean fluxes tested. Unless dedicated fluxes can be developed to alleviate this, the alloy is therefore not attractive for general flip chip assembly in spite of the relatively low melting point. The Sn/Ag/Cu and Sn/Sb alloys did perform almost as well as eutectic Sn/Pb with peak reflow temperatures around the 250$^{o}$C. Indications are that the former can be also be used at somewhat lower temperatures, making it the more attractive candidate from the perspective of assembly.

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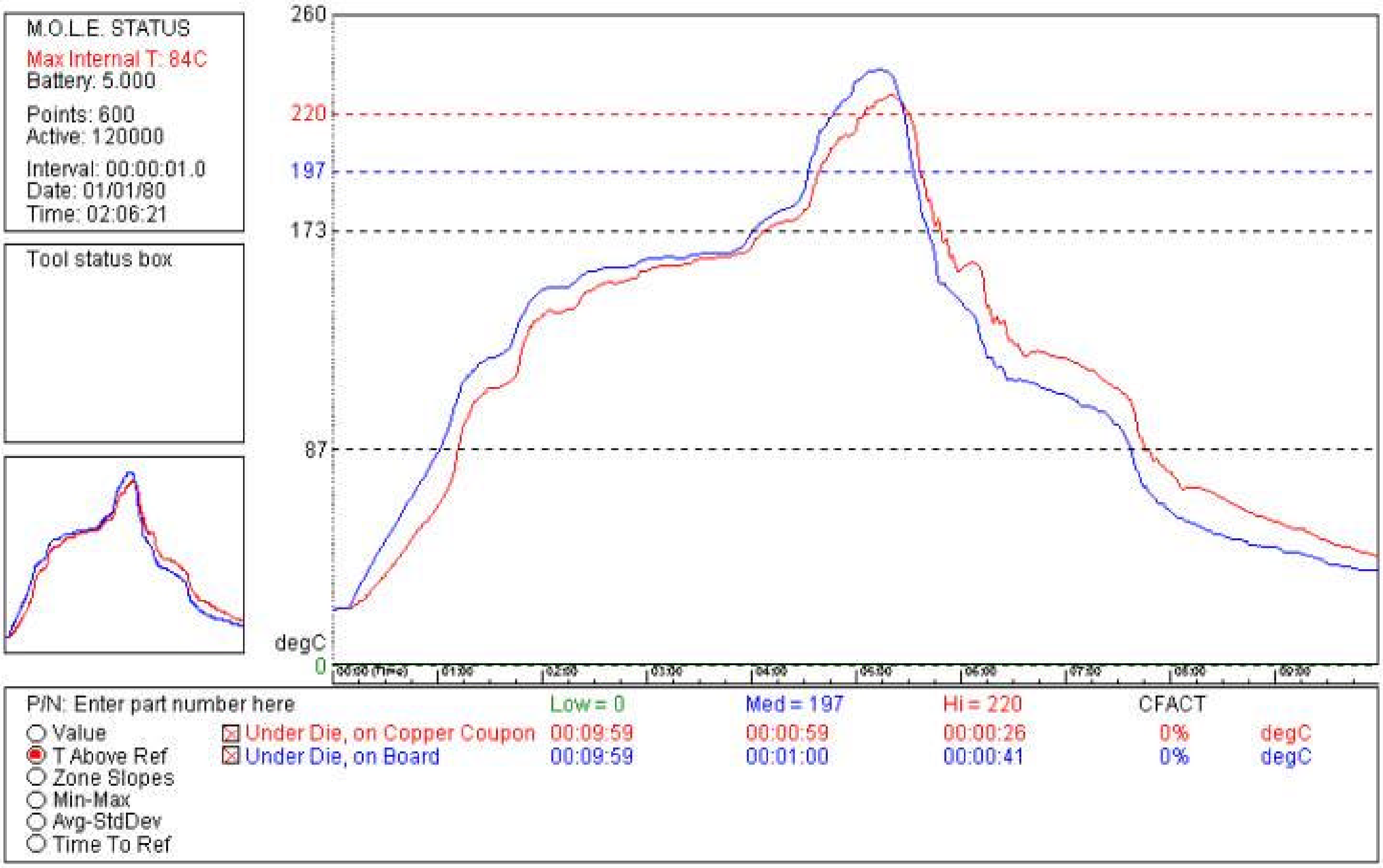
Figure 1.



M.O.L.E. STATUS
Max Internal T: 84C
Battery: 5.000
Points: 600
Active: 120000
Interval: 00:00:01.0
Date: 01/01/80
Time: 02:06:21

Tool status box

P/N: Enter part number here

○ Value
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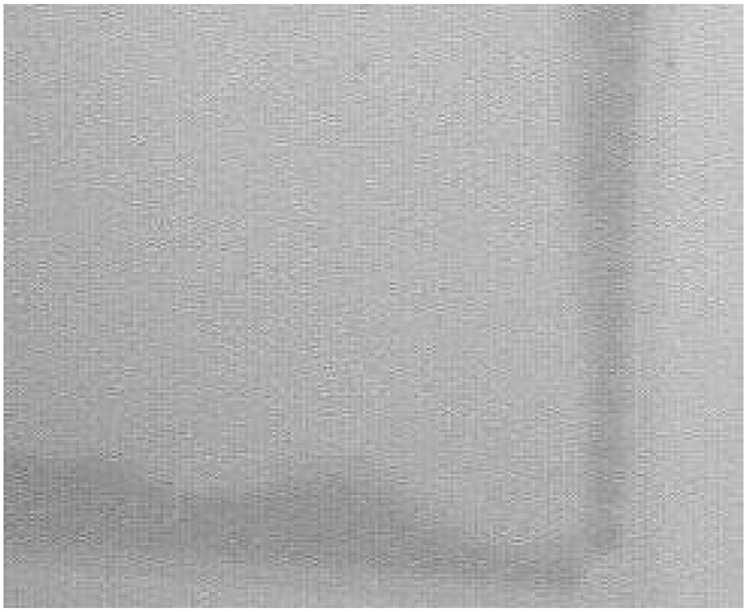
| | Low = 0 | Med = 197 | Hi = 220 | CFACT | |
|---|---|---|---|---|---|
| ☒ Under Die, on Copper Coupon | 00:09:59 | 00:00:59 | 00:00:26 | 0% | degC |
| ☒ Under Die, on Board | 00:09:59 | 00:01:00 | 00:00:41 | 0% | degC |

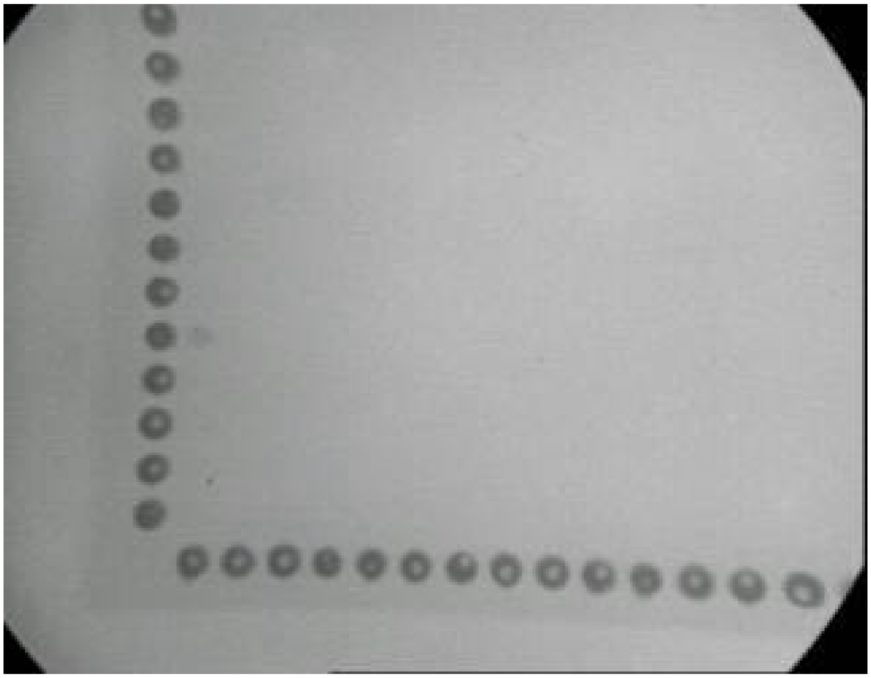
Reflow Profile 1

Figure 2.



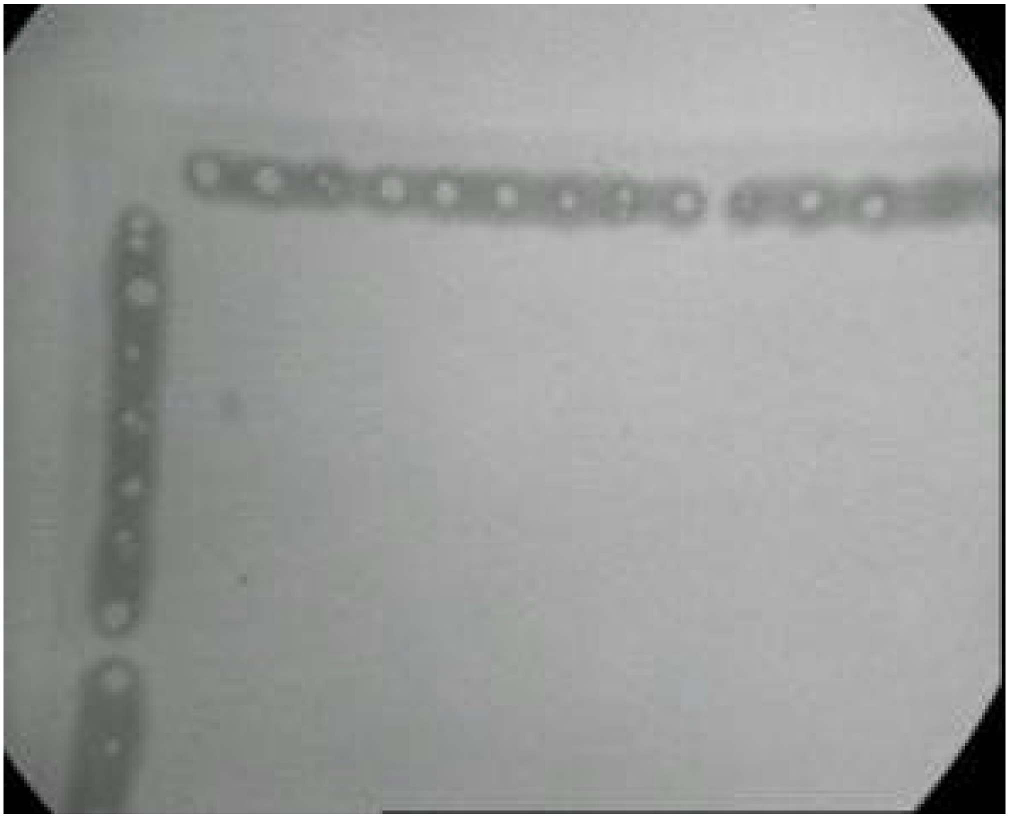
Die with Sn/Pb Bumps Dipped in a 1 mil Thick Film of Flux D, Placed on Blanket Cu(OSP) Substrate and Reflowed According to a Standard SMT Profile

Figure 3.



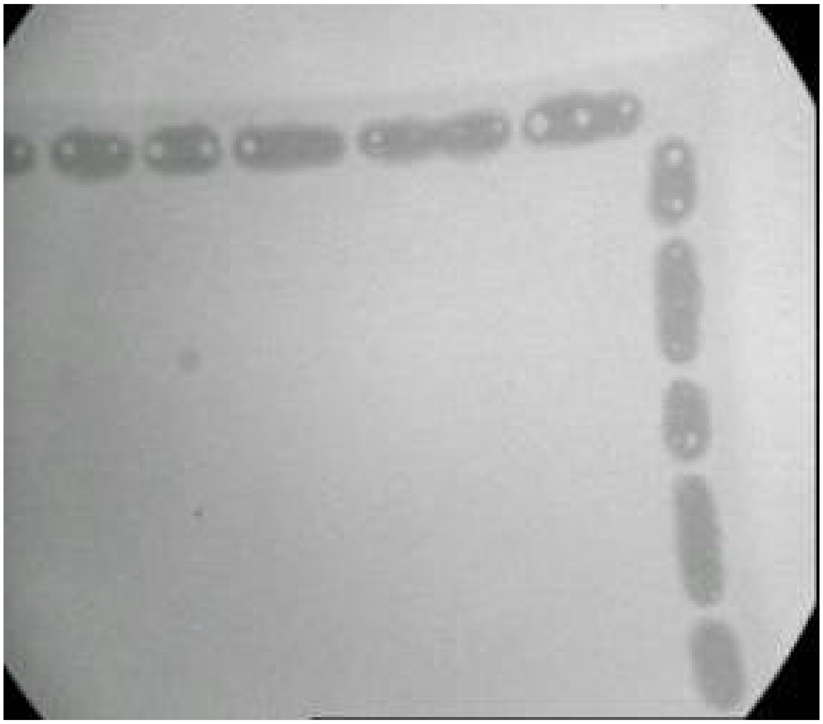
Die with LF-1 Bumps Dipped in a 0.5 mil Thick Film of Flux B, Placed on Blanket Cu(OSP) Substrate and Reflowed According to Profile 3

Figure 4.



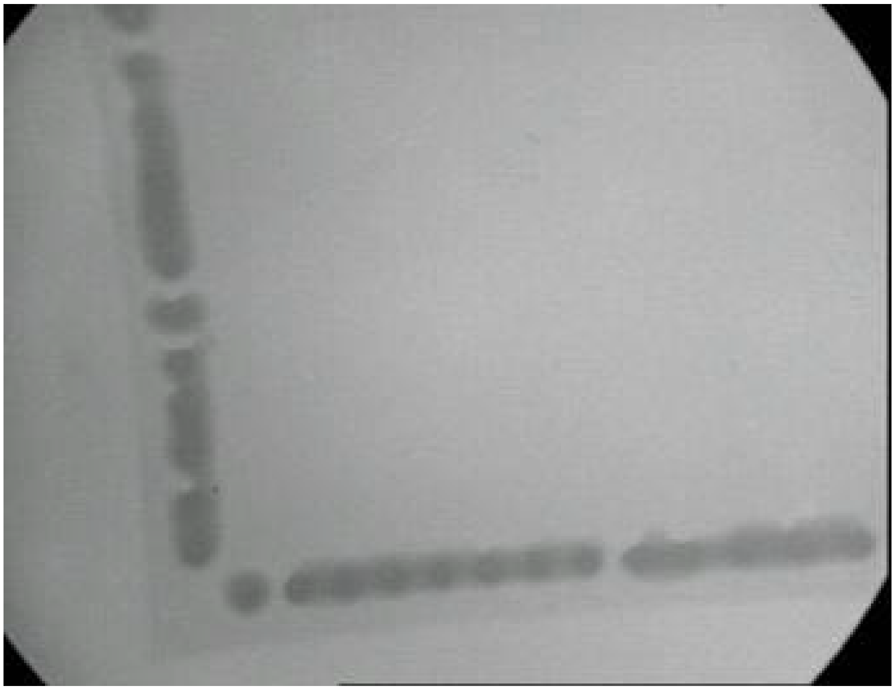
Die with LF-1 Bumps Dipped in a 2.5 mil Thick Film of Flux B, Placed on Blanket Cu(OSP) Substrate and Reflowed According to Profile 3

Figure 5.



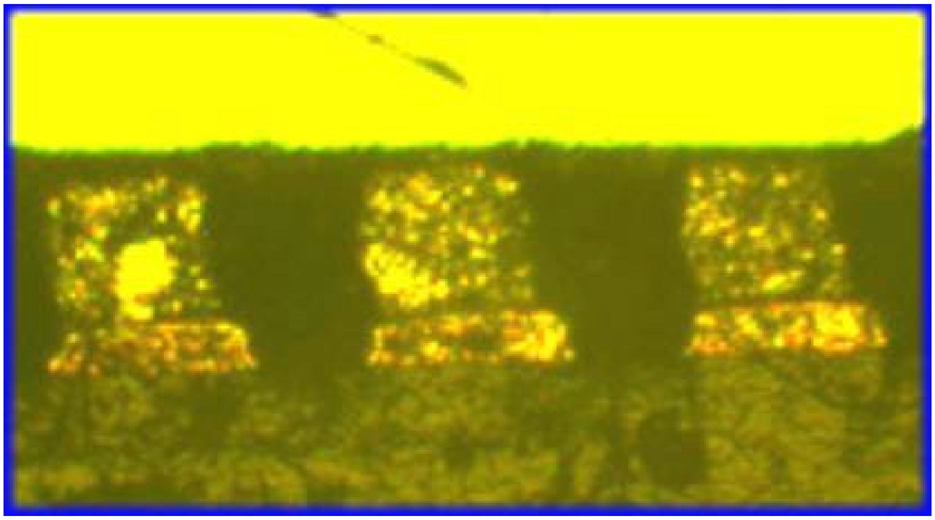
Die with LF-1 Bumps Dipped in a 2.5 mil Thick Film of Flux B, Placed on Blanket Cu(OSP) Substrate and Reflowed According to Profile 1

Figure 6.



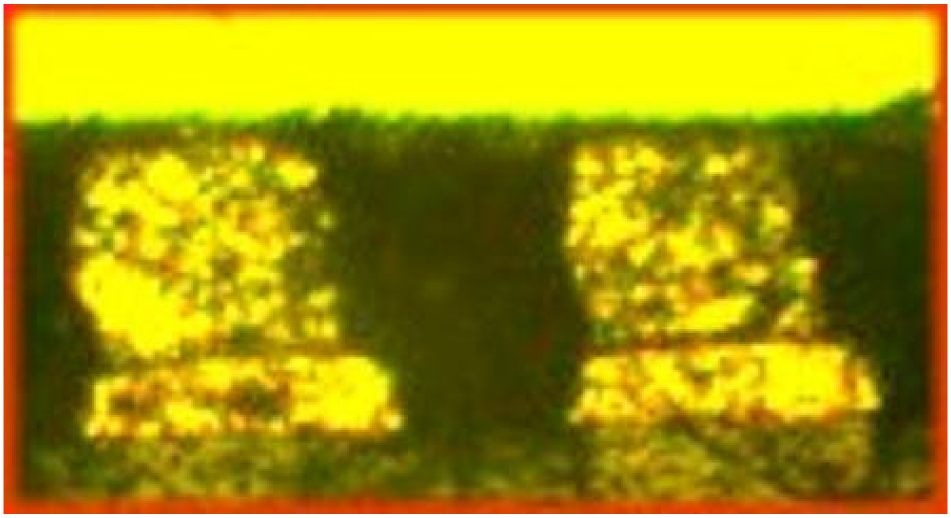
Die with LF-1 Bumps Dipped in a 2.5 mil Thick Film of Flux C, Placed on Blanket Cu(OSP) Substrate and Reflowed According to Profile 3

Figure 7.



Cross-section of a Die with LF-1 Bumps Dipped in a 1 mil Thick Film of Flux A, Placed on a Substrate with Ni/Au Pads and Reflowed According to Profile 1

Figure 8.

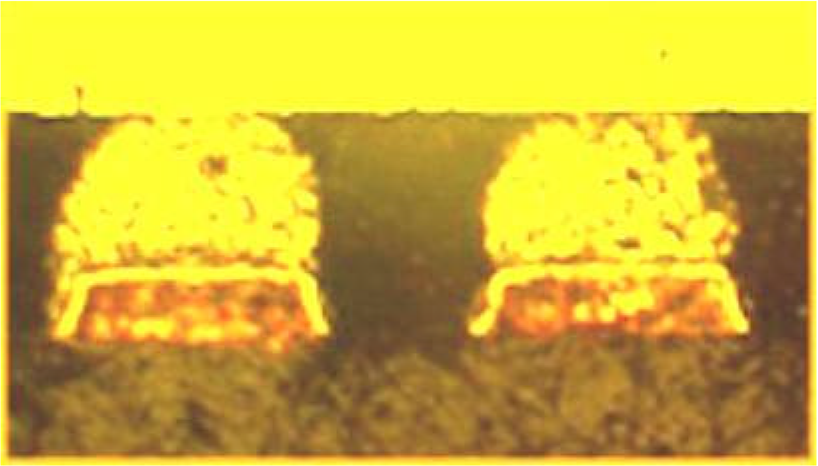


Cross-section of a Die with LF-1 Bumps Dipped in a 1 mil Thick Film of Flux A, Placed on a Substrate with Ni/Au Pads and Reflowed According to Profile 3

Figure 9.

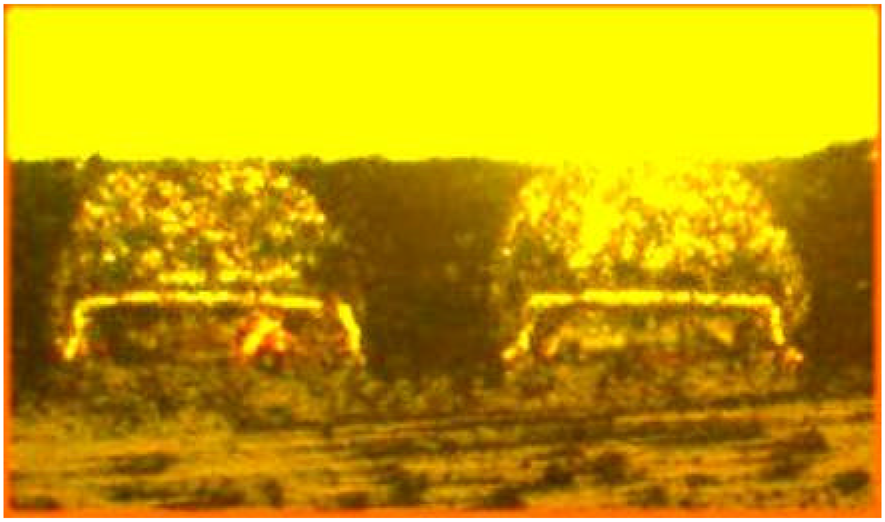
Cross-section of a Die with LF-1 Bumps Dipped in a 2.5 mil Thick Film of Flux A, Placed on a Substrate with Ni/Au Pads and Reflowed According to Profile 1

Figure 10.



Cross-section of a Die with LF-1 Bumps Dipped in a 2.5 mil Thick Film of Flux A, Placed on a Substrate with Ni/Au Pads and Reflowed According to Profile 3

Figure 11.

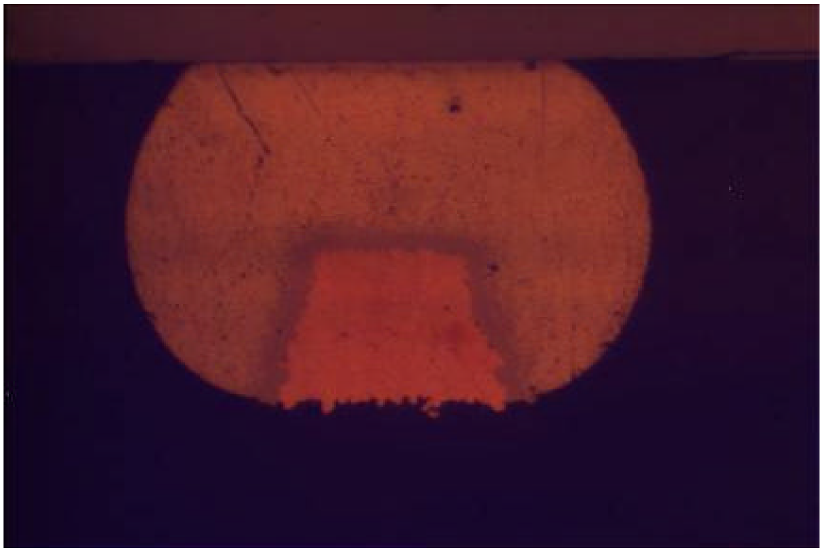


Cross-section of a Die with Sn/Pb Bumps Dipped in a 1 mil Thick Film of Flux A, Placed on a Substrate with Ni/Au Pads and Reflowed According to the Standard SMT Profile

Figure 12.

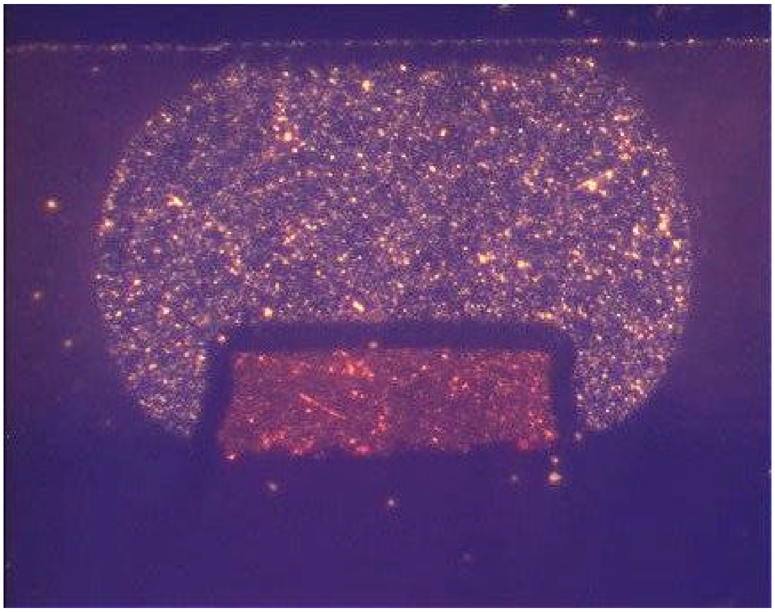
Cross-section of a Die with LF-2 Bumps Dipped in a 2 mil Thick Film of Flux D, Placed on a Substrate with Ni/Au Pads and Reflowed with a Peak Temperature of 241 °C

Figure 13.



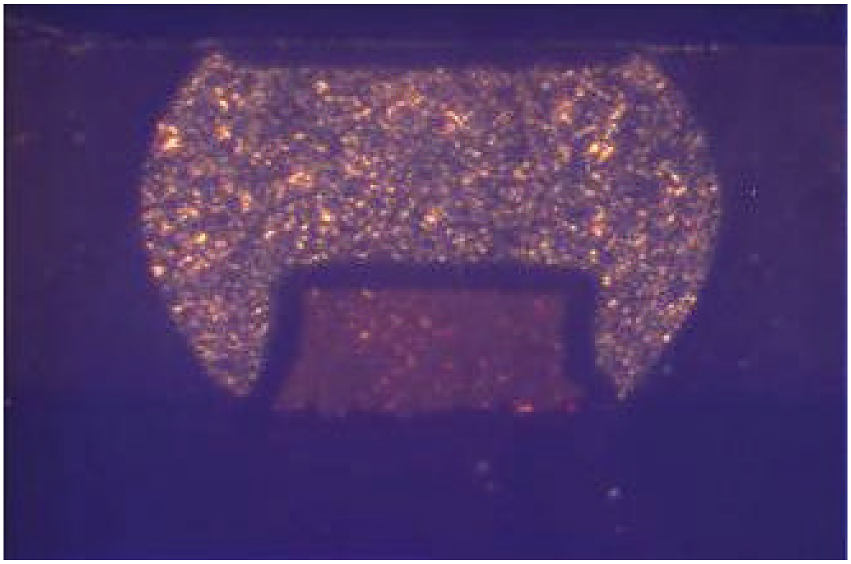
Cross-section of a Die with Sn/Pb Bumps Dipped in a 2 mil Thick Film of Flux D, Placed on a Substrate with Ni/Au Pads and Reflowed According to a Standard SMT Profile

Figure 14.



Cross-section of a Die with Sn/Sb Bumps Dipped in a 2.5 mil Thick Film of Flux D, Placed on a Substrate with Ni/Au Pads and Reflowed According to Profile A1

Figure 15.



Cross-section of a Die with Sn/Pb Bumps Dipped in a 2 mil Thick Film of Flux D, Placed on a Substrate with Ni/Au Pads and Reflowed According to a Standard SMT Profile