Manufacturing Substrates with Embedded Passives

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Passives account for a very large part of today's electronic assemblies. This is particularly true for digital products such as cellular phones, camcorders, and computers. Market pressures for new products with more features, smaller size and lower cost virtually demand smaller, compact, complex circuit boards. An obvious strategy is to reduce the number of surface mounted passives by embedding them in the substrate or printed wire boards. In addition, current interconnect technology to accommodate surface mounted passives impose certain limits on board design, which limit the overall circuit speed. Embedding passives is one way to save substrate real estate, conversion cost, reduce parasitic effects and improve performance [1].

Among the various passives, embedded capacitors deserve special attention as they provide the greatest potential benefit for high density, high speed and low voltage IC packaging. Capacitors can be embedded into the interconnect substrates (printed wiring board, flex, MCM-L, interposer) to provide decoupling, bypass, termination, and frequency determining functions [2,3]. Available commercial polymer composite technology is not adequate for high capacitance density thin film embedded passives. In this paper, we report novel polymer nanocomposites that have the potential to surpass conventional composites to produce high capacitance density, low loss, large area, thin film capacitors.

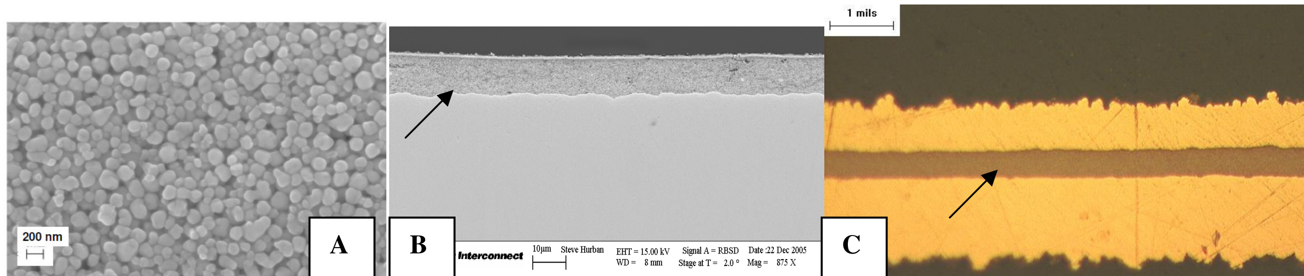

Figure 1: (A) Larger area SEM images of composite, (B) cross sections of thin film, and (C) cross sections of thin films laminated with each other

This paper presents an entire process from design and fabrication to electrical characterization and reliability test of embedded capacitors on organic multilayered substrates. A real challenge in the development of large area thin film nanocomposites is the incompatibility that exists between the typically hydrophilic nanoparticles and hydrophobic polymer matrix, which leads to nanoparticle agglomeration. As a result inferior coatings with poor performance are obtained. We have identified proper surface treatment that results in excellent dispersability of the nanoparticles and good quality, monolithic coatings. The finer details of the particles and their surface morphologies were investigated using SEM. **Figure 1A** show the scanning electron micrographs of nanocomposite thin films. Nanoparticles formed uniform dispersion in the epoxy matrix. The particles in the epoxy matrix are so intimately compacted that analysis of individual particle is difficult. However, closer observation of the micrographs clearly reveals a uniform distribution of closely packed, well connected particles. **Figure 1B** shows cross sections of thin films sandwiched between two metal electrodes. It is possible to make a wide variety of films with different thickness. Desired thickness of the film can be achieved by controlling the viscosity of the coatings, composition and the number of layers deposited. In the present

process, we can easily deposit thin films from about 2 microns to about 25 microns. **Figure 1B** shows a thin film with average thicknesses in the range of 8.5 microns as typical representative examples. **Figure 1C** shows cross sections of two thin films laminated with each other. Thicknesses of the films will contribute to the overall thickness of laminates.

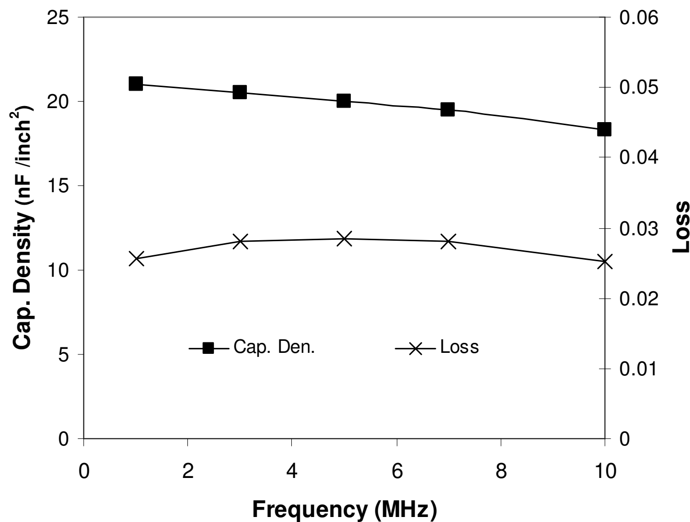

Figure 2A : Capacitance density and loss as a function of frequency .

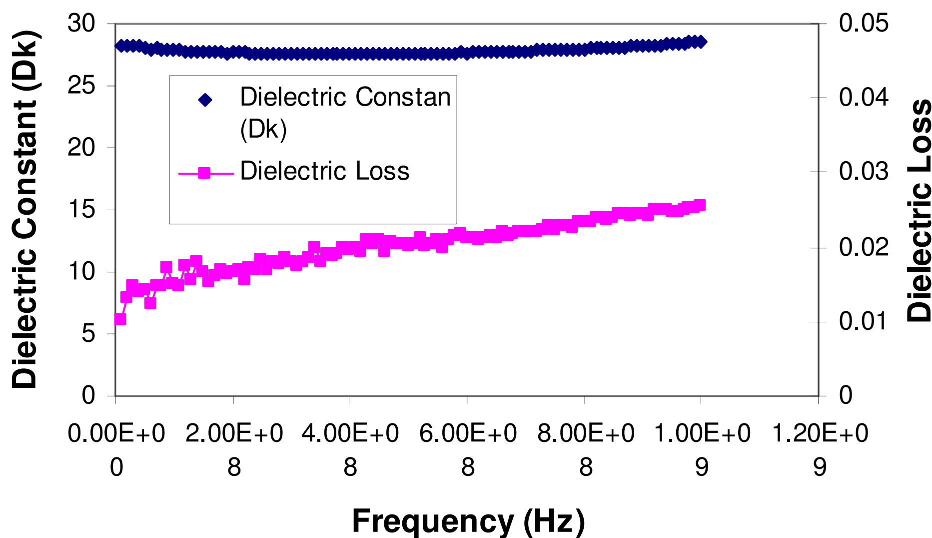

Figure 2B: Dielectric constant (Dk) and loss as a function of frequency for printable materials.

Figure 2A shows the room temperature capacitance profile measured at 1MHz - 10 MHz for a $BaTiO_3$ epoxy nanocomposite thin film as a typical representative example. It was found that with increasing frequency (1-10 MHz), the capacitance density decreased. Change in capacitance with frequency was less pronounced in the case of thicker films. Most of the nanocomposites tested, 8 µm through 25 µm thick, for which the $BaTiO_3$-based ceramic filler concentration was less than 60 vol%, passed 100 volt test. The outcome of high voltage testing depends upon the microstructure and thickness of the film. Nanocomposite film 8 microns thick and consisting of 120 nm particles (Figure 1A) passed 100 volts, whereas 25 µm thick films passed >500 volt tests. Tensile strength with 1 oz copper for all nanocomposites below 60 vol% was found to be higher than 3700 PSI. **Figure 2B** shows the dielectric

constant (Dk) and dissipation factor measured at 1MHz - 1000MHz for a $BaTiO_3$ epoxy nanocomposite as a typical representative example. Minimum Dk (3.7) and loss (0.017) was observed for pure epoxy. Addition of high dielectric constant (~1200) barium titanate particle into the epoxy matrix increases the overall dielectric constant. The dielectric properties of a nanocomposite are likely influenced in two ways: (a) by microstructure of the composite, and (b) by change in the interfacial or Maxwell's polarization at the interfaces. For a well dispersed barium titanate nanocomposite, interface polarization has a great contribution on the dielectric property. According to Maxwell's rule for dielectric mixtures, the measured Dk (composite) values should exceed the corresponding epoxy Dk such that Dk (epoxy) < Dk (composite) < Dk (particle). The dielectric loss increases from 0.01 to 0.025 with increasing frequency .

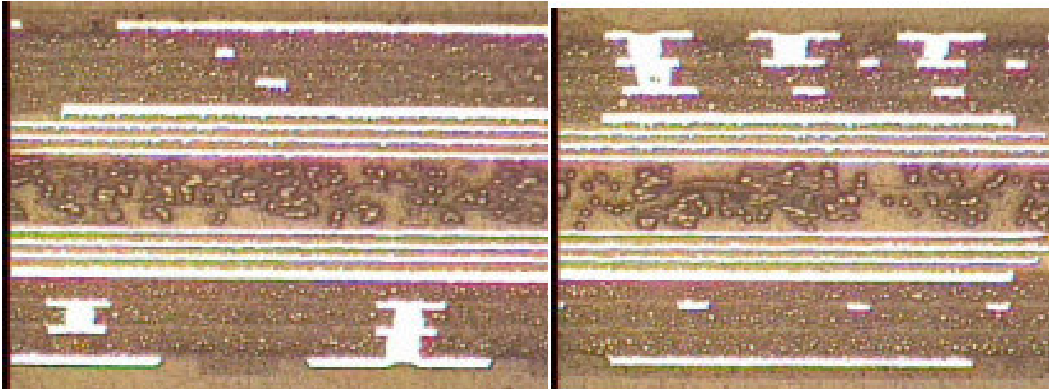

Figure 3: System in a Package (SiP) with embedded resistors and capacitors.

We have designed and fabricated several printed wiring board (PWB) and flip-chip package test vehicles focusing on resistors and capacitors. Two basic capacitor cores were used for this study. One is a layer capacitor. The second capacitor in this case study was discrete capacitor. In both cases, capacitance values are defined by the feature size, thickness and dielectric constant of the polymer-ceramic compositions. Nanocomposite can be directly deposited either by liquid coating or screen printing. Alternatively, nanocomposite thin films can be laminated and capacitor laminate can be used as the base substrate for subsequent build-up processing. For example, Resin Coated Copper Capacitive (RC3) nanocomposites were used to fabricate 35 mm substrates with a two by two array of 15mm square isolated epoxy based regions; each having two to six RC3 based embedded capacitance layers. The total TV core consists of four to eight metal layers. Design features, including antipad diameters, internal plane pickups for vias, and core via pitch were varied within each 15 mm square region. High temperature/pressure lamination was used to embed 6 capacitance layers into the 8 layer internal core. The capacitor fabrication is based on a sequential build-up technology employing a first patternable electrode. After patterning of the electrode, RC3 nanocomposite can be laminated within PCB. An Impedance and network Analyzer was used for dielectric characterization of 8 layers core. Cores are showing high capacitance density ranging from 15 nF to 30nF depending on Cu area, composition and thickness of the capacitors. When the capacitor is embedded in the substrate, the impedance from the active device to the supporting capacitor can be much lower than with a discrete SMT capacitor. Therefore, a much lower capacitor value can provide the required filtering.

In another design, we have used eight layer high density internal core and subsequent fine geometry 3 buildup layers to form a 3-8-3 structure (**Figure 3**). The eight layer internal core has two resistance layers in the middle and the 6 capacitance layer sequentially applied on the surface. This allows multiple capacitance layers in a thin total structure. The resin coated copper capacitive nanocomposite layer does

not need to supply any structural support; it can be very thin and achieve high values of capacitance per unit area. Also, since it is not structural, the material choices expand significantly. The structure with small vias allows the vias to thread through the legs of the serpentine resistors and significantly improves z-directional communication. This is especially important when there are multiple voltages that are supported by the capacitor layers. The overall approach lends itself to package miniaturization because capacitance can be increased through multiple layers and reduced thickness to give the desired values in a smaller area. These layers can be accessed because the laser drilled small holes (about 50 um diameter) do not consume large amounts of capacitive area.

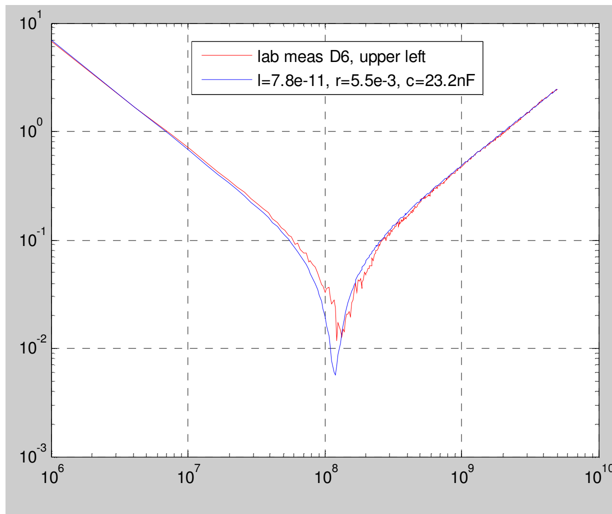

Figure 4: Capacitance and Impedance profile of Capacitors.

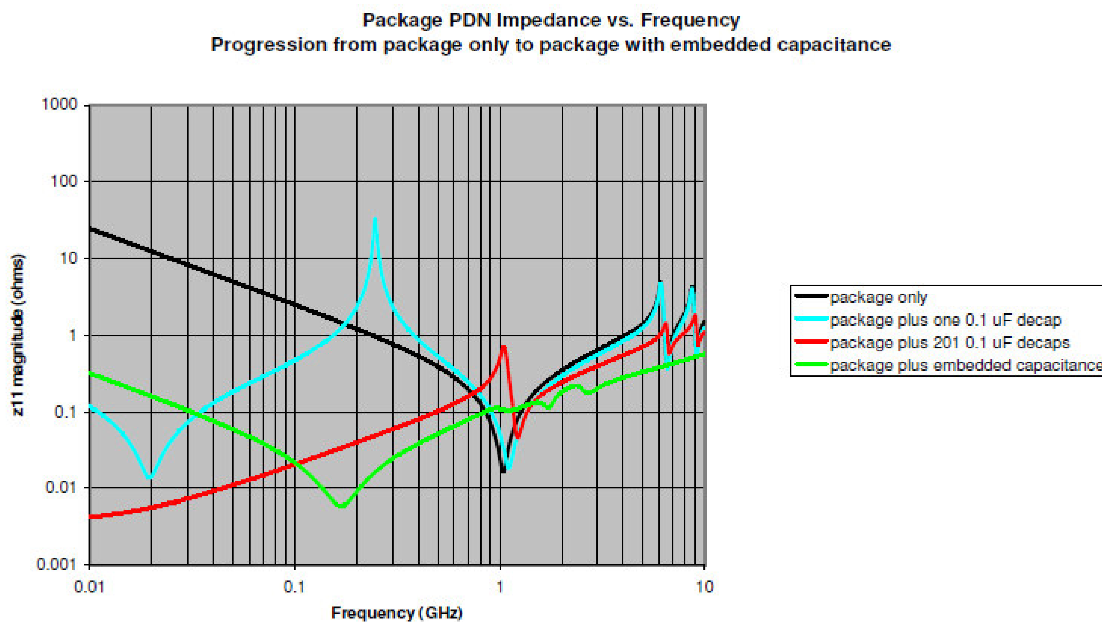

Figure 5 : Power Distribution Impedance Profile showing enhanced performance of embedded capacitance over SMT components.

The electrical properties of multilayer embedded capacitors fabricated from RC3 nanocomposite thin films showed high capacitance ranging from 16nF to 28 nF, depending on Cu area, composition and

thickness of the capacitors. **Figure 4** shows high frequency capacitance profile of 15 mm square capacitors. The curve fitting indicates that these capacitors are equivalent to 23 nF bulk capacitance. **Figure 5** shows the simulated impact on power distribution impedance when discrete SMT capacitors are replaced with embedded capacitance. Impedance is reduced at frequencies greater than 1.5 GHz and high frequency resonances are dampened.

Reliability of the test vehicles was ascertained by IR-reflow, thermal cycling, PCT (Pressure Cooker Test) and solder shock. Embedded discrete capacitors were stable after PCT and solder shock. Capacitance change was less than 5% after IR reflow (assembly) preconditioning (3X, 245 ^{o}C) and 1000 cycles DTC (Deep Thermal Cycle). Detailed electrical characterization and reliability evaluations are in progress.

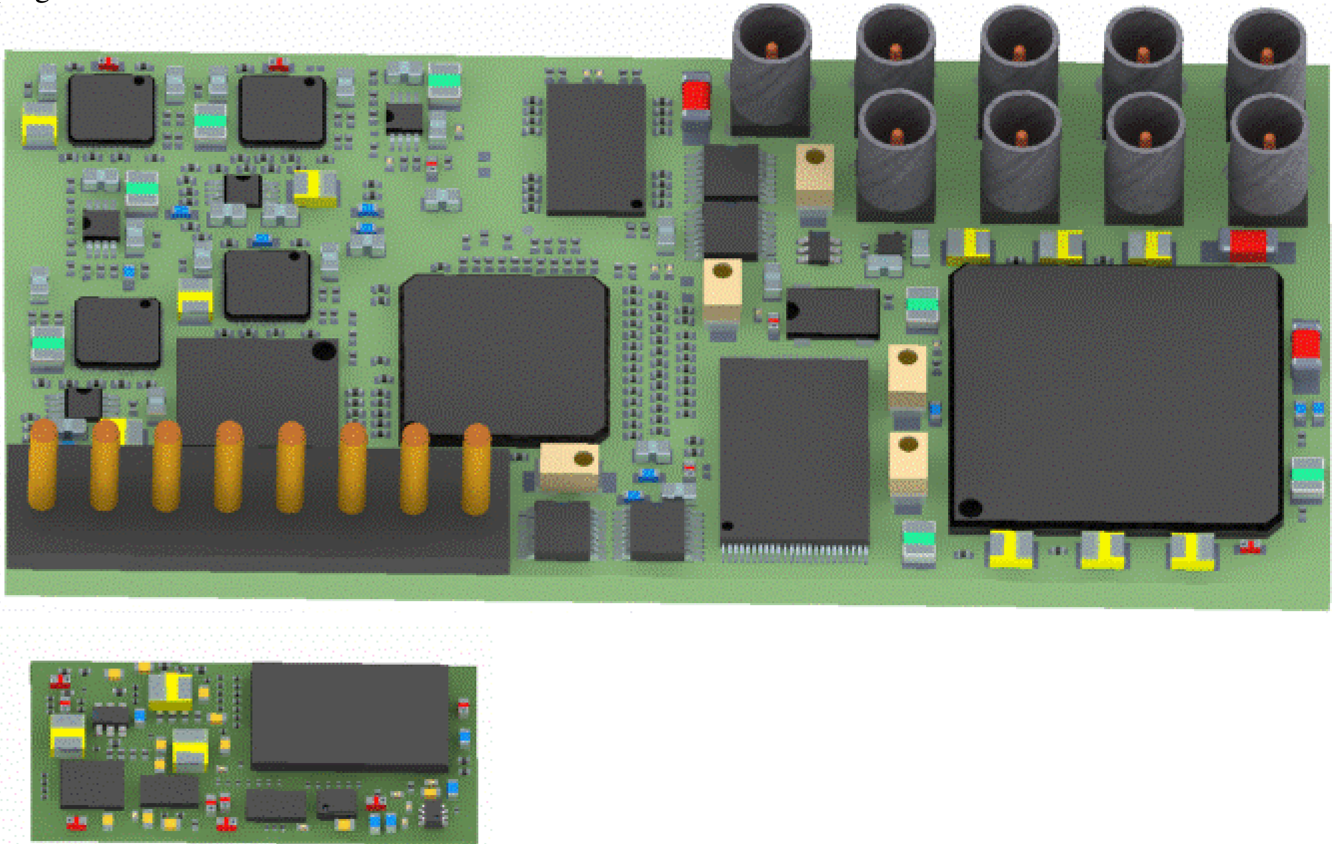

Figure 6: PWB vs SiP (26X area reduction)

The combination of the thin-core package and multilayer embedded capacitance core technologies lends itself well to single-chip and system-in-package applications, especially in situations where space constraints are critical and miniaturization is a requirement (**Figure 6**). The capability of embedded capacitance and the associated ability to reduce discrete component counts create significant additional miniaturization leverage.

References

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