# Manufacture and Characterization of a Novel Flip-Chip Package Z-interconnect Stack-up with RF Structures

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**Abstract**

More and more chip packages need multi-GHz RF structures to meet their performance targets. The ideal chip package needs to combine RF features with Digital features for these applications. They drive low-loss, controlled-impedance transmission lines, flexibility in assigned signal and power layers, and clearances of various shapes in power layers. Building these features in a chip package is difficult without making the stack-up very thick or compromising the reliability of the product. In the present paper, we have designed and built a flip-chip package test vehicle (TV) to make new RF structures, using Z-axis interconnection (Z-interconnect) building blocks. Specifically, large rectangular clearances were cut in multiple ground planes to make a very wide 50-ohm stripline. Also, typical 50-ohm stripline was designed with a ground-signal-ground structure. The stack-up had 16 metal layers, including 3 0S2P joining cores, 2 2S2P signals cores, plated copper on top and bottom and embedded resistance on layer 7. A variety of material sets including liquid crystal polymer (LCP), polytetrafluoroethylene (PTFE), allylated polyphenylene ether (APPE) were used for the dielectric layers associated with the signal layers. Several conducting adhesives formulated using silver and Low melting point (LMP) fillers were used to fill small diameter holes for Z-interconnect applications. Laminated conducting joints show low resistance in the range of 10-12 milliohm per square inch. Electrically, S-parameter measurements showed very low loss at multi-gigahertz frequencies. The losses were equivalent to typical transmission lines in ceramic. This effort is an integrated approach on three fronts: materials development and characterization; fabrication; and design and electrical characterization at package level.

## Introduction

Many new designs require multi-GHz signals, dense wiring due to high I/O count, and both wide lines for RF signals and narrower lines for digital signals [1-3]. With standard substrate stack-ups it is difficult to satisfy all those constraints at once. Most existing organic substrate technologies create via stubs which can only be avoided with restrictive design rules, and do not have the flexibility to build arbitrary transmission-line structures. A Z-axis interconnect technology (Z-interconnect) stack-up is developed to solidly satisfy all the constraints. Using Z-interconnect, via stubs can be eliminated and all of the RF flip-chip requirements can be satisfied [4-7]. Z-interconnect involves building mini-substrates of 2 or 3 layers each, then assembling several mini-substrates together to make the finished product. It is used to connect PCB metal layers vertically, using a conductive paste. Designing and manufacturing the mini-substrates separately makes it possible to reliably manufacture substrates with no via stubs, very low-loss materials, nearly arbitrary transmission line structures and a lot of flexibility in tuning features to reduce signal loss.

Currently there are a number of choices for a core plus build-up substrate that satisfy multi-gigabit data rates. [1, 5] The core plus build-up construction allows good performance and wireability in the build-up layers, but at a cost of less flexibility in the core layers. For instance, the core layers typically have a minimum via pitch, must be mostly a copper plane, and cannot have large clearances in them.

In the present paper, a new design is shown that uses Z-interconnect building blocks to make RF structures. New stack-ups are developed using LCP material, PTFE and APPE material in combination with embedded passive materials which achieve the main features that an RF flip-chip package needs:

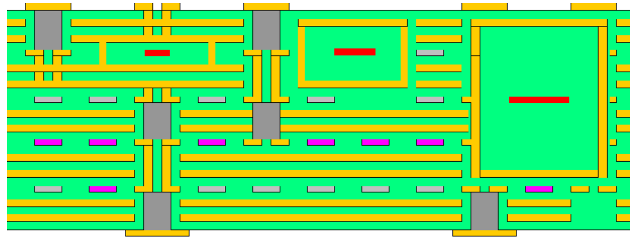
- Low-loss signal path
- Small, medium, large width, controlled-impedance lines
- Embedded passive components, discrete resistors and capacitors, plus capacitance layers
- Delay matching
- Islands in all plane layers, can be either power or ground
- Narrow lines for digital and low-frequency signals
- Arbitrary stack-up, symmetric or not, all layers have ground and signal regions
- Large, arbitrary-shaped clearances in planes
- Lightweight, thin

The work involved optimizing dielectric and conducting adhesive materials for the structures and includes embedded resistors. The various requirements lead to development in three main areas: (1) materials optimization; (2) fabrication, and (3) electrical performance at the package level.

## Z-interconnect construction

Electrically, in micro-chip packages, there is always a need for substrates that can handle a diverse range of signal types. Focusing resources, such as area on the substrate and expensive materials, where needed maximizes performance versus cost. The fastest RF signals get the widest lines and well-controlled impedance. The slower RF signals have narrower lines. Digital signals are just wide enough to carry their data and are squeezed as close as possible without violating crosstalk specifications. Low frequency interface

signals (MHz) are very narrow and fit in around the critical signals. Power and DC nets are put in last. A Z-interconnect stack-up gives a design engineer quite a bit of flexibility to place wide signals, narrow signals and grounds and clearances only where needed. [8] The result is sketched below.

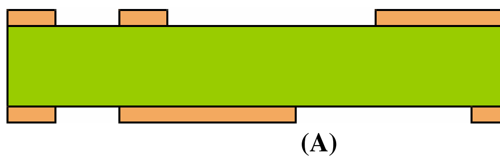


**Red = RF signals** **Purple = digital**

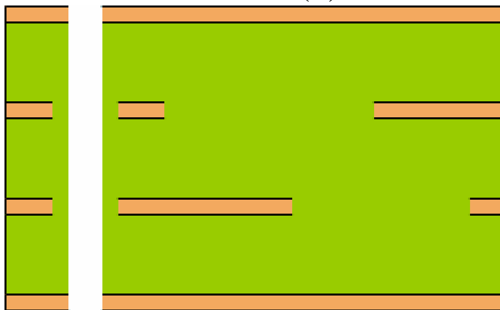
**Gray = all other signals**

**Figure 1 Versatile, Arbitrary stack-up**

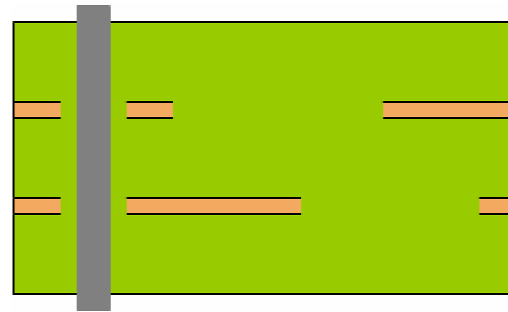
The methods used to build a Z-interconnect structure is with a series of building blocks called cores. The main building blocks are a plane-plane (0S2P) core and a signal-plane-plane-signal core (2S2P). The joining core is the name of the 0S2P because it has a conductive paste which allows it to attach to the 2S2P signal cores. The joining core starts with an off-the-shelf laminate with 2 layers of copper attached to a dielectric sheet. Then shapes and lines are etched into the copper on both sides. A layer of dielectric and copper is stuck to both sides of the etched plane-plane core. Holes are then drilled all the way through the structure. Lastly, the hole is filled with conductive paste and the outer copper is etched away, yielding a 0S2P joining core. These steps are sketched below.



**(A)**



**(B)**



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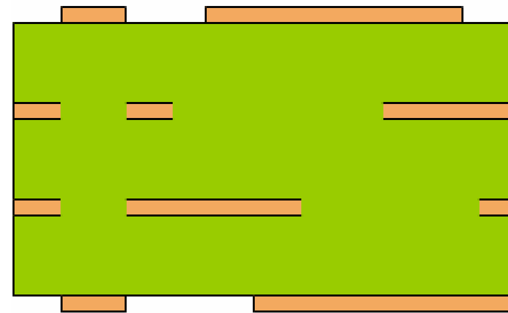

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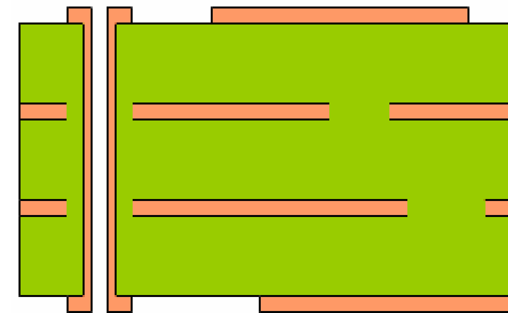


**(E)**

**Figure 2 :** Fabrication of joining and signal cores (A) Etch 2P core; (B) Drill laminated 2P core; (C) Paste fill drilled 2P core; (D) Etch laminated 2P core (E) Drill and plate laminated 2P core

The 2S2P signal core process starts the same as the 0S2P core, up to attaching the dielectric and metal layers to the 2P core. As the next step, instead of drilling, the outer copper is etched to create all the signal features. Lastly, the holes are drilled and plated to make the 2S2P core. The 0S2P and 2S2P cores are combined to make a Z-interconnect stack-up. **Figure 2** and **Figure 3** describes simplified diagram of Z-interconnects which includes 2P, joining cores, signal cores and their combined structures.

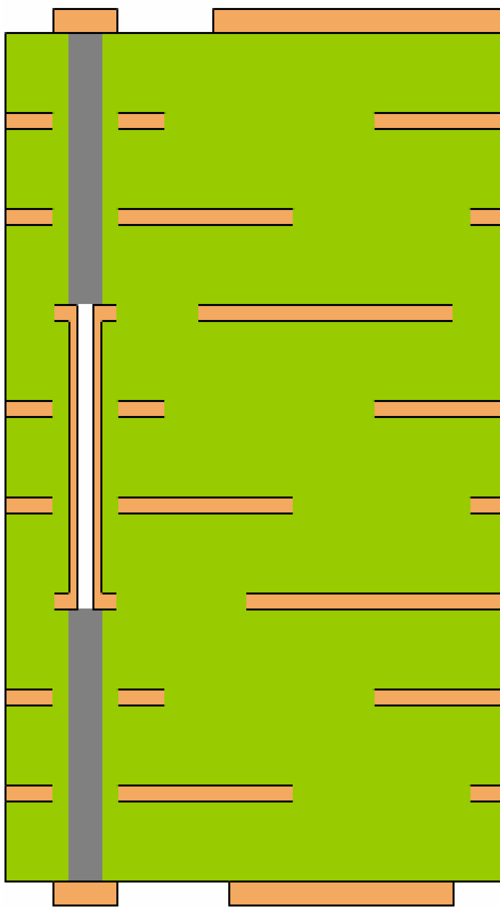


**Figure3: Z-interconnect composite stack-up**

In combination with blind and buried vias (see **Figure 4**), the signal and joining core building blocks allow arbitrary via connections starting at any layer and ending at any layer. In the 2P core, vias can be drilled and plated before the additional dielectric layers are added. Blind vias can be drilled on the outer layers of the 2S2P also. These one-layer micro-vias can be stacked to make arbitrary via connections.

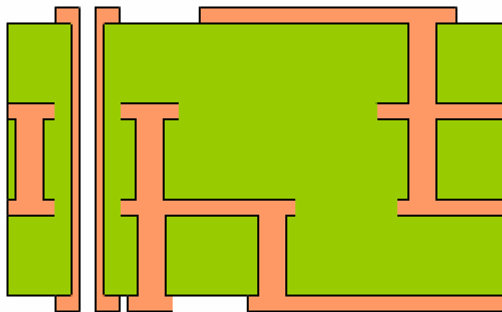


**Figure 4: Buried and blind vias in core**

In addition, embedded capacitance layers can be inserted in any 2P core of the stack-up. Discrete embedded capacitors and resistors can be added to most layers in the stack-up. Barium titanate–fluoropolymer can be used for embedded capacitance layers. Printable barium titanate nanocomposites or thick film resistors or resistor foil typically used for discrete embedded passives.

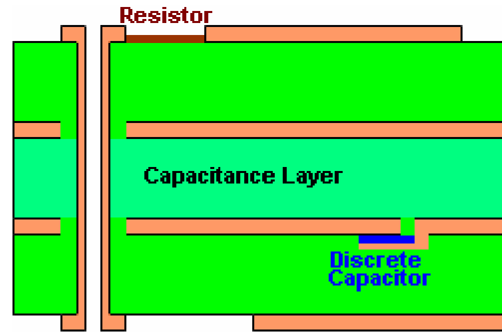



**Figure 5: Embedded capacitance layer and embedded discrete caps and resistors**

**Test Vehicle Design**

Test vehicles were designed to make new RF structures, using the Z-interconnect building blocks. Specifically, large rectangular clearances were cut in multiple ground planes to make a very wide 50-ohm stripline. Also, typical 50-ohm stripline was built with a ground-signal-ground structure. Each stack-up had 16 metal layers, including 3 0S2P joining cores, 2 2S2P signals cores, plated copper on top and bottom and embedded resistance on layer 7. Each dielectric layer was about 50um (2mils) thick. The stack-up used a mixed set of materials, using different materials or the plane-dielectric-plane structure and for the dielectric layers associated with the signal layers. (**Figure 6**) The total thickness of the stack-up was slightly less than 1mm. Dielectric 1 has Dk = 2.7 and tan$\delta$ = .003. Dielectric 2 has Dk = 3.2 and tan$\delta$ = .003. This made the manufacturing process a little simpler by customizing the dielectric material to the particular process where it will be used[8].

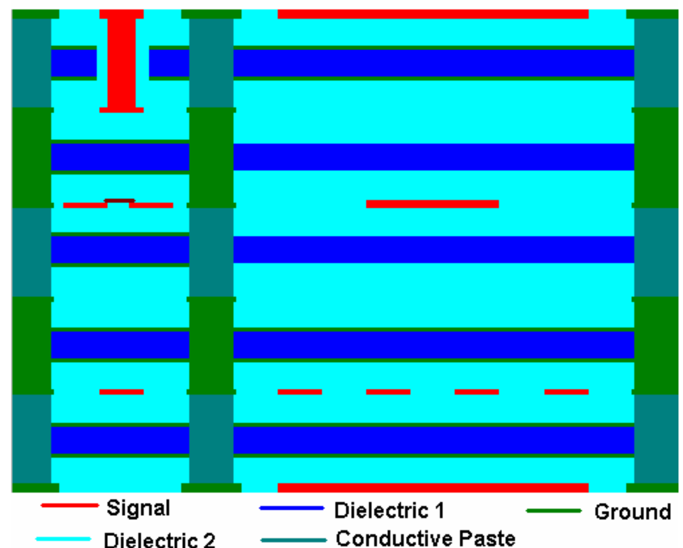



**Figure 6: Mixed dielectric stack-up**

Electrically, this type of stack-up allows a well-controlled, low-loss wide 50-ohm RF line. In the test vehicle the widest line width was roughly 270um, with the smallest at 48um. This new construction allows both transmission lines to fit in a

stack-up less than 1mm thick. With the 48um line at 30mm long, the estimated 3dB bandwidth of a link with vias and pads is about 25GHz, and is nearly transparent (-0.5dB) to 2GHz. Using a 270um line instead, the 3dB point extends beyond 50GHz and is nearly transparent to 10GHz.

The basic structure of the proposed test vehicle is shown in **Figure 7**. The test vehicle includes a flip-chip pad array and is compatible with flip-chip processes. The materials and processes used to manufacture the Z-interconnect substrate will work with flip-chip attach assembly steps.

**Figure 7: Snapshot of Test Vehicle Design**

### Composite Lamination

Alternating the joining and signal cores in the lay-up prior to lamination, allows the conductive paste to electrically connect copper pads on the 2S/2P cores that reside on either side of the 0S/2P core. A structure with four signal layers composed of five sub-composites (two 2S/2P cores and three 0S/2P cores) is shown schematically in **Figure 8**. Although this particular construction comprises alternating 2S/2P and 0S/2P cores, it is also possible to place multiple 0S/2P cores adjacent to each other in the stack.

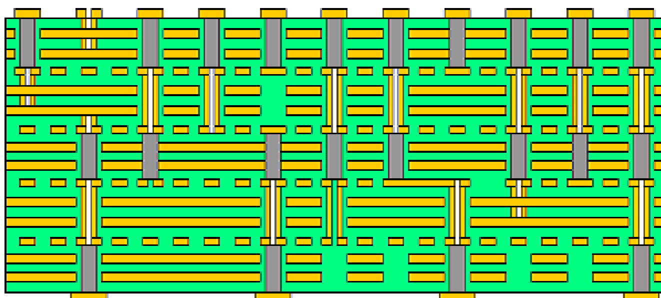


**Figure 8: Sixteen-layer Z-interconnect composite**

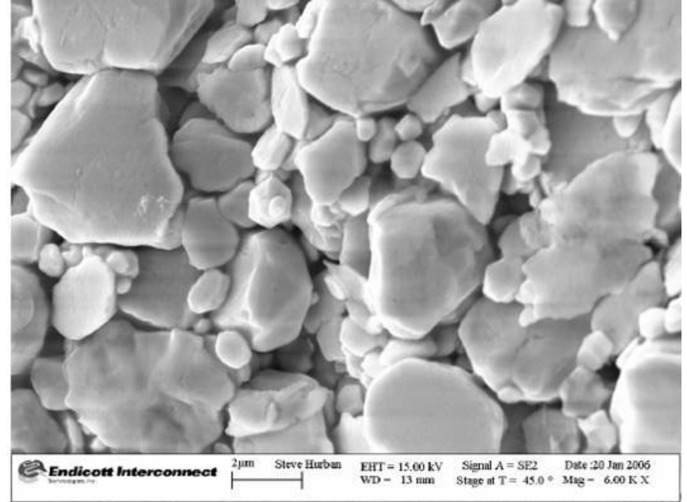



**Figure 9: SEM micrographs conductive adhesive with nano and micro particles**

### Results and Discussion

The formation of a conduction path was observed by SEM images. **Figure 9** shows a SEM image of nano-micro filled conductive adhesive as a typical representative example. In the silver adhesive, the average filler diameter is in the range of 5 µm. Filler loading was high and adjacent particles united mutually, and necking phenomena between fillers occurred; namely, a conduction path was achieved, as shown in **Figure 9**. A variety of silver filled adhesives with a mixture of nano and micro particles were studied. In nano-micro mixtures, nano particles occupy interstitial positions to improve particle-particle contact for conductivity. For the silver nano particles (~80 nm size), the fillers can self sinter and make a continuous conduction path. Because of the high surface area of silver nanoparticles, an excess amount of solvent is required to make a high loading silver paste.

The adhesive-filled joining cores were laminated with circuitized sub-composites to produce a composite structure. **Figures 2-3** show a process flow chart for fabrication of adhesive filled 0S/2P cores. High temperature/pressure lamination was used to cure the adhesive in the composite and provide Z-interconnection among the circuitized sub-composites.Reliable metal-epoxy adhesives were used for hole fill applications to fabricate Z-axis interconnections in laminates.

A Z-interconnect substrate, with large clearances in planes was built successfully. The conductive paste connects subcomposites and forms an electrical and mechanical path.

**Figure 10** show silver adhesive-filled joining cores as representative examples. Holes having a diameter of roughly 65 um, with an aspect ratio of about 3 to 1, were filled with different pastes. All pastes had continuous connection from top to bottom.

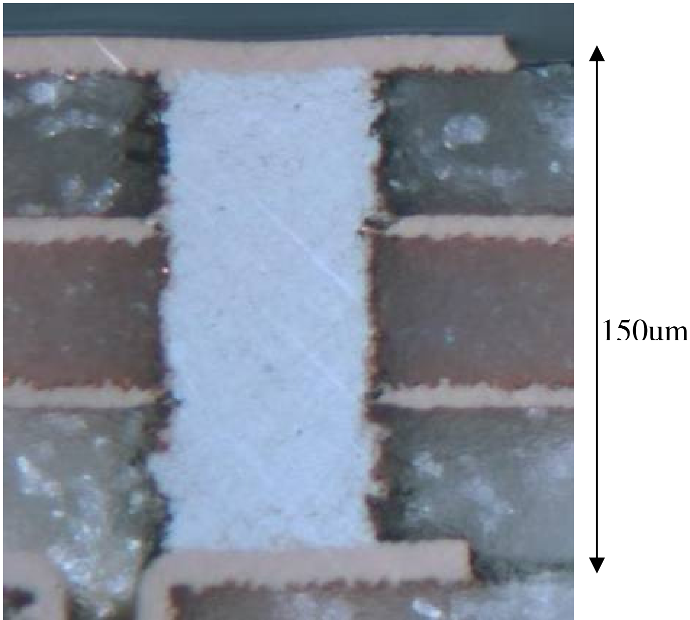
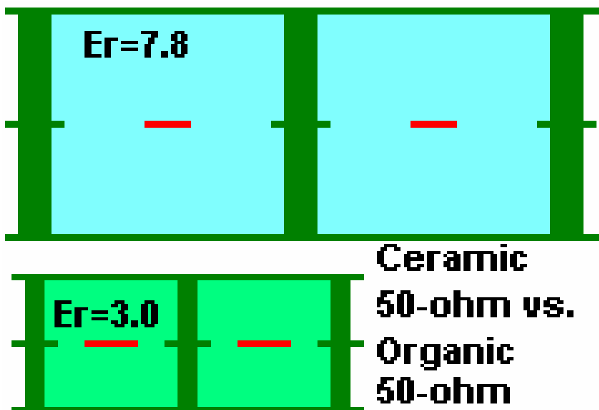
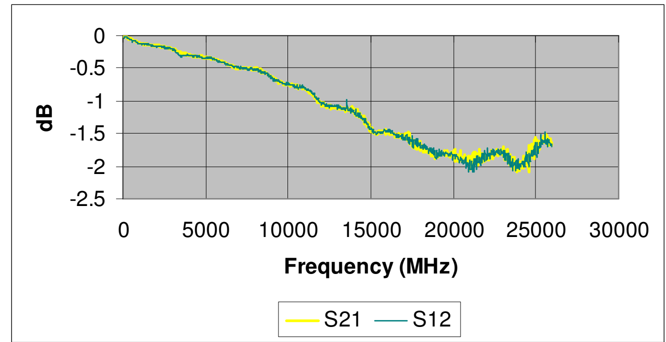



**Figure1 0:** Cross-section of Conductive Paste Connection in the Test Vehicle

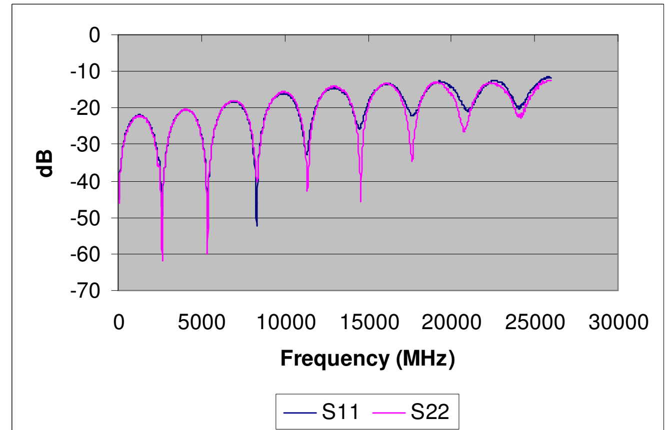
**Figure 11 (A)** shows the stripline configuration and **Figure 11 (B-E)** shows the experimental results. Electrically, S-parameter measurements showed very low loss at multi-gigahertz frequencies. The measured return loss and insertion loss for both shallow and deep stripline are similar. In both cases, return loss is lower than -10dB and insertion loss at 10GHz around -2dB and -4dB with deep and shallow stripline respectively. The losses were equivalent to typical transmission lines in ceramic. The Z-interconnect stack-up and low dielectric constant organic dielectric allowed wide, 50-ohm, lines. Low-loss striplines, in organic, take up a lot less space and are lighter than similar ones in ceramic.



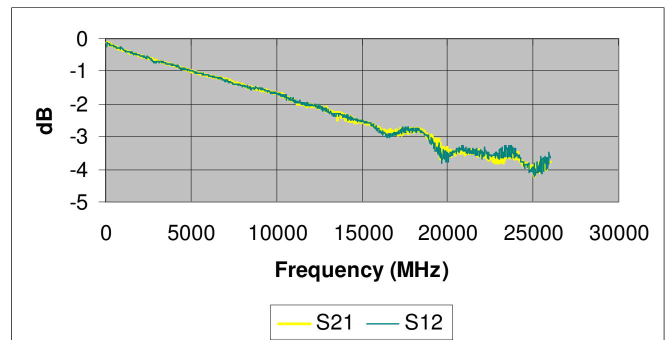

**(A) Designed configuration**



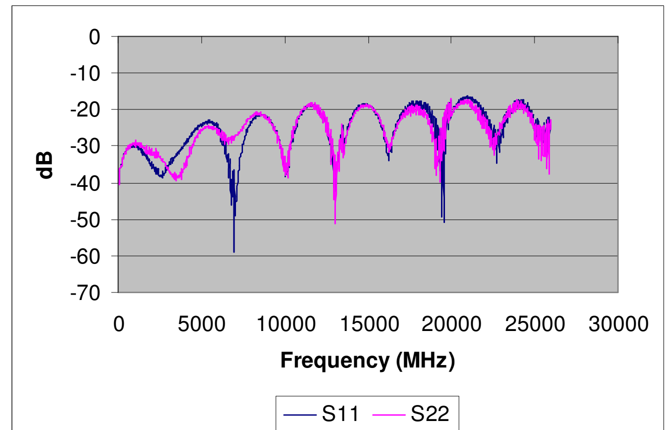

**(B) Deep Stripline (270um) Insertion Loss**




**(C ) Deep Stripline (270um) Return Loss**



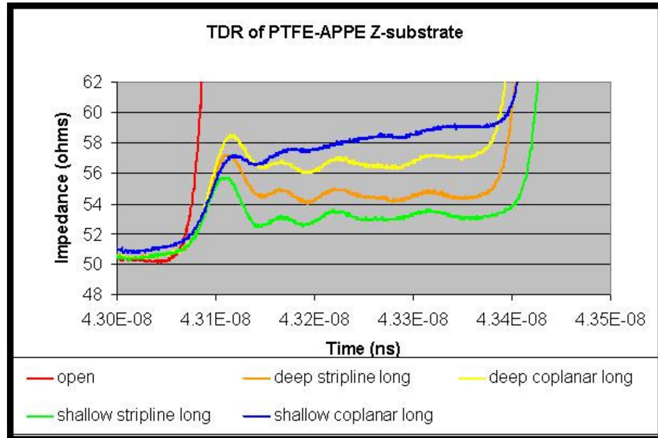

**(D) Shallow Stripline (48um) Insertion Loss**



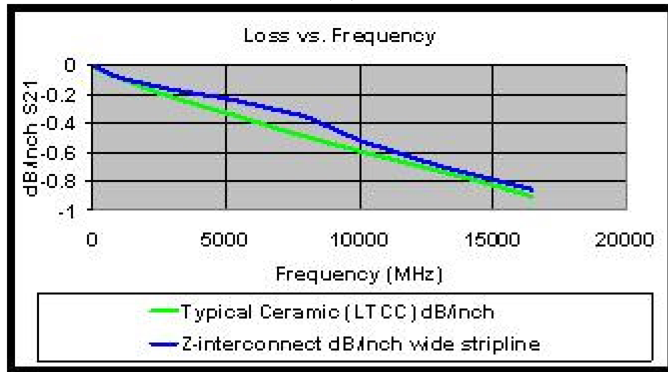

**(E) Shallow Stripline (48um) Return Loss**

**Figure 11**: Test results with stripline **(A)** design configuration, **(B)-(E)** Measured results

Below is a TDR (Time-Domain Reflectometry) plot (**Figure 12A**), showing the impedance measured along the transmission lines. The impedance measured a little higher than the 50-ohm target because dielectric thicknesses were a little bigger than predicted. On subsequent builds, reflections should get smaller and return loss should improve as the line width is fine-tuned to hit the 50-ohm target more accurately. Also below is a plot of insertion loss **(Figure12 B).** Overall the dB/inch of the Z-interconnect compares favorably with low temperature co-fired ceramic (LTCC).




**(A)**




**(B)**

**Figure 12:** (**A**) TDR Plot, and (**B**) Insertion Loss dB/inch of Stripline in Organic vs. Ceramic Dielectric

## Conclusions

A Z-interconnect substrate, with large clearances in planes and embedded resistors, can be built with sufficient flatness on subsequent metal layers. Using 0S2P and 2S2P building blocks, a nearly arbitrary stack-up of signals and planes can be built. This allows very low-loss 50-ohm stripline to be built by making nearly 300um-wide lines and clearing out ground planes to make a 50-ohm structure. This also allows narrower 50-ohm lines and narrow digital lines and DC structures to be built on the same layers as the wide lines. A high-performance, mixed signal design can be built in a substrate less than 1mm thick. In addition, the electrical performance is outstanding, since the wide lines are nearly transparent to signals up to 10GHz. Very low-loss RF, controlled-impedance transmission lines can be built using Z-interconnect in organic dielectric. In fact, the losses are at least as good as ceramic dielectrics, and the stack-up is lighter and more compact than using ceramic dielectrics.

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