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Package-on-Package (PoP) for Advanced PCB Manufacturing Process

By Joseph Y. Lee, Jinyong Ahn, JeGwang Yoo, and Shuichi Okabe

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Abstract:

In the 1990's, both BGA (Ball Grid Array) and CSP (Chip Size Package) are entering their end in the front-end packaging materials and process technology. Both BGA and CSP like SMD (Surface Mount Device) from the 1980's and THD (Through-Hole mount Device) from the 1970's are reaching its own impasse in terms of maximizing its electrical, mechanical, and thermal performances, size, weight, and reliability. Now, 3D packages are the next phase for its future use in advanced PCB manufacturing process. They can be classified into wafer level, chip level, and package level stacking. So, package-on-package (PoP), a type of 3D package level stacking, is to be discussed in this paper. [16]

Index terms:

3D packaging, package-in-package (PiP), package-on-package (PoP), stacked packaging, folded packages, 3D-chip-stacked-packaging (3D-CSP)

I. INTRODUCTION

The purpose for 3-D packaging is to have more functional integration in small and thin packages, to lower cost, to design with flexibility, to establish supply chain, to shorten time-to-market product, to increase reliability, to provide RoHS compatiability, to improve its electrical properties, and to have compelling advantages with low risk.

Despite the advantages, one of the challenges for 3-D packaging is to put mechanically more die in a thinner package or to put mechanically more packages into one single package. PoP is placing a stronger emphasis on more packages into a single package. There are other tradeoffs. For example, wafer thinning and sawing is required to reduce die thickness for 3D PoP packages. Wafer warpage is a serious issue for wafer thinning and sawing. Also, die attach materials and spacer technology are required for proper wire bonding between the top and bottom dies. This increases thickness of 3D packages and increases the length of wire bonds, which decreases the speed in terms of its electrical properties. Wire bonding has difficulties in terms of low loop wire bond, overhang, multi-row, and fine bond finger pitch.

Besides the wire bonding difficulties, thin mold for top center mold gate is needed for thin 3D PoP packages. Another hurdle like low-k material is needed to avoid parasitic capacitance, which slows the electrical performance for the entire package. Right now, major dielectric enabling technology materials can be found in non-polymer types like diamond and coral and polymer types like SiLK. Challenges for assembling with CUP (Circuit Under Pad) and dielectrics are chipping, chip interlayer delamination, pad peeling and collapse at wire bonding, electrical function shift due to packaging stress, and ILD delamination with thermal stress cycles. Thin and dense substrates with fine pitch ball attach is a difficulty in terms of wafer thinning, thinner molds, thin spacers, and low loop wire bonding. Module design, modeling, and performance testing require new computer simulations to determine the thermal, electrical, mechanical properties and design of new novel 3D packages for PoP.

Integrating 3D PoP packages for PCB technology stretches the performance envelope of all assembly processes, materials, simulations, and equipment. The drive towards stacked packages like PoP instead of stacked-die packages is determined by its final test cost and complexity in terms of manufacturing processes, simulations, reliability, and performance. [8]

II. DISCUSSION AND RESULTS

Valtronic

Valtronic has a claim on their Gold Stub Bumps with a Non-Conductive Paste (NCP), and it does not require additional preparation of the pads such as under bumps metallization before bumping. Reliability is excellent in terms of thermal and humidity.

Flip-Chip has its advantages in terms of smaller size, lower contact resistance and impedance, and lower costs with high i/o counts. Flip-chip technology is mainly driven by bumping technique and type of substrate. The characteristics of FC are:

1) low contact resistance gold to gold
2) low contact impedance compared to wire bonding
3) compatible with reflow process
4) compatible with organic substrates, including flex ones
5) reduced assembly operations count
6) compatible with production up to 1 million dice a year
7) excellent reliability.

New FC process allow assembly of dice with a smaller pitch of 120μm. Valtronic has some recommendations for FC process. For example, bonding pressure is critical for FC process, and it depends on the number of bondpads. Recommended parameters for bumping are:

1) 50 to 80g of pressure/bump
2) 150-250°C temperature
3) 10s adhesive cure time
4) +/- 5μm alignment
5) +/- 5μm planarity [1]

Benefits from the FC process are:

1) die bumping requires no UBM
2) no underfill operation
3) complete electronic function integrated into same package because SMT component implementation is possible
4) very good resistance to thermal shock
5) fast signal speed
6) die can be functionally tested [1]

Reliability is determined in temperatures around 85°C at 85% relative humidity. Excellent reliability has been

demonstrated by Valtronic's process.

PiP vs. PoP

The difference between PiP (Package-in-Package) and PoP (Package-on-Package) can be a little confusing. It is possible that both PiP and PoP are the same. According to STATSChipPac, they show their PoP such that two flip-chip packages are bonded together while they show their PiP such that two packages wire-bonded together as one flip-chip package. The slight difference can be seen in Figures 1 and 2. [8]

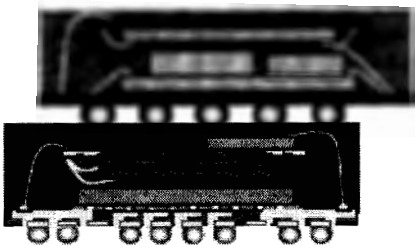

Figure 1. Package-in-package [4]

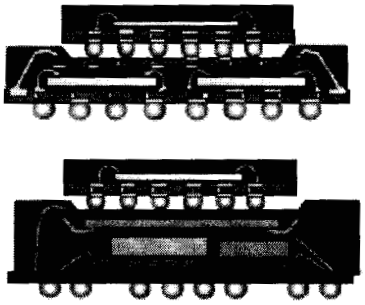

Figure 2. Package-on-package [4]

According to Fylnn Carson *et al.* at ChipPAC, they believe that a packaged and tested device can cost less than a Known Good Die (KGD). Not only KGD has high cost, but it also has limited availability and supplier base. On the other hand, a good package has low cost with less supply issues than a KGD.

Instead of stacking die themselves, very thin Land Grid Array (LGA) type packages enclosing one or more dies can be stacked as if it is one die. Figure 3 is almost identical to Figure 1. Figure 3 is basically a PiP such that the bottom die in the package stacked is assembled and encapsulated while a thin tested LGA package is stacked on top of the base package, wire bonded, and finally encapsulated like a conventional stacked die package.

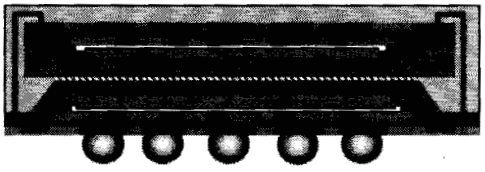

Figure 3. PiP with Single Die LGA (ChipPAC, Inc.) [4]

The key advantage for PiP is that LGA can be fully tested before it is integrated into one PiP package. ChipPAC claims that they have met the Lead-free moisture sensitivity and reliability levels. In Fig. 4, ChipPAC also designed a more robust PiP with two dies separated by one spacer within the LGA.

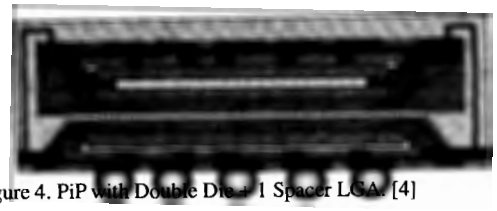

Figure 4. PiP with Double Die + 1 Spacer LGA [4]

In Figure 4, the maximum package height is at 1.6mm while in Figure 3, the maximum package height is at 1.4mm. The dimensions for the PiP test vehicle are shown in Figure 5.

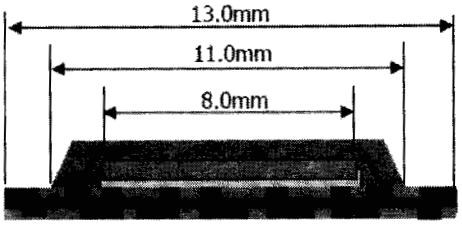

Figure 5. Test Vehicle Base Package [4]

This 13x13mm 341 ball package has a 0.5mm solder ball pitch and is in mass production with Lead-free solder balls. The die thickness is at 0.075mm. Not only thin dies are required for this process, but also very thin substrate, mold cap, and low loop height has to be integrated for this PiP structure. At a 0.125mm bond finger pitch, 280 wire bonds can be fitted on the bottom die. Besides the test vehicle package, the LGA uses a 8x10mm test vehicle with 88 lead array. A 5x6mm size die is used within the LGA package.

It is forecasted that the next generation packaging technology requires a thickness of 1.4mm. However, a 1.2mm maximum thickness restraint is going to be no surprise in the near future. Wafer thinning, ultra low wire bonding, very thin laminate substrate, encapsulant molding technology and materials need to occur. [4]

Underfill vs. No Underfill

Samsung Electronics shows that there are tradeoffs between the underfill and the no-underfill for PoP technology. While the underfill improves the reliability, the no-underfill improves the thermal shock for PoP's. Good PoP processability for the underfill requires wetting, low viscosity, and reworkability while good PoP reliability involves low CTE and high T_g. As shown in Figure 6, it basically consists of two flip chips one on top of the other. The top package for the PoP is the memory MCP while the bottom package for the PoP is a baseband, application processor. [9]

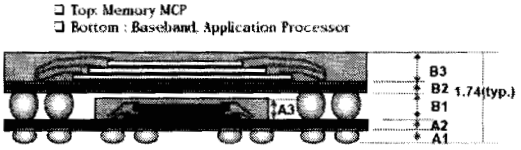

Figure 6. PoP from Samsung Electronics. [9]

Cu Column

Figure 7 shows two packages stacked on top of each other. This PoP is known as the Matrix Molded Array Package (MMAP). The top package is a multi-chip that stacks flash and RAM memories. The bottom package is single chip package. It is basically a logic chip. Intel claims that they can achieve three packages stacking. The advantage for this process is that each individual package

can be tested as a Ball Grid Array (BGA).

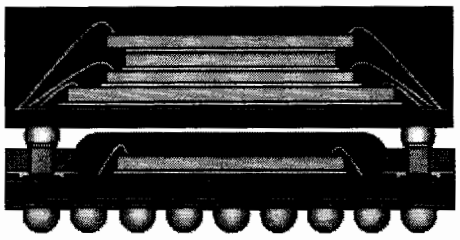

Figure 7. Cross sectional schematic of SP-CSP [11]

They propose a copper column to reduce the size of pitch to 0.33mm with a total of 160 interconnects with a single row peripheral pad, as shown from Figures 8 to 10. They have also claimed that 330 interconnects with a dual rows in a 14x14mm packaged can be accomplished. The copper columns consist of a glass woven resin core substrate. Then, they are laminated on the bottom package substrate by a vacuumed hot press. [11]

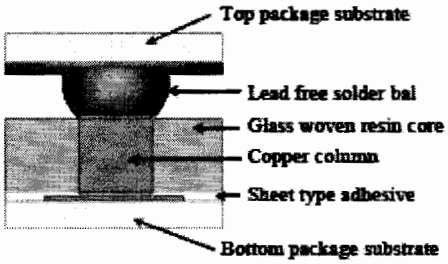

Figure 8. Schematic diagram of solder ball, reflow bonding structure with a copper column implanted interposer. [11]

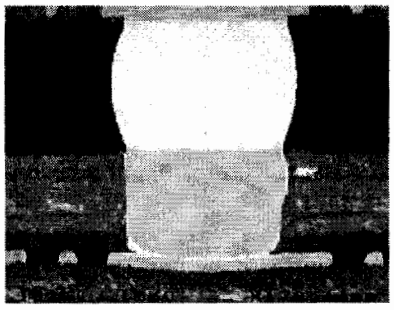

Figure 9. SEM photo of solder ball reflow bonding using a copper column implanted interpose. [11]

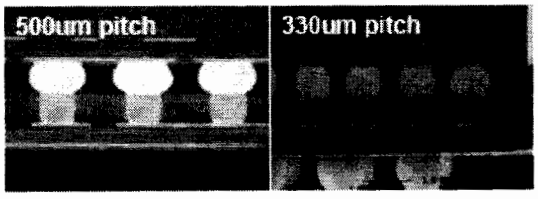

Figure 10. Cross sectional SEM image of PoP interconnections. [11]

Reliability for Cu Column

Intel claims that they are able to have excellent reliability even in the absence of a underfill material. Both BGA and PoP structures show resilient solder joint reliability. Electrical failures are not detected even though sample size may not be enough for a final conclusion.

Table 1: Unit-level reliability testing [11]

Stress	Results
MSL3 Preconditioning (7 hrs bake@125°C, 5x T/C 'B', 216hrs 30°C/60%RH + 3x CR @ peak temp of 260°C)	0 / 30 unit fail
MSL3 + T/C 'B' 1000 cycles (-55°C to 125°C)	0 / 20 unit fail
MSL3 + Biased HAST 100 hrs (130°C/85%RH, +3.3V)	0 / 10 unit fail
Bake @ 150°C, 500 hours	0 / 10 unit fail

Table 2: Second-level board reliability testing [11]

Stress	Results
T/C 'G' 2500 cycles (-40°C to 125°C)	0 / 30 unit fail
Drop 250 drops (1500G/0.5ms/half sine pulse , Z-axis)	0 / 27 unit fail
3 point Board Bend (5 & 6.5mm displacement, 1.25Hz)	>100K cycles at 0.001 strain

Reliability tests cover thermo-mechanical stress, moisture stress and ion migration, high temperature storage, and signal integrity. All indicates excellent reliability even after 1000 'B' condition temperature cycles. Package to package interconnections show no leakage current at 3.3V. [11]

Folded Stacked Packages – Type of PoP

Young Gon Kim at Tessera Technologies claims that he can develop a process to stack four memory dies at a height of 1.2mm. Since μBGA package has high reliability, minimizing any interaction folding among individual dies is needed to ensure high reliability for the folded stacked packages. A 140μm ball height and compatible test socket contact mechanism are used to minimize overall package height.

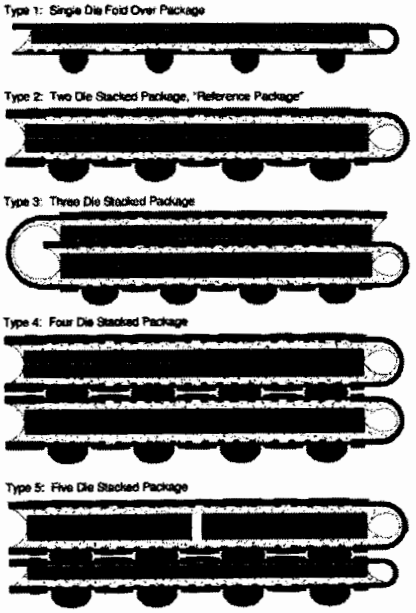

Figure 11. Folded stacked package variation [14]

As shown in Figure 11, type 1 is a single-die fold over package. This is used for high voltage applications such as power IC of medical products. 0.5mm package height can

be achieved as well. Type 2 is a two-die stacked package. This unit is not easy to repair compared to the single-die stacked. So, it is required that they use KGD with dies of high yield. Type 3 is a three-die stacked package. KGD is almost a must for this process. A 1.0mm height can be achieved for this process with two flash dies and one SRAM die. Type 4 is a four-stacked die package.

Combining two reference packages with LGA joints may be a more cost effective solution. The small LGA height is at 50μm, and the 1.2mm package height can be achieved. Type 5 is probably under development. It is a five-stacked die package with a 1.2mm package height. It consists of controller chip and four-memory dies. [14]

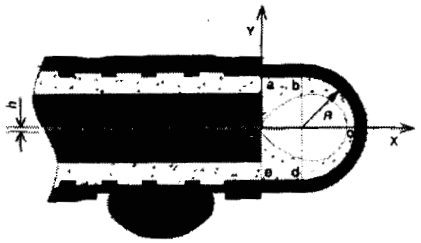

Figure 12. Die-to-die distance design rule derivation and recommended amount of encapsulant in the folded area. [14]

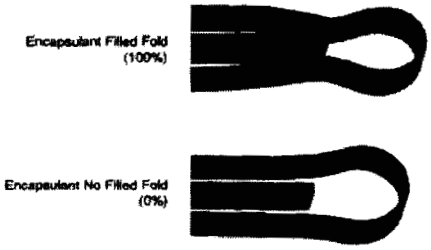

Figure 13. The effect of encapsulant at folding area. [14]

In Figure 12, there is no encapsulant in the bubble area. It is very important to take note. If the folded die-stacked is filled with the encapsulant, then folded area deforms as shown in the top schematic of Figure 13. Y.G. Kim rationalizes the cause of the deformation due to its high CTE and Poisson's ratio. Since the folded area is confined in a small area, the tape is pulled or pushed significantly causing the deformation. It is Y.G. Kim's recommendation that the fold be coated rather than left completely empty. This recommendation can be seen from Figure 12. An optimal elastomer height is an important consideration to reduce stress deformation at the folded area. It is recommended to have 114μm elastomer height for 8x8mm die for high reliability. Other values differ for the size of die.

Curing condition for the adhesives is another important parameter for the folded stacked package process. A 30 second curing time at a temperature of 170°C is recommended for consideration. The author does not give all of the details on the exact composition of the adhesives. Material strength and short curing time have to be considered for the best adhesive for the folded stack die packages.

Thermal performance is extremely critical for die packages for folded stack packages, which is another form for a PoP. The type 4 package can dissipate about 1.9 watts of power under room temperature assuming a 115°C maximum allowed junction temperature. 96% of the heat is dissipated through the board. To improve the thermal performance, Kim recommends by putting the high power device at the bottom of the package. Thermal resistance of the package has been reduced from 47°C/Watt to 34°C/Watt.

S. Krishnan *et al.* from Tessera Technologies design a heat spreader attached on top of the package using a thermally conductive silver filled epoxy. The silver epoxy is then soldered to the test board.

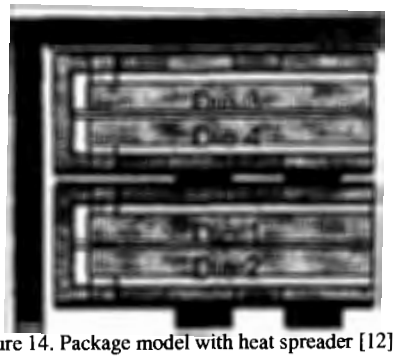

Figure 14. Package model with heat spreader [12]

55% of the heat goes through the heat spreader while the rest goes through test board through the package. The results can be seen on Figure 15. [12]

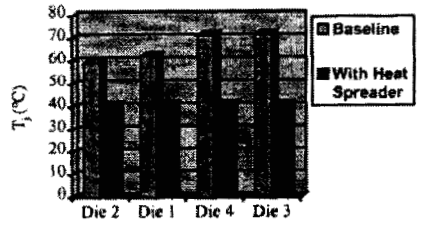

Figure 15. Heat spreader effect (equal power distribution) [12]

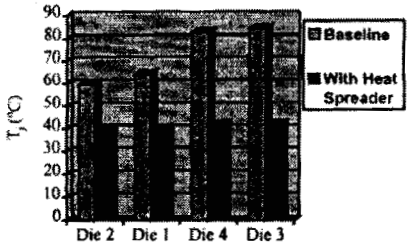

Figure 16. Heat spreader effect (top die powered) [12]

When the top die is being powered up and the rest of the dies are left passive, 70% of the heat is dissipated by the heat spreader. [12]

3D Packaging for High performance Memory Applications

Illyas *et al.* at Tessera also work on 3D packages for high performance memory application. Even though TSOP (Thin Small Outline Package) has served well for SDRAM and DDR SDRAM, it is forecasted that TSOP will not meet performance requirements for DDRII. Industry is already implementing CSP technology for RDRAM and DDR SDRAM memory.

At Tessera, they are able to achieve an overall thickness of 2.0mm (top figure) and 2.3mm (bottom figure) respectively as shown in Figure 17.

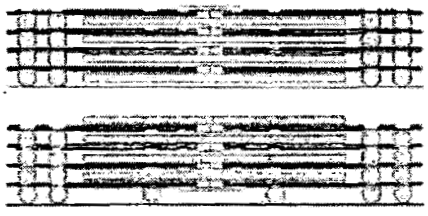

Figure 17. Two configuration of a 4-die μZ ball stack package [2]

It seems that Figure 17 is a type of PoP or 3D stacked package. There seems to be no wire bonding. Flip chip technology seems to be used. In the one die case, the

electrical performance for 3D-CSP is claimed to be superior to the electrical performance for TSOP or TQFP. The 512 Mb DDR SDRAM operating at a frequency of 167 MHz and 333 MHz data rate is used as a benchmark for comparison. Thus, when the maximum inductances and capacitances are considered, FBGA's delay at 30.2ps offers better performance than TSOP's delay at 80.5ps. Single and two-stack packages have similar maximum delay while the 4-stack package has a maximum delay of 75.5ps, superior to TSOP packages.

Thermal performance is always an issue in this case. Air velocity of 1m/s seems to optimize best thermal heat reduction for a 4 layer JEDEC standard board with 20% Cu on the surface. The total power dissipated is around 1W. At 0m/s airflow, the package thermal resistance Θ_{ja} is 20°C/W while at 1m/s airflow it is 11.2°C/W. So, airflow plays an important role cooling a PoP package for high performance memory applications.

Teressa has one comment about bringing the I/O to the periphery of the die and stacking them by using solder balls as electrical connections. Teressa has confidence that a 2 stacked process has adequate thermal performance. [2]

Chip in Polymer Technology

There are different embedding technologies for the packaging chips. For example, there is ceramic substrate with cavities for the chips while another integrates the chips into cavities of an organic PCB.

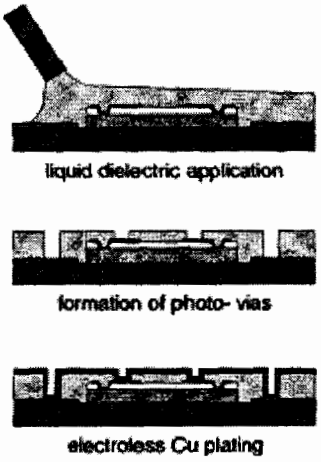

Figure 18. Two concepts or the realization of Chip in Polymer: (a) chip embedding by a liquid dielectric. [15]

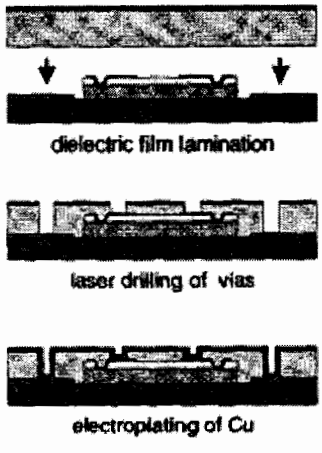

Figure 18. Two concepts or the realization of Chip in Polymer (b) embedding by lamination into a RCC layer [15]

A. Ostmann *et al.* proposes a very novel idea called chip in polymer (CIP) technology. The chips are about 50μm thick into build-up layers. Lamination substrates like FR4, liquid epoxy, or RCC (resin-coated copper) film are used. Schematic diagrams in Figure 18 are shown for the CIP process.

In Figure 19, test chips have thickness of 60μm. They have a size of 10x10mm with 120 I/O's. Al bondpads have a pitch of 300μm and are covered by electrolessly deposited 5μm of Ni and 2μm of Cu. 0.5mm thick FR4 board is required for this process. It is considered to be relatively too thick. It is proposed a thinner FR4 board needs to be developed. [15]

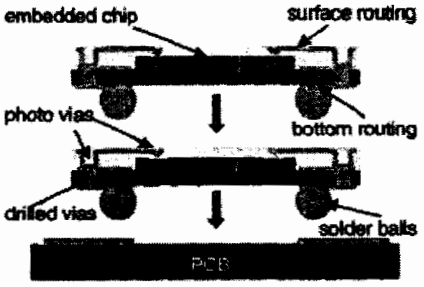

Figure 19. Concept of stacked packages or PoP [15]

Sharp's 3D Stacked Process

Even though Sharp called their 3D stacked package as a SiP, it can be considered as a PoP. It has its advantages when there are no yield problems. It is also easy to perform independent electrical testing, and it is possible to achieve multi-level stacking while freely combining different kinds of LSI chips like memory or ASIC.

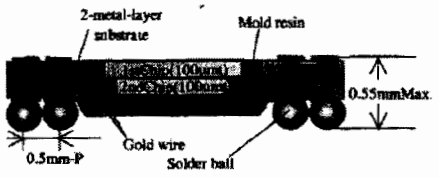

Figure 20. Cross-sectional structure of 2-chip type Ultra-thin CSP. [13]

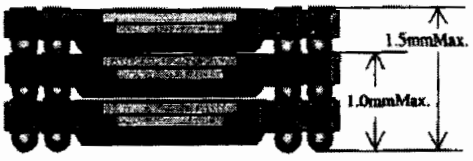

Figure 21. Cross-sectional structure of 3-layer stack (PoP) [13]

Figure 20 is a double die stacked package. Both chips are somehow wire bonded together. Sharp is able to achieve 0.55mmMax thick single package stack with 2 chips, a 1.0mmMax thick 2 layer package stack with 4 chips, and 1.5mmMax thick 3 layer package stack with 6 chips.

Items	Conditions	Result
Popcorn Test	(30C70%Rh×120h →260CMax.Reflow)×2times	0/13
HT/HH Bias	85C 85% R.H.×1000h (Flash=3.6V,SRAM=3.6V)	0/45
Temp.Cycle	(-65C/30min.~150C/30min.) ×300cyc.	0/43
PCT	110C85%Rh1.2atm×300h	0/22

Table 3. Package-level reliability results

Sharp has claimed that they have reduced an the mounting area by 30-60% compared to conventional CSP

or stacked CSP. They also claimed excellent reliability as shown in Table 3. The device is 16M flash with 8M SRAM memories. It has package size of 11x15mm.

Tampere University of Technology

The required steps for this PoP process are wafer or die thinning, inserting thin interposer, and stacking components. Seppo K. Pienimaa *et al.* from Tampere University of Technology claim a 40 to 50 times reduction in size and weight for 3D PoP packaging compared to conventional packaging. [5]

Again, they reiterate what other engineers say about 3D packaging from their papers. They are:

1) thermal management is a difficulty
2) flip chip offers superior features
3) interconnections are done on the periphery or area

However, Pienimaa *et al.* has a different claim on the best interconnection methods. They claim area interconnections provide the most accessible and usability. So, Piennmaa *et al.* use a totally different area interconnection process compared to Illyas Mohammed *et al.*'s peripheral interconnection process from Tessera. Pienimaa *et al.* argues that peripheral interconnections require the dimensions of the layers to be the same while area interconnections provide the possibility to stack and interconnect modules as array and singulate them as the last step of the manufacturing flow. However, area interconnections require high yield for each package or die or else it may result high cost for the process. [5]

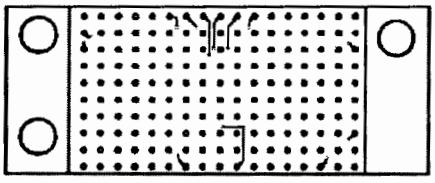

Figure 22. BGA matrix of the stacked structure (bottom) [5]

Each layer consists of 2 dice, 4.87x4.87mm^2. The size of the package is 8x14mm with a 0.8 thickness. Three layer stack has a 127% efficiency in terms of area. Even though the author classifies the stacked package as a SiP, it can be considered as a PoP.

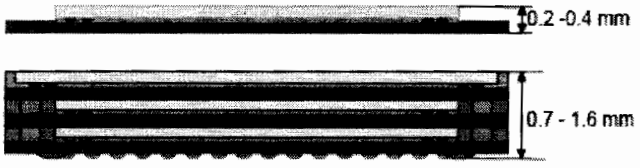

Figure 23 Schematic diagram of a stacked package. [3, 5]

Their solder process is not a lead-less process. They use a 62%Sn 36%Pb 2%Ag solder process. Underfill is used in this process to diminish maximum stress by spreading the stress more equally. [5]

Jarmo *et al.* from Tampere University of Technology uses a daisy chain to test reliability. They use some alignment markers consisting of a square, circle, and another square cut diagonally. Position of chip has to be in the range of +/- 5μm. [3]

J. Miettinen *et al.* also from Tampere University of Technology uses solder-plated polymer balls with a polymer core of 230μm and a Cu layer of 2.0μm coated with a solder layer of 8.0μm. Solder material consist of 63%Sn 37%Pb or 96.5%Sn 3.5%Ag. They claim that solder-plated polymer balls have excellent reliability and do not collapse under pressure. High yield KGD is required for this process still. [6]

Roadmap

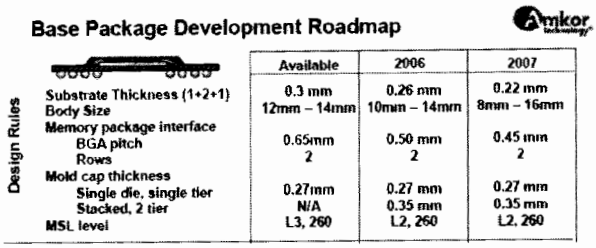

Figure #. Roadmap provided by Amkor Technology. [7]

Amkor Technology forecasts a substrate thickness of 0.26mm in 2006 and a substrate thickness of 0.22mm in 2007. Present technology is at 0.3mm. Mold cap thickness maintains the same at 0.27mm from the present to 2007. 2 tier die stacks for the base package is not available presently. However, in 2006 and 2007, substrate thickness maintains at 0.35mm for a two-tier stacked. Pitch is at 0.65mm presently. By 2006 and 2007, pitch has to reach at 0.50mm and 0.45mm respectively. [7]

III. CONCLUSION

3D packaging is the next phase of development for advanced PCB manufacturing process. Two examples for 3D packaging are stacked die and PoP packaging. Stacked die packages basically stack one die on top of another die in some cases with an interposer while PoP stacks one package on top of another package. Both technologies have their advantages and tradeoffs.

Stacked die's yield is a huge challenge. For example, it is reported that a 2 stack package has 80% yield while a 3 stack package has 60% yield. On the other hand, while PoP may have a thicker package compared to stacked dies, PoP's can achieve the thinnest profile by having a full cavity process. Low cost, high I/O count, high performance, and size reduction can be achieved for PoP's. It is forecasted that PoP is to be the next stage for packaging technology in terms of reliability and cost. [7]

So, what is the next technology after 3D packaging like PoP's? According to Amkor Technology, they have forecasted that wafer level packaging (WLP) is the next trend after 3D packaging. WLP is characterized by small die sizes with very low lead counts, high volume, low cost and relatively stable devices. The difficulty with WLP is that present wafer level test and burn-in solutions are targeted to high-end microprocessor applications. It is most likely that WLP is going to face similar obstacles that FC has faced in the past 30 years. [10]

References:

[1] Ph. Clot *et al.*, "Industrial Flip-Chip Process for CSP-3D from Design to Manufacturing," Electronics Manufacturing Technology Symposium, 2000. 26th IEEE/CPMT International, 2-3 Oct. 2000, pp. 19-26.

[2] Illyas Mohammed *et al.*, "A Design and Performance Study of 3D Packaging for High Performance Memory Applications," Electronics Manufacturing Technology Symposium, 2003. IEMT 2003. IEEE/CPMT/SEMI 28th International, 16-18 July 2003, pp. 149–155.

[3] J. Tanskanen *et al.*, "Reliability evaluation of 3D-package with specific test structures," Electronic Components and Technology Conference, 2002. Proceedings. 52nd, 28-31 May 2002, pp. 1709-1713.

[4] F. Carson, *et al.*, "The development of a novel stacked package package in package," Electronics Manufacturing Technology Symposium, 2004. IEEE/CPMT/SEMI 29th International, Jul 14-16, 2004, pp. 91–96.

[5] S.K. Peinimaa, *et al.*, "Stacked thin dice packaging," Electronic Components and Technology Conference, 2001. Proceedings, 51st, 29 May-1 June 2001, pp 361–366.

[6] J. Miettinen, *et al.*, "System design issues for 3D system-in-package

(SiP)," Electronic Components and Technology, 2004. ECTC '04. Proceedings, Volume 1, 1-4 June 2004, pp. 610–615.
[7] Y. Eun, "Reliability Study of Package on Package," unpublished.
[8] Y.C. Kim, "3D Packaging: Where All Technologies Come Together," unpublished.
[9] 장세영, "제품화를 위한 3차원 실장 기술," unpublished.
[10] L. Smith, "Trends in multi-chip package integration," Electronics Engineer, July 2000.
[11] T. Kamgaing, *et al.*, "Future Package Technologies for Wireless Communication Systems," Intel Technology Journal Electronic Package Technology Development, Nov. 9, 2005, pp. 352-364.
[12] S. Krishnam, *et al.*, "Thermal Performance Characteristics of Folded Stacked Packages," Semiconductor Thermal Measurement and Management, 2002. Eighteenth Annual IEEE Symposium, 12-14 March 2002, pp. 42–49.
[13] Y. Yano, *et al.*, "Three-dimensional very thin stacked packaging technology for SiP," Electronic Components and Technology Conference, 2002. Proceedings. 52nd, 28-31 May 2002, pp. 1329–1334.
[14] Y. Kim, "Folded stacked package development," Electronic Components and Technology Conference, 2002. Proceedings. 52nd, 28-31 May 2002, pp. 1341 – 1346.
[15] A. Ostmann, *et al.*, "Realization of a stackable package using chip in polymer technology," Polymers and Adhesives in Microelectronics and Photonics, 2002. POLYTRONIC 2002. 2nd International IEEE Conference on 23-26 June 2002, pp. 160-164.
[16]M. Kada, *et al.*, "The Dawn of 3D Packaging as System-in-Package (SiP)," pp. 1-9.
[17] C.W.C. Lin, *et al.*, "3D Stacked Packages with Bumpless Interconnect Technology," Electronics Manufacturing Technology Symposium, 2003. IEMT 2003. IEEE/CPMT/SEMI 28th International, 16-18 July 2003, pp. 231–235.
[18] L. Wu, *et al.*, "Innovative stack-die package - S2BGA" Electronic Components and Technology Conference, 2002. Proceedings. 52nd, 28-31 May 2002, pp. 250–253.
[19] Stephane Donnay, *et al.*, "System-on-a-package integration of 4 GHz WLAN RF front-ends."
[20] Charles Harper, *High Performance Printed Circuit Boards*, New York: McGraw Hill, 2000.

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