Interconnect Reliability Correlation with System Design and Transportation Stress

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Abstract
Interconnect reliability especially in BGA solder joints and compliant pins are subjected to design parameters which are very critical to ensure product performance at pre-defined shipping condition and user environment. Plating thickness of compliant pin and damping mechanism of electronic system design are key successful factors for this purpose. In additional transportation and material handling process of a computer server system will be affected by shock under certain conditions. Many accessories devices in the server computer system tend to become loose resulting in poor contact or solder intermittent interconnect problems due to the shock load from the transportation and material handling processes.

In this paper, design variables such as pin hard-Au plating thickness, mother board locking mechanism and damping structure design are experimented and reviewed. Also a shock measurement device is used to real-time monitor the acceleration, duration and direction of shock in large stationary or moving systems in transportation and transferring process. Two transportation routes from Fushan China to Sezimovo Czech Republic through China and Russia border by train then return by sea cargo through Mediterranean, Arabic and South China Seas in which a product package is embedded with the shock measurement device. The collected force data of g force can be used to calculate the shock energy level ΔV. The comparison between the value of ΔV and shock energy tested in the lab can be used to judge whether a system design can sustain and cause contact interconnect problem in transportation and transferring process. These design variables and stresses can be evaluated by drop test or vibration test to ensure system functional integrity is achieved.

Introduction
Reliability of BGA solder and compliant pin interconnect are critical to ensure product performance is maintained at pre-defined shipping condition and user environment. Many electronic devices such as network card, HDD in the server system tend to become loose resulting in poor contact problems due to the severe shock from the transportation and material handling processes. Different design variables such as hard-Au plating thickness on the pin, Mother Board locking mechanism and damping plate are experimented and reviewed in this paper. And a shock measuring device is used to real-time monitor the acceleration, duration and direction of shock in large stationary or moving systems in transportation and transferring process.

Poor contact issue happened on some model of desktop, AIO and server computer system. After removing the top cover of computer system, some accessories such as memory and NIC card were found partially disengaged from its normal interconnect position as shown in Figure 1. Example of contact interconnect defect rate for a specific experimental test vehicle is shown in Table.1. In most of the cases these contact problems may not be permanent but can be quickly resolved by double insertion of the interconnect system.

Although not the main topic of this study other source of contact interconnect problem[1] is coming from particles or fibers from raw material, manufacturing, or the user environment in a DIMM socket pins and circuit board contact pads can be observed from time to time. These foreign materials can create a barrier for proper contact between pad and socket as shown in Figure 2. In one of the extreme case as shown in Figure 3, soft plastic white particles were smeared on the contact surface creating a risk of intermittent contact or open circuit. FTIR organic chemical analysis indicated that the fibers were Rayon/cellulose which is a common material from various sources such as cloth and gloves, which are difficult to clearly implicate in a failure. The white particles however are most likely polyethylene from plasticizer, a fatty acid that poses an interconnect concern as shown in Table 2. To avoid the accumulation of fibers and particles on contact pads, there are many changes required in environment control and management for sensitive interconnects device such as press-fit pins and optical modules. The use of particle counters is getting popular in particulate control in the manufacturing floor along with connector vacuuming, cleaning and re-seating/insertion of an edge card. Again in most of the cases these contact problems may not be permanent but can be quickly resolved by double insertion of the interconnect system to provide a clean contact interconnect interface.

Approach
In this study a realistic test vehicle as shown in Fig 4 is designed with commercial available press-fit connector of various sources on to a mother board with full electrical function. A riser card is plugged into the press-fit connector that serves as interface for NIC and SSL card interconnect. The following three design variables were experimented in addition to the pallet of test vehicles with installed shock measurement device were shipped through two shipping routes of train and sea cargo to see the correlation to the function failure of the test vehicle.

- Damping plate for NIC and SSL cards
- Hard gold plating thickness
- Locking mechanism for mother board

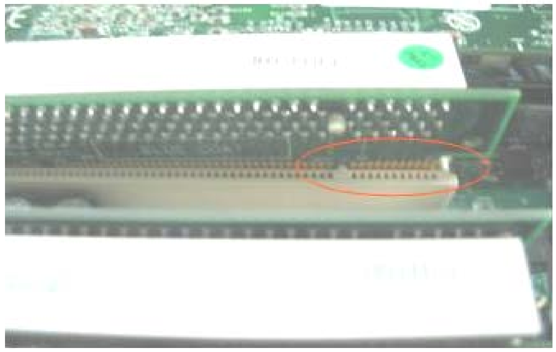
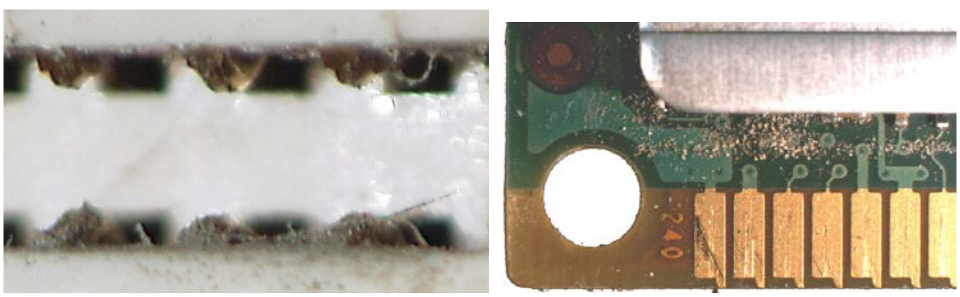


Figure 1 - Example of partial loose contact of Daughter Card from Press-Fit Connector

Table 1 - Defect rate of a series of computer server system

Model XXX to location Y	**20xx/6 to 20xx/4**	**May**	**Jun**	**Jul**	**Aug**	**Defect Rate**
Total tested Qty	2265	229	119	207	155	2975
HDD poor contact Qty	22(0.97%)	0	0	0	1(0.65%)	23(0.77%)
NIC/SSL poor contact Qty	8(0.35%)	0	1(0.84%)	0	0	9(0.30%)
Mem poor contact Qty	0	0	4(3.36%)	0	0	4(0.13%)
cable poor contact Qty	1(0.04%)	0	0	0	0	1(0.03%)
Total poor contact Qty	31(1.37%)	0	5(4.2%)	0	1(0.65&)	37(1.24%)



(a) (b)

Figure 2 – (a) Dust and fiber accumulated in DIMM slot (b) Particles found near DIMM contact pads

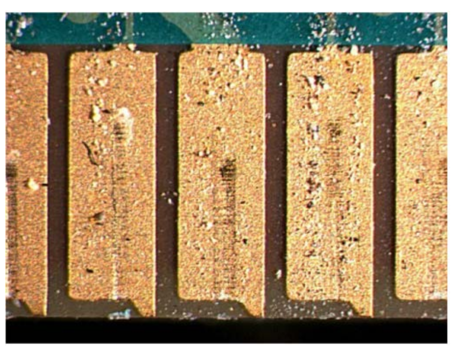


Figure 3 – Close up view of particles on DIMM contact pads

Table 2 – Chemical analysis of foreign material on contact pads

Visual Appearance	FTIR Match to Library	FTIR Attribution	Comment
Tan fiber	70%	Rayon/Cellulose	Common material, multiple sources. Rarely causes a problem, at least that can be isolated.
White particles	1) 92%, 2) 91%	1) Ethyltria-contanoate 98; 2) Polyethylene	1) Plasticizer, fatty acid, possible constituant of bulk, low melting point (soft), 0.86 g/cm3; 2) Not common use in electronics components. Softness poses concern, and is clearly engaged with contacts.

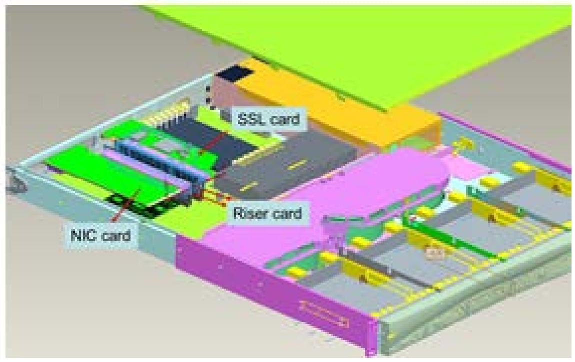


Figure 4 - Test Vehicle with Press-Fit Connector and Riser Card Interface for NIC and SSL Interconnect

Result and Discussion

I. Design Variable Change

Several design variables to improve the press-fit interconnect quality are considered to be tested in the shipping routes and during material handling. Some design changes was made specifically to solve the NIC/SSL poor contact issue.

Firstly, the plating thickness in various press-fit connectors on the test vehicle is measured. As shown in Table 3 and 4, plating thickness Au on some connectors are in the 1 micro inch range and the other are more than 15 micro inches. By comparing the Au thickness on the connector pins in Table 2 and 3, it shows that the Au thickness on some connectors is only 1 micro inch and is more than 15 micro inches on other connectors. The Au thickness measured in the poor-contact NIC/SSL (Table 4) is also less than 15 micro inches. It is thus seen that the probability of poor contact is much larger on connectors with 1 micro inch Au plating than that on connectors with 15 micro inches.

Table 3 – Hard gold Plating Thickness of Various Interconnect Devices

Cards	Model xxx	Plating	Model xxx	Plating	Model Y	Plating	Model X	Plating
Riser board	SN#ss(Riser PCB)	15µ"	SN#xxx--Riser PCBx8tox8	30µ"	SN#xxx Riser connector)	1µ"	SN#xxx(Riser PCB)	30µ"
			SN#xxx-Riser PCB 8tox4	30µ"			SN#xxx(Riser connector)	1µ"
DIMM socket	SN#xxx	15µ"	SN#xxx	20µ"	SN#xxx	15µ"	SN#xxx	15µ"
	SN#xxx	15µ"	SN#xxx	20µ"				

Table 4 - Example of plating thickness of press-fit connector

PN	DESCRIPTION	Supplier PN	PART	Contact Plating	Model	Supplier
3[illegible]2	TF-CON;SBU,C	E[illegible]	64-BIT 184PIN PCI-X	Gold Flash(1µ" Gold Min)	A	1
4[illegible]J		5[illegible]4	184PIN	15µ" Gold Min	B	2
4[illegible]3		5[illegible]4	184PIN	15µ" Gold Min	C	3
3[illegible]0	TF-CON;SBU,F	A[illegible]	98PIN PCI-X	30µ" Gold Min	D	4
		F[illegible]	98PIN PCI-X	30µ" Gold Min	E	5
		2[illegible]	98PIN PCI-X	30µ" Gold Min	F	6
3[illegible]4	TF-CON;SBU,F	1[illegible]	164PIN PCI-X	15µ" Gold Min	G	7
		V[illegible]WS	164PIN PCI-X	15µ" Gold Min	H	8
		G[illegible]	164PIN PCI-X	15µ" Gold Min	I	9

Secondly, increase in damping plate area and thickness. In the original system, as shown in Figure 5, there were no damping plates on the Riser card and NIC/SSL card. Changing the damping material from plastic to more elastic foam material to helped to enhance the damping effect of the system to overcome external shock load. The new foam will continue in contact with the riser card with no gap between foam and riser card. It can prevent riser card coming out of connectors under transportation stress. In the current design, the Riser card was pressed by one plastic part and the NIC/SSL card were pressed by foam as shown in Figure 6. The exact thickness of the foam damping plate is based on the below tolerance analysis.

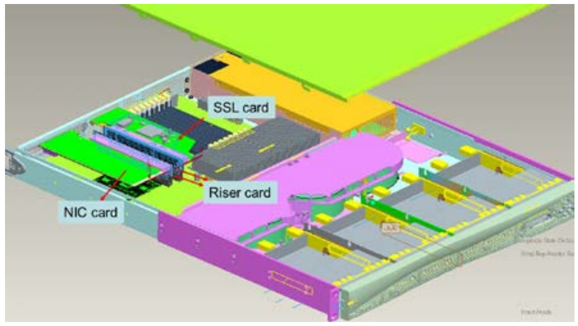


Figure 5 – Original design with no damping plate for daughter cards

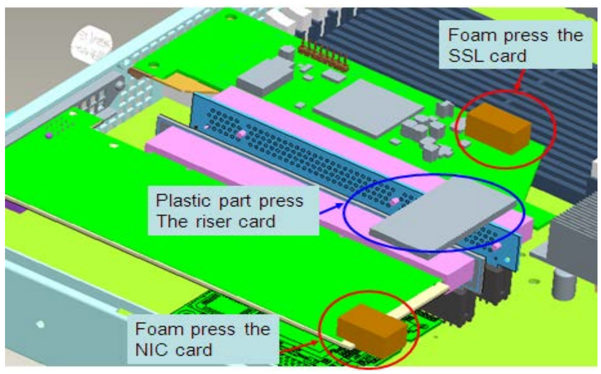


Figure 6 – Foam plates added to enhance damping effect

The tolerance analysis (TA) conducted on the stack of mechanical parts indicates that there is some tolerance among different mechanical parts when the top cover is assembled, which results in a gap between the plastic plate and riser card as shown in Figure 5. The gap is -0.277mm MIN and 0.697mm MAX. When the system is in shock, only one end of the Riser card is pressed; the other end would lift. Based upon this gap issue, the new design is adopted. In the new design, foam is used instead of the plastic sheet to press the Riser card; the foam is thicker and the damping area is larger. Figure 7 lists the difference between the current design and the new design. In the new design, the tolerance analysis shows that the gap between the foam and Riser card is -1.927mm MIN and -0.953mm MAX. Therefore, no gap exists between the foam and Riser card. The two can be firmly pressed. The foam would be pressed tightly onto the top cover and would not lift the top cover due to its perfect elasticity with the change as shown in Figure 8.

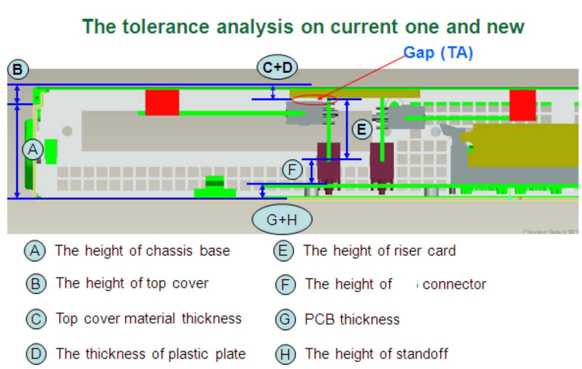


Figure 7 – Tolerance Analysis on stack of mechanical parts

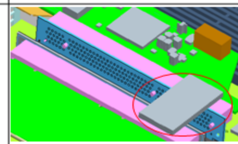
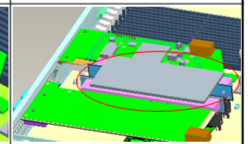
	Current design	New design
Detail		
Part material	plastic	Foam
Thickness	3.1mm	4.5mm
Size	25*50mm	50*110mm

Figure 8 – Damping material design and tolerance analysis

Thirdly, although NIC/SSL is pressed by foam vertically, no protection is there horizontally. The jack that connects the Riser card and NIC/SSL is also seated horizontally. When NIC/SSL is in shock, they may slip from the jack on the Riser card, resulting in poor contact. So, adding mother board locking mechanism can help prevent the disengagement of NIC/SSL card from the Riser card during the vibration of the mother board. Figure 9 illustrated two plastic holders are used to fix the NIC to prevent PCB swaying in transportation.

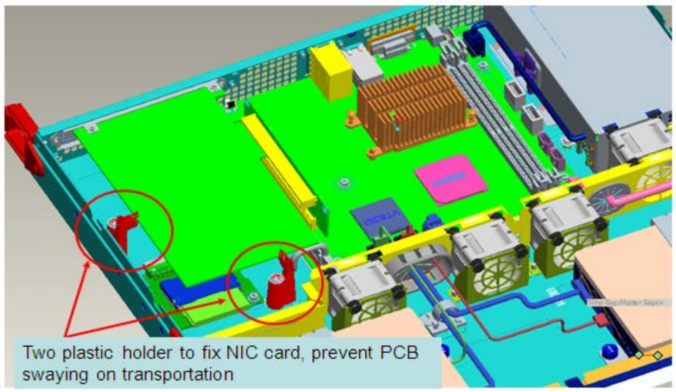


Figure 9 – board locking mechanism to restrain horizontal movement

After the implementation of the three changes in design variables, the effect to the failure rate would need to be verified in terms of whether the system can survive during the severe shock in the transportation and handling processes. Two transportation routes from Fushan China to Sezimovo Czech Republic through China and Russia border by train then return sea trip through Mediterranean, Arabic and South China Sea. As shown in Figure 10, a shock gravitational force measurement device is embedded in the shipping box of the computer server to record the acceleration and direction of shock in real-time in large stationary or moving systems in transportation and transferring process. The data collected can be used to calculate the shock energy level △V. The comparison between the value of △V and the criterion can be used to judge whether the shock can cause poor contact problems in transportation and transferring process. At the same time the maximum temperature and humidity were measured by temperature sticker and humidity sticker as compared to the reading from the shock measuring device.

Figure 10 – A shock gravitational force measurement device is embedded in the shipping box

II. Improvement Effect Verification

Lab drop testing with extreme condition was performed on a boxed computer server system to emulate the harsh transportation process as shown in Figure 11. Test settings are 250Hz filter frequency and drop height 610mm for the packaged weight of 16.42Kg. In the test, the accelerometer is installed in the box and used to record the acceleration and duration along X, Y and Z axis when the system is going through 10 multiple corner-edge-faces drop tests. After the lab test and road test, the system is going through normal boot up and inspection and if any accessories get loosened then the package box is checked, and humidity and temperature numbers on sticker are recorded.

Figure 11 – Lab ten corner-edge-face multiple drop tests to emulate transportation stress

Maximum shock energy from field measurement and lab test were then calculated based on formula (1)[2]. If the total energy level from lab drop test on the product is larger than from real transportation and handling stress then the package design is able to protect the electronic product from shock and vibration in the shipping.

$$\triangle V = 2/\pi * A * D * 10^{-3} \qquad (1)$$

Where

A is the peak acceleration of nominal pulse in g

D is the duration of nominal pulse in 1/ms

The maximum shock force level along X, Y and Z in the drop test is recorded in Table 5. The maximum △V calculated from equation (1) is 17.09 along the Z-axis which can be used as the criteria to judge whether the shock energy level for the packaged system is out of limits in transportation and transferring processes. The data maximum g force from those two routes by train and sea are retrieved from the shock measurement device then the same computation was done as above for maximum energy levels △V. The maximum acceleration recorded by device from the railroad route along the horizontal xy-direction is 20g and vertical z-direction is 35g which covert to 5.46 total energy. On the other hand the maximum acceleration recorded by the device from the sea cargo route along the horizontal xy-direction is 13g and vertical z-direction is 11g which converts to 2.03 total energy. Comparing the total shock energy of railway and sea cargo to the maximum energy from the lab test indicate the package design and three design improvements are able to eliminate the contact interconnect problem and reduce the failure rate to zero.

Table 5 – Product multiple corner-edge-face drop test

Product Package Drop Test			
Corner-edge-face drop Number	MaxX	MaxY	MaxZ
1	31.7	9.3	6.3
2	43.4	13.6	7.1
3	56.4	6.4	16
4	4.6	25.3	21.7
5	69.2	7.7	10.8
6	77.3	5.9	16.1
7	4.9	46.2	18
8	2.9	32.2	3
9	6.2	3.9	49.6
10	8.7	10.8	109.5
Max. Value（g）	77.3	46.2	109.5
△V (m/s)（Assumed Value 4ms）	1.93	1.15	2.73
△V (m/s)（Assumed Value 11ms）	5.31	3.17	7.52
V (m/s)（Assumed Value 25ms）	12.06	7.21	17.09

Finally the temperature and humidity from the stickers in the packaging box and data measurement from shock measurement device are all within the product testing requirement for product storage and operation , $+40\sim-40^{0}$C and 30~95%RH to fulfill the product warranty mission time.

Conclusion

The contact interconnect problem of electronic accessories in the computer server system due to the severe shock in the transportation and transferring processes can be resolved through the following three approaches:

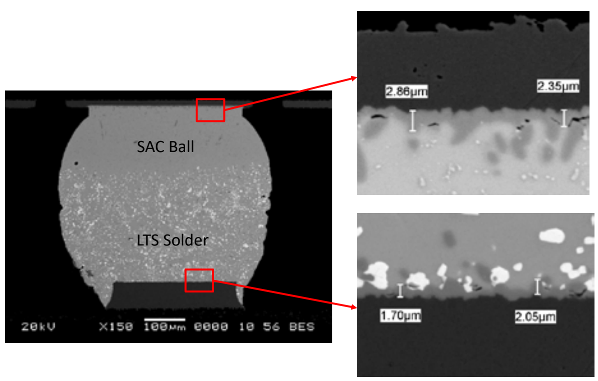
- Ensure hard-Au plating thickness
- Increase the damping plate area and thickness
- Add the mother board locking mechanism

The re-design verification approach to compare shock energy from the field through two shipping routes to the lab test indicated that the total energy level from the lab drop test on the product is much larger than from real transportation and handling stresses so that the package design is able to protect the electronic product from shock and vibration during the shipping and avoid the contact interconnect failure totally.

Future Work

One of the major drawbacks of this energy level approach which derived from the maximum g force is not able to compute the accumulated stresses so as to understand the damage from accumulated energy to the interconnect system of contact and solder joint. The research teams are looking forward to add the lab rolling rock test to emulate the accumulation energy for railway and sea cargo routes then compare to the shock energy accumulated over time in these two routes by integration of the area under the g force-time curve.

The iNEMI Board Assembly Technical Roadmap of 2017 predict that the low temperature soldering (LTS) usage will increase to 20 plus percent by 2027[3]. The drivers for this LTS technology trend are three folds, the energy and CO_2 emission reduction, overcome material limitation in electronic component and PCB, and low temperature soldering process to match with electronic miniaturization. Due to the nature of the brittleness of Bismuth contained in the low temperature solder SnBiAg, the impact related failure rate of LTS is substantially below current SAC305 which is widely used. Potential mechanical strengthening mechanism, such as corner or edge bonding material is attached along the BGA are being evaluated to reduce the susceptibility to mechanical shock. Since some of the BGA still use SAC lead-free solder there is going to be forward compatibility issues with LTS paste applications to the SAC component circuit interconnect system. The mixture of SAC and SnBiAg create a complicated mixed alloy system in which Bismuth tends to form a layer in bulk form in the mixture as well as along the IMC and solder interface[4] as shown in Figure 12. It is intention of the project team to use the energy level approach to evaluate the LTS solder joint interconnect integrity when the product package are going through the same shipping routes.



(a) (b) (c)

Figure 12 – Microstructure of mixed alloy of SnAgCu and LTS (a) with IMC thicker at package side (b) and Bismuth accumulation at LTS and IMC interface (c)

References

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