ACHIEVING SMT COMPATIBLE FLIP CHIP ASSEMBLY WITH NO-FLOW FLUXING UNDERFILLS

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Abstract

Recent developments in No Flow-Fluxing Underfill (NFFUF) products have demonstrated their utility to enhance the reliability of flip chip assemblies with reduced processing steps over conventional capillary flow methods. This basic work considered processing conditions such as dispensed volume and placement force, speed and dwell time. Further evaluations of these new products on a variety of flip chip assembly configurations manufactured by various processes have been undertaken to provide further evidence of their suitability and potential in high volume electronic manufacturing.

This paper summarizes the recent evaluations and discusses new studies of additional assembly configurations, which include higher input/output (I/O) counts up to full arrays in excess of 1200 I/Os. The primary land surfaces used in these experiments were organic solder preservative (OSP) coated copper and Nickel/Gold (NiAu) over copper. The paper also examines the use of NFFUF to make Ball Grid Arrays (BGA) and Chip Scale Packages (CSP) more rugged, a requirement that is emerging in the marketplace. This characteristic is being sought for assemblies such as rugged portable computers for field data collection, automotive under-hood electronics and certain space applications where more extreme stresses are imparted to the interfaces between the device and the substrate.

In addition, the paper discusses the processing considerations and assembly constraints that define the processing window required to attain high electrical continuity yields while meeting reliability requirements for the various peripheral bumped assembly configurations. The results of typical tests used to predict assembly reliability, such as thermal shock resistance and JEDEC pre-conditioning, are also described.

Introduction

The packaging of microelectronics devices is moving toward high density interconnects that can accommodate larger integrated circuits. The use of flip chips, CSPs and BGAs has increased over the past two years to meet these needs. It has been found that flip chips in particular benefit from the use of underfills to meet assembly reliability requirements. CSPs and BGAs have also employed underfill materials to increase shock and vibration resistance for demanding applications such as automotive devices, cellular phones and other portable electronic products.

While traditional capillary flow materials used for this purpose now possess high flow speed and reduced time to cure, they require additional processing steps. The use of newly developed NFFUF suggests a means of reducing these processing steps and enhancing Surface Mount Technology (SMT) compatibility. They can be applied and used in virtually the same manner as traditional tacky flux products to pre-attach devices prior to the underfill step. Consequently, they can provide both the fluxing and the protective underfill layer within the

same reflow process used for solder paste. A comparison of SMT assembly process steps using traditional capillary flow versus NFFUF is presented in Table 1.

Table 1. Assembly Process Steps Comparison

SMT Assembly	SMT Traditional Flip Chip	SMT Fluxing Adhesives
Apply solder paste	Apply solder paste	Apply solder paste
Place discretes	Place discretes	Dispense flux adhesive
Place ICs	Flux die	Place discretes
Reflow paste	Place ICs and die	Place ICs and die
	Reflow	Reflow
	Pre-heat assembly	
	Dispense underfill	
	Capillary flow	
	Cure underfill	

Performance data, gathered from recent field evaluations and new studies, are reported here to help assess the reliability and usefulness of the NFFUF on various test vehicles and under various process conditions.

A variety of substrates and area array packages were used in these evaluations. Substrates included rigid boards and one flexible circuit. The packages included three peripheral array flip chips, two full area array flip chips, two chip scale packages (CSP), and one ball grid array. Specific substrates and packages are identified in Table 2.

TABLE 2: Substrates and Packages Utilized in Evaluation

Substrates	Composition	Thickness	Metallization
Rigid Board	High Tg FR 4 single sided	62 mil	Ni / Au
	High Tg FR 4 single sided	62 mil	OSP Cu
	High Tg FR 4 double sided	62 mil	OSP Cu
	High Tg FR 4 double sided	31 mil	Ni / Au
	High Tg FR 4 double sided	31 mil	OSP Cu
Flexible Circuit	KAPTON® Polyimide	5 mil	OSP Cu
PACKAGE TYPES		**Size**	***I / O count***
Peripheral Array Flip Chip			
PB 500		500 x 500 mil	96
MSFB		220 x 240 mil	96
PB8		200 x 200 mil	88
Area Array Flip Chip			
FA-10		200 x 200 mil	300
FA-10		400 x 400 mil	1200
Chip Scale Package (CSP)		400 x 400 mil	108
SuperCSP®		350 x 350 mil	240
Ball Grid Array (BGA)		1000 x 1000 mil	256

Results

Section 1: Performance Data on Peripheral Bumped Assemblies

The reliability of peripheral-bumped (PB), 500 and 200 mil, square dies on both OSP-coated and Ni/Au land finishes using NFFUF products has been verified in previously published work. . Evaluations with PB-8 die show NFFUFs can withstand liquid-to-liquid thermal shock of more than 1000 cycles from -55° to 125°C. These assemblies maintained electrical continuity and displayed no significant delamination. A PB-500 assembly, incorporating NFFUF products, withstood air-to-air thermal shock from -65° to 150°C

maintaining continuity and exhibiting no delamination after 1500 cycles. These same assemblies passed JEDEC Level 3 followed by JEDEC Level 2 requirements.

In more recent work, larger builds of 300 MSFB die on both OSP-coated and Ni/Au lands were made with three commercially available NFFUFs. All of them provided continuity yields in excess of 98 percent. One product used on the OSP-coated lands gave a 100 percent yield. While the test dealt with a population quite small by production standards, it is considered an indicator of the high yields that can be achieved with this technology. It is believed that even higher yields could be attained with a steady state process and improved processing techniques.

Evaluation of a NFFUF was also made on a peripheral-bumped 200 x 200 mil die. The assembly configuration for this build used 3-mil bumps on a 6-mil pitch. Assemblies withstood liquid-to-liquid thermal shocks of more than 1000 cycles from -55° to 125°C. Initial continuity failures began to occur at 1150 cycles with a mean time to failure of 1785 thermal shocks.

In another evaluation a NFFUF was tested on a board fabricated with a 62 mil thick high Tg FR4 substrate having a NiAu finish over the copper pads. The test vehicle contained eight SuperCSP® sites. Immediately after assembly, about 90 percent of the CPS exhibited complete electrical continuity. Cross sections are to be performed upon completion of thermal shock evaluations to determine if lower than expected yields are the result of observed solder mask registration issues. To date these assemblies have withstood 2000 thermal shocks, air-to-air, in the -25° to 125°C range without any loss in continuity or delamination.

Test Vehicle for New Studies

To extend the evaluations of the NFFUF products, a new double-sided test vehicle was designed. It employed a 62-mil thick FR-4 substrate with OSP-coated copper lands. The area array devices included two different full array flip chips on side one (a total of six sites) and eight CSPs and two BGAs on side two.

During the board and device inspection, two issues arose. First, the flip chip locations on the board were the mirror image of their intended sites. Although evaluating continuity was still feasible on most areas of the die, one bump was sitting on the solder mask while the corresponding pad had no bump. The principle concern with the miss-aligned device was that the bump on the solder mask would not allow for proper collapse of the other bumps. The bump variations differed from die to die. The 200 x 200 mil die with 300 I/Os (FA-10) contained only one pair of these misplaced bumps to pads while the 400 mil die with 1200 I/Os (FA-10) contained four pairs of misplaced bumps.

On side two, the main issue seen during inspection was the planarity of the large BGAs, 1 inch square. The BGA evaluated consisted of 256 bumps, 24 mils high, 32 mil diameter in a peripheral array format. No issues of planarity or alignment were observed with the CSP, which is 400 mils square with 17 mil bump height, 23 mil bump diameter and a 32 mil pitch.

Test Board Evaluations

A preliminary build (reflow) was made with two NFFUFs (identified as A and B) to determine any additional issues that required resolution. The products were dispensed on all the devices in one large spiral pattern. A summary of the preliminary build data is presented in Table 3.

Table 3: Summary of Double-Sided Board Preliminary Build

DEVICE	FA10 – 300 I/O		FA10 – 1200 I/O		CSP	
Product	A	B	A	B	A	B
# of Devices	20	20	20	20	18	18
Yield %	100	50	50	50	67	0
Pass 500 T/S	20 OF 20	10 of 10	10 of 10	10 of 10	11 of 11	N/A
Pass 1000T/S	20 OF 20	10 of 10	10 of 10	10 of 10	11 of 11	N/A

All functional assemblies were tested for liquid-to-liquid thermal shock resistance from -55° to 125°C. At 1000 cycles (the results to date), all devices that achieved good initial continuity were still functioning after 1000 cycles.

Several additional issues were noted in testing with this preliminary build. Some voiding was seen around bumps on most devices. Evaluation of more dispensing patterns with each device is planned to determine the best technique for eliminating these voids. Continuity yields were low for all devices except the 200 mil full area array flip chip with one of the NFFUF products. To resolve these yield issues, further examinations of the reflow profiles and placement force and dwell times are also planned. Also, it was found that the size differences among the components made it difficult to tune the reflow profile to insure that all devices fell within a specified window. This was particularly true of the BGA and CSP devices on side two of the board.

The BGA package presented other variables in the planarity of the device, its size and the larger bumps. This particular BGA package was quite large, measuring one square inch with three rows of peripheral bumps. In most cases the two interior rows of bumps displayed 100 percent interconnect. The continuity issue routinely was observed to occur with one side of the outermost row of bumps. The observed BGA warpage during device inspection may account for this.

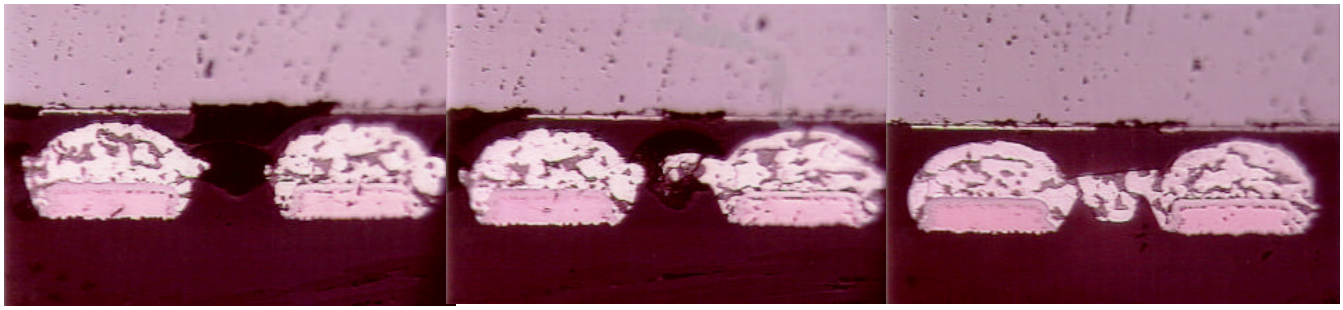
Processing

Section 2

Processing considerations and assembly constraints using the new NFFUFs were investigated in each of the manufacturing steps: pre-bake; dispense operations; placement operations; and reflow operations.

One critical consideration in achieving reliable flip chip assemblies utilizing either NFFUF products or traditional capillary flow underfills is the elimination of large voids (>2 mils), especially between bumps. Voids are caused primarily by moisture in the substrate and entrapped air from dispensing and die placement. When voids between bumps exist and the device is subjected to thermal shock, the pressures exerted on the solder joint force the solder into the void. If the void is large enough, the resulting failure allows bridging from one I/O to the adjacent one. This can be seen in the cross-sections shown in Figure 1.

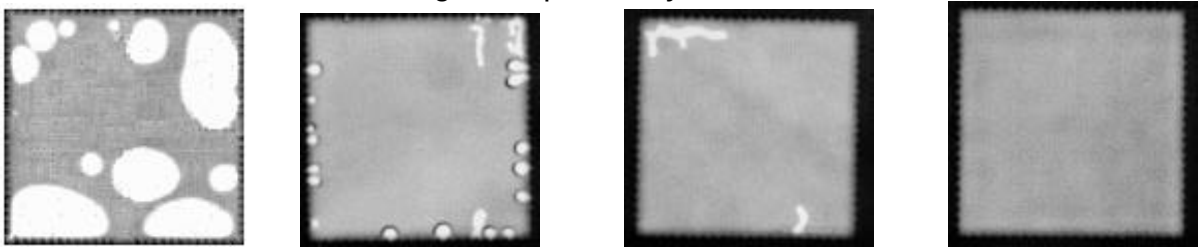
Figure 1: Solder migrating into void between bumps



Pre-bake

Moisture absorbed by the substrate previous to assembly can create voids in the NFFUF during reflow processing. To eliminate moisture-induced voids, the substrate must be pre-baked. To determine the proper pre-bake temperature and time guidelines for eliminating such voids, two studies were conducted. The substrates examined were made of 31 mil thick FR4 and Kapton®, a flexible polyimide material. The metallurgy used in both studies was OSP over copper, since there were concerns that too long or high a pre-bake schedule may compromise yield by allowing for too high an oxide buildup on the copper.

Assemblies, comprised of PB8 (200 mil sq.) die on 31 mil FR-4 substrate with OSP over copper finish were removed from inventory. Assemblies were made with several NFFUFs under typical reflow profile/temperature conditions (see Diagram 2). C-sam inspections were made to observe the degree of voiding for base-line comparisons. Additional substrates were then placed into 60°C and 120° ovens. Substrates were removed at various time intervals. Assemblies were then made and again inspected by C-sam.



No Pre-bake | Pre-Bake 24 hrs. @ 60°C | Pre-Bake 96 hrs. @ 60°C | Pre-Bake 2 hrs. @ 120°C

Results from the 60°C pre-bake evaluation showed voiding still in evidence even after 96 hours of bake time. At 120°C, voiding virtually disappeared after 90 minutes of bake time. Yield values for forty assemblies in a pre-bake time range between 90 minutes and 3 hours were at the 100 percent level. Boards that were also conditioned for 18 hours at 120°C exhibited lower yields, about 90%. Cross-sections indicated problems with bump-to-pad wetting. This suggests the use of a nitrogen-purged oven when OSP over copper is employed.

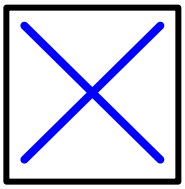
Three different NFFUFs were also evaluated using a PB-500 device on a 62 mil FR-4 assembly configuration both without a pre-bake schedule and with a 2-hour pre-bake at 120°C. Results from this study indicate that formulation compositions have an effect on the degree of voiding seen in substrates that were not pre-baked. One composition in particular exhibited consistently less voiding than did the other two. This suggests that pre-bake schedules can be shortened through proper product selection.

Although a pre-bake schedule of 2 hours at 120°C was employed with a Kapton® assembly, voiding was still in evidence upon reflow. This suggested that re-absorption of moisture could be the issue. Studies, therefore, centered on the length of time the Kapton® substrates could be exposed to humid conditions. Kapton® substrates were removed after baking for two hours at 120°C and placed in a humidity chamber set at 25°C and 50% RH. Assemblies were removed every 10 minutes, built (reflowed) and inspected by C-sam. Within 40 minutes of exposure, the first evidence of voiding became visible. After 70 minutes, the level of voiding approximated that of non-dried Kapton® substrates. These results indicated that moisture-induced voiding occurs rapidly, within 40 minutes, on the Kapton® substrates.

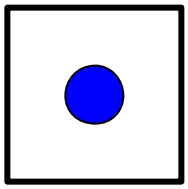
Dispense Patterns

One issue in the dispensing of a NFFUF is how the dispense pattern influences the creation of air voids around the bumps either during dispensing or flow-out of the material. Three dispense patterns were studied using a PB-500 die on a 62 mil FR-4 substrate with a NiAu lands. The pads were located in a solder mask-defined trench of 16 mils in width. Boards were pre-baked for 2 hours at 120°C to remove moisture. The desired quantity of NFFUF was deposited by an automated positive displacement dispenser. The dispense patterns are illustrated in Diagram 1.

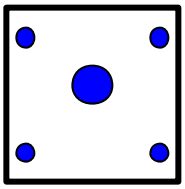
Diagram 1



X pattern (10mg. ea.)



Glob (20 mg.)



5 Dots (4mg. ea. Corner, 8 mg. center dot)

C-sam inspections of assemblies, ten for each dispense pattern, indicated that the glob pattern entrapped no air voids while the other two occasionally created a small void around a solder joint and sometimes an elongated void running down the trench. It was concluded that when multiple flow fronts converge during placement they are more likely to trap air voids. The other advantage with the glob pattern is that the time to dispense is much shorter than the X pattern or the 5 dots.

Placement Parameters

Three placement parameters were studied using one of the NFFUF products. The parameters were speed of placement; placement dwell time; and placement force. Placement speed and dwell time (the amount of time the force is applied to the die after placement) are important influences on production throughput speed while placement force has no impact on throughput.

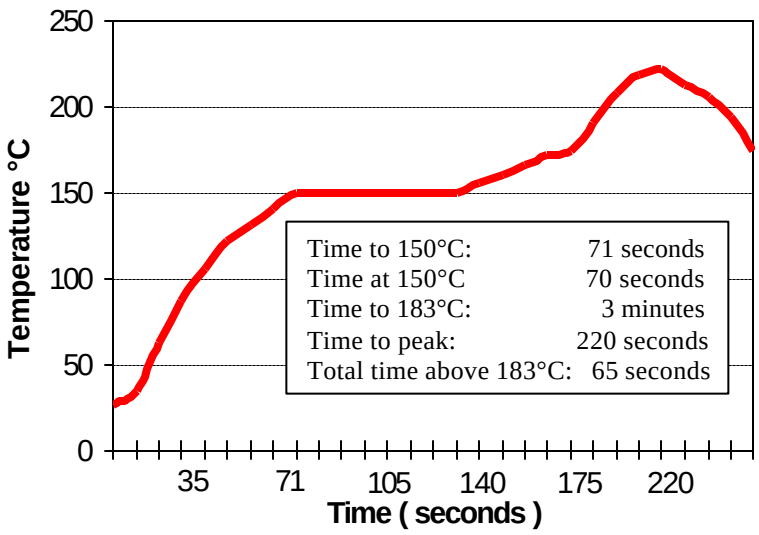
Air entrapment is a primary issue influenced by placement speed. As the die is placed and contact is made with the NFFUF, this action compresses the NFFUF and spreads it out. The NFFUF must flow evenly around bumps and fill depressions on the board. These depressions are either trench-defined pads, popular in peripheral arrays, or solder mask-defined pads, most often employed in full area arrays. The faster the placement speed, the faster the NFFUF flows around the obstructions, bumps, and over the depressions. This action suggests that a higher degree of air entrapment will occur as placement speed increases.

The assembly configuration used in the study was a peripheral-bumped die (PB-500) on a 62 mil FR-4 substrate with trench-defined Ni/Au lands. The study evaluated three placement speeds of 2, 5 and 10 cm./second. C-sam inspections indicated that within this placement speed window on this configuration there was an equivalent incidence of voiding. Contrary to our suspicions, voiding did not increase with faster placement speeds within the test window. Similar studies should be performed with full area arrays and solder mask-defined pads.

Placement dwell time and force have a predominant influence on continuity yield. The dwell time allows the liquid rebound effect to dissipate before the pressure is released. The placement forces insure that all bumps are in contact with the lands. Using the same

assembly configuration, the study evaluated dwell times of 5, 2 and 0.5 seconds at 400 and 600 grams of force. After reflow, all thirty test-configurations exhibited 100% continuity.

Diagram 2



Reflow Oven Parameters and Effect on Cure and Reworkability

Reflow oven time and temperature are critical parameters in achieving interconnect and the required degree of cure. The traditional reflow profile recommended for most solder pastes is illustrated in Diagram 2. In this profile the PCB ramps to 150°C in 71 seconds at which point a dwell of 70 seconds occurs. This dwell allows volatile solvents to evaporate from the solder paste after which the ramp in temperature continues through the solder's liquid-state temperature (183°C) at 3 minutes. The profile peaks at about 220°C with a dwell time in the liquid-state range of about one minute. Unlike traditional tacky fluxes, the NFFUFs are 100%-solid polymeric materials. Their viscosity must remain low to insure that proper wetting and bump collapse occur. Issues arise when either the dwell time at 150°C is extended or the dwell temperature rises above 150°C. Either condition can affect the quality of interconnect because cross-linking and molecular weight build-up of the NFFUF have increased its viscosity to the point where it can compromise the wetting of the bump to pad.

NFFUFs cure after they reach the liquid-state phase (183°C). Degree of cure is greatly influenced by the peak temperature attained and the length of time above 183°C. The percent cure achieved by two NFFUFs (A and B) after one reflow exposure and with four different reflow modifications to the time and temperature of the solder's liquid-state phase was examined by differential scanning calorimeter. Results are compared in Table 3.

Table 3

Profile #	Time above 183°C	Peak Temperature	Product A % cure	Product B % cure
1	1 minute	220°C	33%	50%
2	1 minute	240°C	40%	67%
3	2 minutes	220°C	56%	78%
4	2 minutes	240°C	73%	94%

Both Products A and B, compared in this evaluation, are designed for use with the standard reflow profile illustrated in Diagram 2. However, Product B is more sensitive to the amount of time and temperature to which it is exposed below the liquid-state phase due to the formulation composition.

Product A, as reflowed in profile #1, is easily reworked by rapidly pre-heating the assembly to 190°C, shearing the die from the substrate and cleaning with a solvent and soft brush. Product B in profile #1 at 50% cure, on the other hand, is not easily reworked.

Other NFFUFs that will cure in one reflow profile are available. However, the extent to which the profile is altered for this purpose can cause issues with certain solder pastes, component tomb-stoning and solder paste voiding. Some of the newer solder pastes are reported to be insensitive to the ramp rate of the reflow profile and hence more suited for profile alteration.

Conclusions and Future Work

The studies show that NFFUFs used with peripheral-bumped flip chips can meet the reliability requirements of most direct chip attach (DCA) applications. The devices evaluated included dies up to 500 mils square with bump pitch down to 6 mils. The studies also indicate that the continuity yield attained with these devices exceeded 98 percent and can be improved with fine-tuning and a steady state production process. Additional processing studies should be undertaken with full area array flip chips, particularly on the larger 1200 I/O die. Issues dealing with board fabrication, voids and yield deserve further examination and resolution.

Two different CSP builds using NFFUFs were examined in this work. Each was evaluated on a different assembly configuration with different process conditions. The SuperCSP® build provided 90 percent continuity yields and withstood 2000 thermal shocks which is considered reasonably successful performance. Two NFFUFs were used for the other CSP build on the double-sided test vehicle. Testing with Product A provided yields of 70 percent. With Product B, no package achieved 100 percent continuity. Yet Product B was the same one that performed well in the SuperCSP evaluation. This suggests that processing or land finish differences, may have been issues that deserve further study.

With most BGAs, one side of the exterior row of bumps did not interconnect. This suggests further examination of the planarity. This larger device requires further examination of placement parameters. All the processing work presented in this paper was performed on various peripheral-bumped flip chips. The processing information related to the pre-bake and reflow profiles is also appropriate to other devices. However, dispense and placement parameters may differ for other devices and must be evaluated further.

Performance results assembled from recent work and the new studies reported here indicate that NFFUF have real potential in high-volume electronic manufacturing. Evaluations to date show that they can perform on various assemblies, on various vehicles and on various process assembly lines. Their ability to eliminate or reduce processing steps decreases cycle times and suggest significant benefits in production cost savings. Further studies are underway to extend the evidence of their reliability and usefulness for widespread industry application.

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