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RELIABLE NOVEL NICKEL-FREE SURFACE FINISH SOLUTION FOR HIGH-FREQUENCY PCB APPLICATIONS

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ABSTRACT

The evolution of internet-enabled mobile devices has driven innovation in the manufacturing and design of technology capable of high-frequency electronic signal transfer. Among the primary factors affecting the integrity of high-frequency signals is the surface finish applied on PCB copper pads – a need commonly met through the electroless nickel immersion gold process, ENIG. However, there are well-documented limitations of ENIG due to the presence of nickel, the properties of which result in an overall reduced performance in high-frequency data transfer rate for ENIG-applied electronics, compared to bare copper.

An innovation over traditional ENIG is a nickel-less approach involving a special nano-engineered barrier designed to coat copper contacts, finished with an outermost gold layer. In this paper, assemblies involving this nickel-less novel surface finish have been subjected to extended thermal exposure, then intermetallics analyses, solder ball pull and shear tests to evaluate the aging and long-term reliability of solder joints, and insertion loss testing to gauge whether this surface finish can be used for high-frequency applications.

Key words: surface finish, ENIG, nickel-less technology, high reliability, robust solder joint, intermetallics.

INTRODUCTION

With the tremendous growth of mobile phones/devices, the availability of internet, and hand-held/wearable devices, the amount of information transfer occurring on wireless networks has increased enormously. In order to transfer the amount of data required by today's standards, electronic device manufacturers resort to high speed, high-frequency electronic signals. The integrity of high-frequency signals can be affected by the choice of materials used to fabricate printed circuit board (PCB) assemblies in receiving devices. The combination of high-frequency signals with small geometry conductive traces (eg: wearable devices, etc) lead to signal losses and compromised performance.

The primary factor which affects the integrity of high-frequency signals is conductor loss, mainly affected by the surface finish applied on the copper pads of PCBs [1] [2]. Among the surface finishes available for these applications, Electroless Nickel Immersion Gold (ENIG) surface finish has been a popular choice. However, ENIG can lead to an increase in insertion loss due to presence of nickel (see schematic Figure 4, and graph Figure 1 below). Nickel has

1/3 of the conductance of copper, leading to higher conductor losses [3]. Also, the nickel-phosphorous (Ni-P) layer has ferromagnetic properties which adversely affect the circuit performance [4].

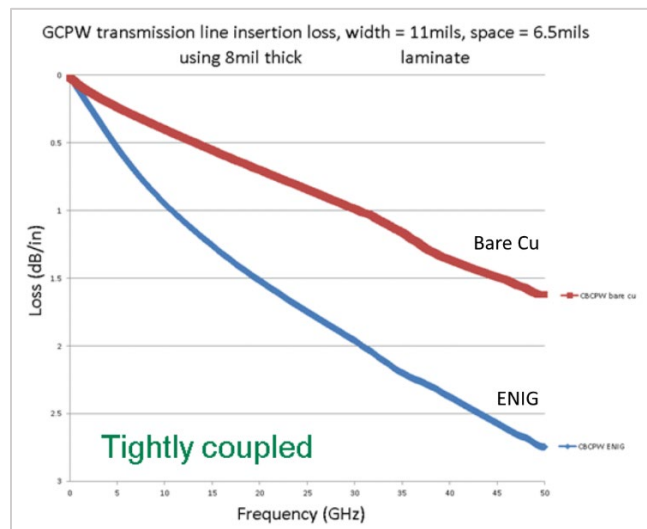


Figure 1. Insertion loss comparison between circuits with bare copper conductors and with ENIG-plated copper conductors, from 0 – 50 GHz. [3]

Figure 1 shows increased insertion loss due to ENIG surface finish on copper conductors compared to bare Cu over 0 – 50 GHz range. [3] [4] [5]. 5G cellular networks, which are currently in use worldwide, are using millimeter frequency bands at the higher end of that range; for example, Verizon (US) is using a 29 GHz band, and AT&T (US) is using a 39 GHz band [6]. Higher GHz bands are already being discussed for cell networks between 50 – 100 GHz due to the higher throughput of data available at higher frequencies [7], and automotive radar already uses a 76-81 GHz band [8]. This creates an issue that must be addressed not only for fast-approaching future technologies, but also for current devices which still have to contend with the signal losses due to the nickel in ENIG surface finishes. Already, the market is using a number of high-frequency circuit boards, and is one of the fastest-growing areas in the electronics industry (Figure 2) [9].

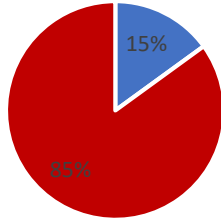


Figure 2. High-frequency PCB market share in China [9]

With the growing need for circuit boards and designs for high-frequency applications, the insertion loss due to ENIG surface finish is becoming unacceptable in the industry. In these applications, a new type of surface finish must be developed. The requirements for a replacement for ENIG in this sphere should be: 1) no nickel, in order to remove the high insertion loss and ferromagnetic element of ENIG surface finish; 2) gold final finish in order to retain the high reliability and long shelf life rating that ENIG is used to satisfy currently. A surface finish solution satisfying both of these criteria could reasonably replace ENIG in high-frequency applications without a loss of features which ENIG provides in lower-frequency circuits.

In this paper, a proposed alternative to ENIG for high-frequency applications is discussed – a Ni-free surface finish solution in which a barrier layer is deposited on bare copper in place of nickel in ENIG, and gold is deposited on the barrier layer (see schematic Figure 3). There is no nickel in this approach and therefore no adverse effects of insertion loss for high-frequency/space related circuits, and the reliability aspect of the gold final finish is still upheld.

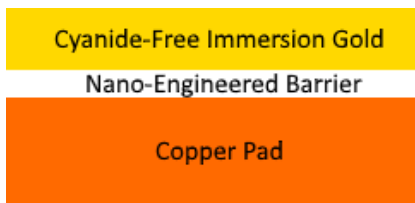


Figure 3. Nickel-less surface finish that is tested in this paper, which includes a nano-engineered barrier layer instead of the Ni-P layer in ENIG. Layers not to scale.

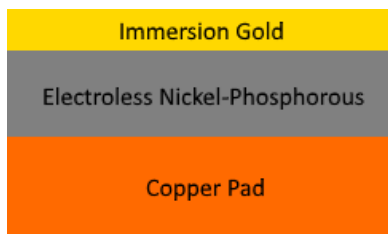


Figure 4. ENIG surface finish, including the problematic nickel-phosphorous (Ni-P) layer. Layers not to scale.

EXPERIMENT

The goal of the following series of experiments was to determine whether the novel Ni-free surface finish outlined

above would function within acceptable parameters for high-frequency applications. In order to do test this, PCBs were plated with the Ni-free surface finish and then put through a series of tests to determine solder joint strength and insertion loss. Solder joint strength samples went through many reflow cycles and extensive aging, and then were analyzed by examining: intermetallic compound (IMC) growth, which was compared against industry-standard Ni-less surface finishes; and solder ball pull and shear test failure modes. Insertion loss data from the Ni-less surface finish was compared against pure copper (no surface finish).

The barrier layer in the Ni-less surface finish in this paper serves a couple of different purposes. First, the barrier layer passivates the copper. Second, similar to the function of the Ni-P layer in ENIG, the barrier layer provides a barrier between the copper and gold, and therefore also a barrier between copper and the tin of the solder ball during the soldering process. Theoretically, this should limit the intermetallics growth due to the barrier inhibiting diffusion between the copper and solder. The efficacy of barrier layer as a barrier to diffusion is tested in the intermetallics analysis and solder ball pull/shear tests. Future data on the efficacy of the barrier layer as an inhibitor to diffusion between the copper and gold before the soldering process is due to be published in subsequent papers. The insertion loss testing determines if there is any insertion loss due to the barrier layer with gold. With these tests, the efficacy of barrier layer, and by extension the Ni-less surface finish as a whole, is thoroughly tested in this paper.

Solder Joint Strength Tests

The solder joint strength tests were intended to greatly stress and age the solder joints in order to mimic the worst possible scenario, under which the assembly with these joints was used extensively and in unusually poor conditions. The PCBs had solder balls applied and then were put through 1, 3, and 6 lead-free reflow cycles at 260°C. Then the samples were aged in heat storage at 150°C for either 500 or 1000 hours to mimic use over the lifetime of an assembly including these solder joints [10]. After the reflow cycles and aging, the PCBs were divided into two groups: intermetallics analysis samples and solder ball pull and shear test samples.

The intermetallics analysis samples were cross-sectioned, and the width of the intermetallics measured. In order to see the largest possible intermetallic layers, only samples that had gone through 6 reflow cycles and 500 and 1000 hours of heat storage at 150°C were cross-sectioned. The intermetallic layers in solder balls are weaker than the surrounding copper and tin of the assembly, so the width of these layers needs to be minimized in order to create strong solder joints [11]. In Ni-less surface finishes, the intermetallics are Cu₃Sn and Cu₅Sn₆ [11]. After the total width of the combined Cu₃Sn and Cu₅Sn₆ intermetallics was measured, the value was compared with previously published data on the intermetallics of Direct Immersion Gold (DIG) and Electroless Palladium Immersion/Autocatalytic Gold (EPIG/EPAG). The comparisons were conducted to see if the barrier layer was

performing as a barrier to interdiffusion between tin (solder) and copper, which is what creates intermetallics. The data on the Ni-less surface finish was compared to DIG in order to see how the intermetallics of samples with the barrier layer compared to intermetallics with no barrier layer, since DIG is gold directly onto copper. Ideally, the intermetallics of the samples with barrier layer should result in a smaller intermetallic layer than DIG. Then, the Ni-less surface finish samples were compared to EPIG/EPAG in order to see how the barrier layer inhibits the growth of intermetallics compared to a non-nickel barrier layer (palladium). In this scenario, the width of the intermetallics in the Ni-less surface finish samples should be similar or better than those shown in EPIG/EPAG samples.

The solder ball pull and shear test samples were tested under JEDEC B115 and B117 standards, respectively. In this standard, there are 4 failure modes: mode 1, ductile solder failure, where the tin solder ball stretches and breaks away from the intermetallics (failure of solder ball); mode 2, pad lift or cratering, where the copper pad is removed from the laminate (failure of laminate); mode 3, non-wetting, where the solder ball lifts entirely off of the surface plating due to not being properly soldered in the first place (failure of soldering and/or surface finish cleanliness); and mode 4, brittle intermetallics failure, which is the most important type of failure originating in the choice of surface finish (failure of intermetallics). Failure modes were examined for brittle failure modes. Brittle failure modes (mode 4) are common in solder balls on ENIG surface finish due to the weakness of the phosphorous-rich nickel intermetallics [11], but if the Ni-less surface finish tested in this paper is to be a viable replacement, then the samples need to have an equal or lesser percentage of brittle failures compared to ENIG.

Insertion Loss Tests

Strips of smooth rolled standard ½ oz ED copper were plated with the Ni-less surface finish and tested for insertion loss against identical bare copper strips. Since insertion loss is dependent on circuit design [12], both tightly coupled grounded coplanar waveguide (GCPW) circuit and microstrip transmission line circuit designs were tested. The GCPW circuit design results in more of the surface finish being part of the circuit path due to four sidewalls in the design which are plated with the surface finish [12]. The microstrip transmission line design does not have the side walls, so the surface finish contributes less to the insertion loss value [12]. “Tightly coupled” indicates that the sidewalls have a higher current density compared to loosely coupled due to the smaller spacing. The microstrip differential length method of testing was used across a frequency ranging from 0 - 100 GHz to see if the surface finish was acceptable for high-frequency circuit designs.

RESULTS AND DISCUSSION

The following section will move through the data in the following format: 1) intermetallics width comparisons to predict solder joint strength, 2) solder ball pull and shear failure modes to determine the rate of brittle intermetallics

failures, and 3) insertion loss comparison to determine insertion loss compared to bare copper.

Intermetallics: DIG Comparison

This comparison was conducted to see how a sample with the barrier layer compares to samples without any barrier to intermetallic growth.

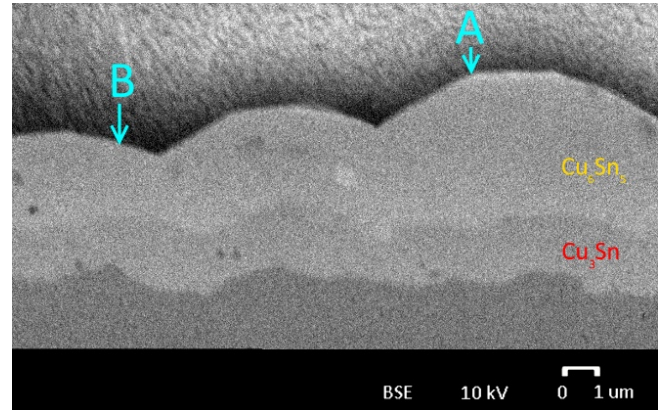


Figure 5. An example of the Ni-less surface finish intermetallics after 6 reflow cycles and 1000 hours of aging.

Table 1. Comparison between previously published data on DIG intermetallics [13] [14] and the Ni-less surface finish intermetallics.

Parameter	Direct Immersion Gold	Ni-less surface finish
Surface Finish Contents	Gold (150-200nm)	Barrier Layer, Gold (50 nm)
Total IMC Thickness Range	~6 – ~11 μm	3.8 (B) – 6.5 (A) μm

The references for DIG surface finishes in Table 1 included different testing parameters, including only 1 or 2 reflow, respectively, on instead of the 6 reflow that the Ni-less surface finish samples were subjected to, and much higher thicknesses of gold. Additionally, the second reference used temperature cycling instead of heat storage, but the first reference used heat storage for 1000 hours at 150°C, the same as the Ni-less surface finish samples.

However, despite the harsher sample preparation for the Ni-less surface finish samples, the results in Table 1 above show that the Ni-less surface finish has consistently smaller intermetallics than the DIG surface finishes. This data is as expected, since the DIG surface finishes have no barrier between the copper and gold to prevent interdiffusion and therefore intermetallic growth. Since the DIG intermetallics are larger than the Ni-less surface finish intermetallics, the solder balls that are on the Ni-less surface finish should be stronger than those on DIG surface finishes.

Intermetallics: EPIG/EPAG Comparison

This comparison was conducted to see how the barrier layer component of the Ni-less surface finish compares to a

barrier layer in a different surface finish, in this case 100nm of palladium in EPIG/EPAG surface finishes.

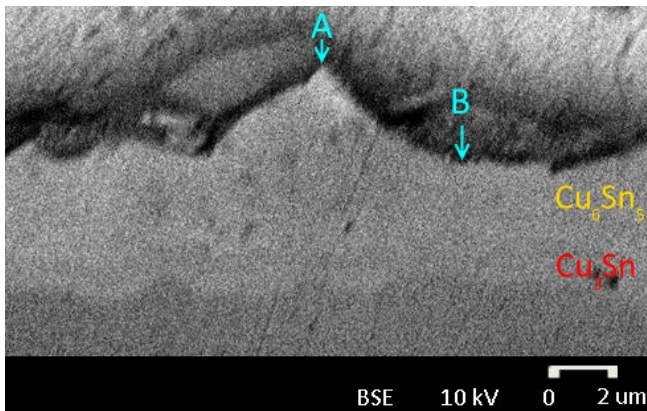


Figure 6. An example of the Ni-less surface finish intermetallics after 6 reflow cycles and 500 hours of aging.

Table 2. Comparison between previously published data on EPIG intermetallics [15] [16] and the Ni-less surface finish.

Parameter	EPIG/EPAG	Nickel-less surface finish
Surface Finish Contents	Palladium (100 nm), Gold (100nm)	Barrier Layer, Gold (50 nm)
Total IMC Thickness Range	~3 – ~10 μm	1.7 (B) – 3.2 (A) μm

The references for the EPIG/EPAG surface finishes in Table 2 differ slightly in sample preparation, with one of the references only using 300 hours of heat storage instead of 500 hours like the Ni-less surface finish samples and the other EPAG reference. Additionally, both of the EPIG/EPAG references only subjected the samples to 1 reflow cycle, compared with the 6 reflow cycles of the Ni-less surface finish samples. Both EPIG/EPAG references used 100nm of palladium and 100 nm of gold.

Despite the harsher sample preparation for the Ni-less surface finish samples, the results show that the Ni-less surface finish had consistently smaller intermetallics than the EPIG/EPAG surface finishes. This shows that the barrier layer in the Ni-less surface finish performs better than 100nm of palladium in inhibiting intermetallics growth. Since the EPIG/EPAG intermetallics are larger than the Ni-less surface finish intermetallics, the solder balls that are on the Ni-less surface finish should be stronger than those on EPIG/EPAG surface finish.

In conclusion, the Ni-less surface finish with the nano-engineered barrier layer served to better inhibit intermetallic growth compared to not having a barrier between gold and copper (DIG) and having a 100 nm palladium barrier between gold and copper (EPIG/EPAG). The smaller intermetallic areas in solder balls on the Ni-less surface finish should result in strong solder joints, which was tested in the next section.

Solder Joint Strength: Solder Ball Pull Test

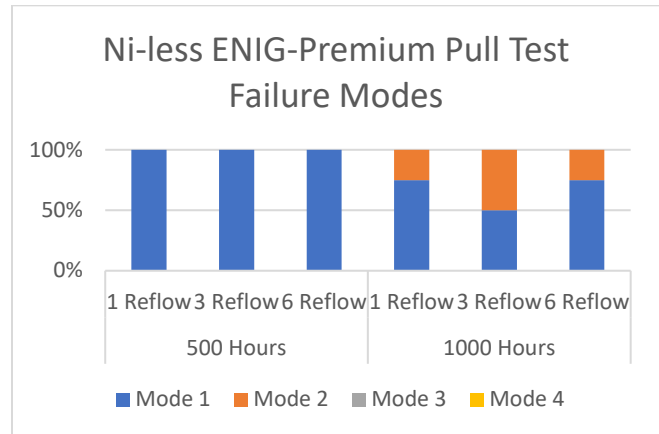


Figure 7. Failure modes during pull tests on solder balls on the Ni-less surface finish for 1, 3, and 6 reflow cycles and 500 and 1000 hours of aging.

The chart above shows the different types of failure modes during pull tests on solder balls on the Ni-less surface finish. The only types of failure modes seen are mode 1, ductile solder ball failure, and mode 2, pad lifting, which are issues with the solder and laminate, respectively. There are no failures surrounding the surface finish in these samples.

Solder Joint Strength: Solder Ball Shear Test

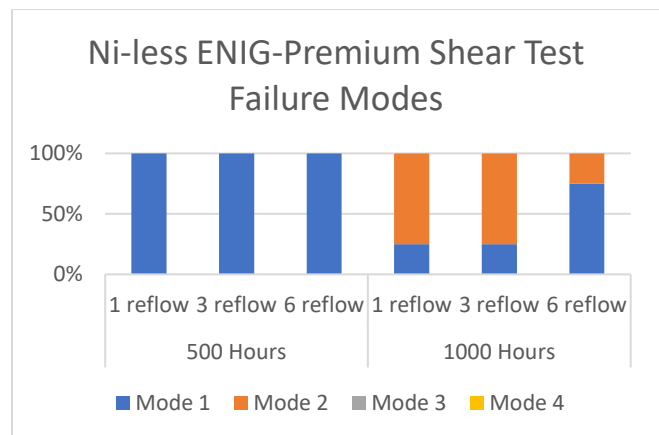


Figure 8. Failure modes during shear tests on solder balls on the Ni-less surface finish for 1, 3, and 6 reflow cycles and 500 and 1000 hours of aging.

The chart above shows the different types of failure modes during shear tests on solder balls the Ni-less surface finish. The only types of failure modes seen are mode 1, ductile solder ball failure, and mode 2, pad lifting, which are again issues with the solder and laminate, respectively. In this testing type, there are also no failures surrounding the surface finish in these samples.

In conclusion, both solder ball pull and shear tests showed no failures related to the surface finish, so the strong intermetallics predicted by the smaller intermetallics seen in the previous sections are proven true. Since there are no

brittle intermetallics failures, the Ni-less surface finish creates a stronger solder joint than ENIG.

Insertion Loss

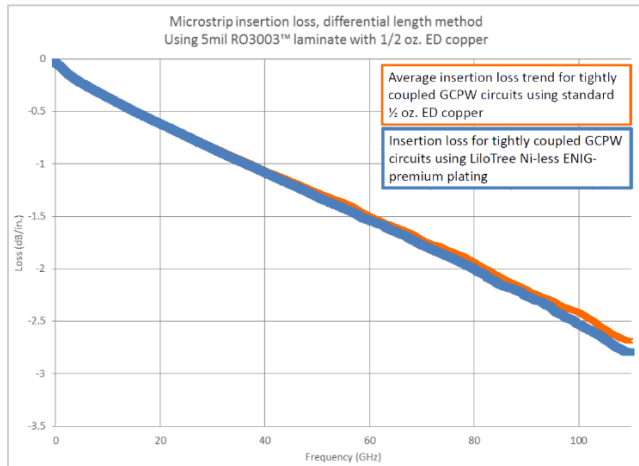


Figure 9 a. Insertion loss of the Ni-less surface finish (blue) compared to bare standard 1/2 oz. ED copper (orange) from 0 – 100 GHz on tightly coupled GCPW circuits.

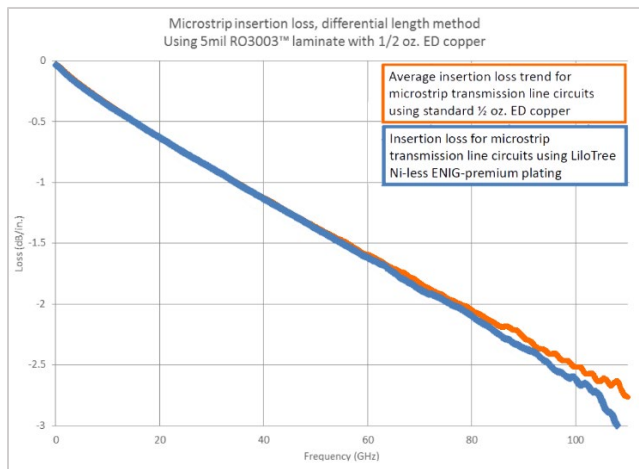


Figure 9 b. Insertion loss of the Ni-less surface finish (blue) compared to bare standard 1/2 oz. ED copper (orange) from 0 – 100 GHz on microstrip transmission circuits.

As shown in the graphs above, the insertion loss of the Ni-less surface finish is almost exactly identical to the insertion loss of bare copper over the 0 – 100 GHz frequency range. This indicates that the Ni-free surface finish is able to be used in high-frequency applications with hardly any insertion loss increase compared to bare copper. The graphs can also be compared to Figure 1, which shows that ENIG has a loss of around 2.75 dB/in at 50GHz, compared to the values shown in these graphs, about 1.25 dB/in at 50GHz – more than a 50% decrease in insertion loss. Since the Ni-less surface finish has such a small difference in insertion loss compared to bare copper, especially when contrasted with ENIG insertion loss, the Ni-less surface finish solution is a good surface finish for high-frequency applications.

CONCLUSIONS

The Ni-less surface finish of cyanide-free immersion gold plated onto a nano-engineered barrier layer on top of copper is a viable solution for high-frequency applications. The surface finish was tested for intermetallic growth, solder ball brittle failures, and insertion loss. The results showed that this surface finish performs better than other currently available Ni-free surface finishes, such as DIG and EPIG/EPAG, due to its smaller intermetallics, lack of brittle solder joint failures, and extremely low insertion loss compared to bare copper. This Ni-less surface finish with nano-engineered barrier layer is a good solution to the current need for a reliable surface finish for high-frequency PCB applications.

ACKNOWLEDGEMENTS

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REFERENCES

- [1] D. Cullen, "Effects of Surface Finish on High Frequency Signal Loss Using Various Substrate Materials," in *IPC APEX EXPO Conference Proceedings*, 2001.
- [2] X. Wu, "Surface Finish Effects on High-Speed Signal Degradation," *IEEE Transactions on Advanced Packaging*, pp. Vol 31, No 1, 2008.
- [3] J. Coonrod, "The Effects of PCB Fabrication on High-Frequency Electrical Performance," in *IPC APEX EXPO Conference Proceedings*, 2016.
- [4] J. Coonrod, "Ambiguous influences affecting insertion loss of microwave printer circuit boards," *IEEE Microwave Magazine*, pp. Vol 13, No 5, 2012.
- [5] Y. Tao, "Revisit Nickel Characterization Effect on High-Speed Interconnect Performance," in *IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO)*, 2015.
- [6] T. Fisher, "How Are 4G and 5G Different?," 3 July 2019. [Online]. Available: <https://www.lifewire.com/5g-vs-4g-4156322>. [Accessed 11 July 2019].
- [7] T. Abbas, "Propagation Channel Characterization for 28 and 73 GHz Millimeter-Wave 5G Frequency Band," in *IEEE 15th Student Conference on Research and Development (SCORED)*, 2017.
- [8] T. Gu, "High-Frequency, High-Speed: an Opportunity for China CCLs to Lead," 24 July 2017. [Online]. Available: <http://pcb.icconnect007.com/index.php/article/105450/high-frequency-high-speed-an-opportunity-for-china-ccls-to-lead/105453/?skin=pcb>.
- [9] J. Ding, "The future development trend of PCB & Flexible PCB industry," 4 June 2018. [Online]. Available: <https://www.linkedin.com/pulse/future-development-trend-pcb-flexible-industry-jessie-ding>.

- [10] D. Collins, "Accelerated Test Methods for Reliability Prediction," Los Alamos National Laboratory Associate Directorate for Theory, Simulation, and Computation (ADTSC).
- [11] A. Olson, "What are Intermetallics and How Can We Overcome the Failures Associated With Them?," [Online]. Available: <http://www.tch.es/wp-content/uploads/Intermetallics.pdf>. [Accessed 11 July 2019].
- [12] J. Coonrod, "Insertion Loss Performance Differences Due to Plated Finish and Different Circuit Structures," in *IPC APEX EXPO*, 2019.
- [13] G. Milad and D. Gudczaskas, "Solder Joint reliability of Gold Surface Finishes (ENIG, ENEPIG, and DIG) for PWB Assembled with Lead Free SAC Alloy," Uyumura International Corporation, Southington, CT.
- [14] D. Kim, "Evaluation of DIG (Direct Immersion Gold) as a New Surface Finish for Mobile Applications," Intel Corporation, Folsom, CA, 2005.
- [15] G. Milad and D. Gudczaskas, "Characteristics of EPIG Deposits for Fine Line Applications," Uyumura International Corporation, Southington, CT.
- [16] T.-C. Huang and M. Tomic, "Scaling Cu pillars to 20um pitch and below: critical role of surface finish and barrier layers," in *IEEE 67th Electronic Components and Technology Conference*, 2017.