CR-5000

Realistic Implementation of Signal Integrity Screening – Guidelines for PCB Designers

WHITE PAPER

This white paper article looks at each of the roles of the engineer and PCB designer, considers the traditional design process, and makes suggestions on how the designer can contribute significantly to improving a design's overall signal integrity while simultaneously saving time so that the engineer can focus on more in-depth issues.

Pick up any PCB or electronics design magazine and probably at least one article will be devoted to some aspect of high-speed digital design; be it routing techniques, signal integrity analysis, electromagnetic compatibility or power integrity. This has now become a mainstream design practice. Being able to achieve successful designs repeatedly suggests that a honed process is in place – one that captures electrical intent, enables design realization, and promotes verification, to ensure that the product delivered matches the requirements and specifications. However, having in place such a formal process is often more an ideal than a reality.

Realizing products with significant high-speed digital content requires the electrical engineer to operate in different specialties. Besides performing circuit design, the engineer needs to evaluate the design's signal integrity, apply mitigation techniques, and all while keeping in mind the physical limitations of the board. The time he or she can devote to such activities is usually a fraction of the overall design time, with the majority being spent on researching parts, attending design reviews, testing the design in the lab, and participating in numerous meetings. This also usually means that an in-depth, post-layout analysis of the product is compromised.
So what can be done to improve the situation?

Context

The PCB designer works closely with the engineer and is also schedule-constrained. The designer's role is to physically realize the design as outlined by the engineer vis-à-vis constraints as quickly as is possible. Because the engineer often has to manage a constant stream of changes, in turn the PCB designer has to be patient and implement these at whatever point in the design process they are required. Traditionally, the main urgency to complete the layout is to obtain a prototype so that the engineer can test the product in the lab – getting to this stage is often set as a design process milestone.

What is Signal Integrity (SI)?

For many board and system designers, Signal Integrity (SI) is a relatively new concept to take into account. It is the result of the interaction between the distributed capacitance, inductance and resistance on the circuit board and the integrated circuits.

This can mean having to use microwave transmission line theory on the digital designs, but in a different way to the traditional domains of radio and radar. The key factor is controlling the track features on a PCB to ensure that the signal distortion and the time taken for a signal to travel from one chip to another (called the flight-time) is within defined limits.

However, gaining access to probe signals in today's high-speed designs can be difficult, due to component packaging. One option to help mitigate this issue is to have a signal integrity (SI) analysis tool in the design environment.

Yet, having access to an SI analysis tool versus implementing the practice of SI analysis as part of the design process are two entirely different states. Further, performing SI analysis has been perceived historically as a black art, requiring specialist knowledge and skill set. Some companies even have an entire group dedicated to performing this task. The traditional design schedule does not promote this activity and to incorporate it now into the schedule does not remove the need for examining the product in the lab. Consequently, the perception could be that adding SI analysis to the design process gives the electrical engineer another job to do, in addition to their already long list of actions. But this can be perceived as a somewhat limited view as the benefits of addressing signal integrity up front can be vast, both in time and money savings – enabling the design team to deliver boards that are going to be right-first-time.

PCB designer best positioned to resolve SI issues early

In traditional-style development organizations, the engineer does not look at SI issues until the board is completely placed and routed. Any issues the engineer finds are flagged and sent back to the designer. In order to complete the design, several iterations of this SI review cycle may occur.

However, if the design environment includes a PCB design tool that incorporates constraint management with the ability to analyze signal integrity, as in the case of Zuken's **CR-5000 Lightning** Realize solution, the PCB designer becomes the person best positioned to improve a design from a high-speed design standpoint; as part of the layout process, the designer can perform first-pass signal integrity checking. Through this SI screening, the designer makes the design process more efficient by greatly reducing the number of SI review cycles, thereby saving time and money.

The advanced capabilities of today's design tools that are available to the PCB designer mean that in one application, the designer can realize the placement and routing as guided by physical and electrical rules (constraints) and then screen for crosstalk and signal quality without needing a deep understanding of electrical theory. Solutions such as **CR-5000 Lightning** from Zuken are so sophisticated that the designer can effectively resolve some lesser issues that were once only solvable by the engineer, therefore reducing the number of actions on the engineer's to-do list.

Since **CR-5000 Lightning** is such a powerful environment, the PCB designer is able to perform signal integrity screening as a fluid part of the PCB design process. Issues are presented in a spreadsheet alongside corresponding constraints, and crosstalk hotspots can be highlighted on the PCB design canvas. The designer can then resolve these issues by manual or automated means. In this preliminary look at signal integrity, there is no need to involve the engineer.

Why would the PCB designer take on this task of signal integrity screening?

Clearly, we are adding to the designer's already compressed schedule.

However, when proposing this action to designers, some have actively told us that they want to increase their value in the design process. Others desire a better understanding of the effects of their routing choices, and a few totally embraced the idea on its own merits – the overall time and money savings for the organization. Again, PCB designers are best positioned to perform the signal integrity screening, as they are the most intimate with the physical realization, knowing which signal names correspond to which traces. They already have the design environment open and therefore the screening activity simply becomes an extension of what they are already doing – realizing the PCB.

If design tools are so sophisticated in realizing electrical design intent, why would screening need to take place at all?

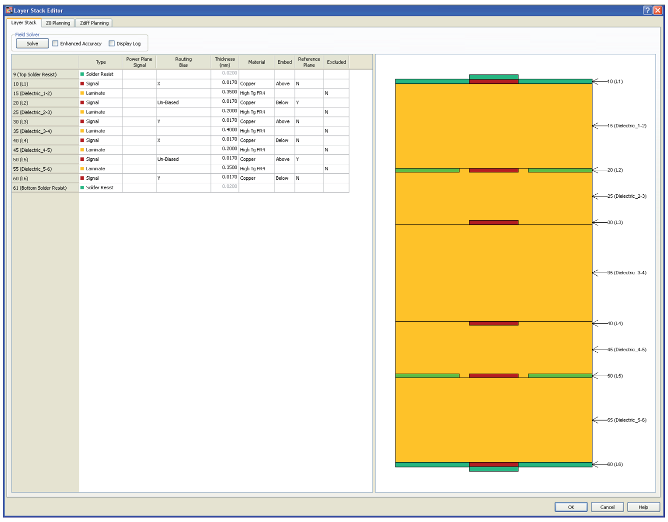
For crosstalk or multi-drop nets with min/max delays (as opposed to lengths), often it is easier to route nets first without considering constraints and then resolve issues using manual or automated methods. Resolving min/max delay issues requires multiple passes. For the first pass, a faster calculation mode is used to check delay of each branch. Then at screening time, actual simulation is used to incorporate all of the reflections and logic low and high voltage levels. Screening for overshoot is best performed after placement. At this stage, the design is returned to the engineer with nets flagged that require termination. Therefore, signal integrity screening is really a continual process throughout the board layout phase.

PCB designer SI Screening Steps

Let us get specific about the PCB designer's actions when performing signal integrity screening using Zuken's **CR-5000 Lightning** solution as an example.

Confirm Board Stackup

A first step for the designer is to confirm the board stackup, ensuring that the materials, thicknesses, and reference planes are correctly established. With this in hand, the designer creates a field solution so that crosstalk and delays can be calculated. In addition, the designer can assess the characteristic impedance for a set of trace widths or conversely, calculate a set of trace widths based upon a specified impedance. A similar process applies to differential signaling, where the variables are trace width, trace-to-trace spacing, and differential impedance.



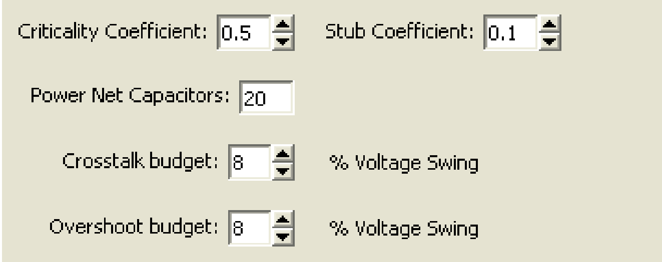
Screenshot of the stackup editor

Set up Simulation Models

Ideally, the engineer has assembled SI models for the design that were used when he or she experimented with signaling scenarios prior to schematic capture. In this case, assigning models is straightforward. If this is not the case, the designer can specify driver/receiver models that are appropriate for the technology being used.

Assess Constraints

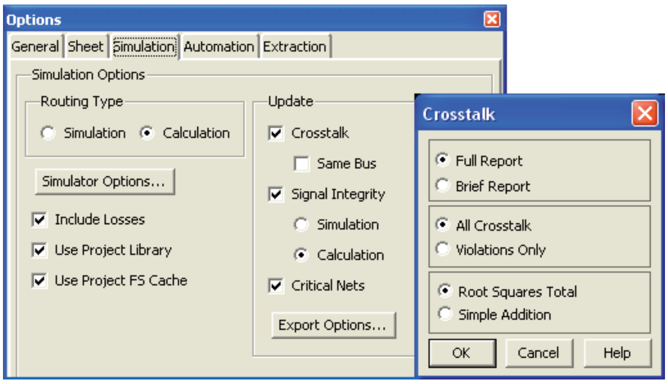
Next, the designer assesses constraints. Ideally, the engineer has captured the design's electrical intent (mV of crosstalk and ps of delay) directly within CR-5000 Lightning. In contrast, it may be that the engineer has communicated requirements in documentation; it may be incumbent upon the designer to enter them. In the absence of specified constraints, for the purposes of SI screening the designer can constrain the design automatically for crosstalk, overshoot, and stub length based on the rise time of the SI models.



Configure Automatic Constraint Assignment

Configure Analysis and Checking

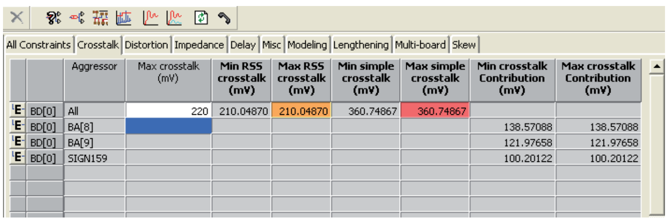
At this point, the designer configures how the tool will behave when screening is performed. The default settings are shown below. However, if the designer also wants to assess overshoot, the button for Simulation under Signal Integrity would need to be selected. In the Physical Editor, the designer specifies how crosstalk will be reported when checking is performed.



Configure Analysis and Crosstalk Checking

Perform Screening and Review the Results in Constraint Manager

After the board has been placed and there is routing to evaluate, the designer starts the screening process. Results are shown in the spreadsheet-based presentation of the Constraint Manager. To investigate a net of interest, the designer uses the "Update Selected" command. If the designer chooses many nets to review, the color-coded results make it easy to see which nets are in compliance (color green), close to violation (orange) or exceeding the constraint (red). In the crosstalk case, shown below, the contribution of the primary aggressors is included.



Crosstalk

If desired, the designer can check distortion, as shown here:

All Constraints | Crosstalk | Distortion | Impedance | Delay | Misc | Modeling | Lengthening | Multi-board | Skew | Routing

	Max overshoot (mV)	1st Overshoot (Rising Edge) (mV)	Overshoot (Rising Edge) (mV)	1st Undershoot (Rising Edge) (mV)	Undershoot (Rising Edge) (mV)	1st Overshoot (Falling Edge) (mV)	Overshoot (Falling Edge) (mV)	1st Undershoot (Falling Edge) (mV)
E LB_LA30	750	1377	1377	712	712	1598	1598	908

Disortion

Further, the designer can check the impedance of a net based on the layers it traverses.

All Constraints | Crosstalk | Distortion | Impedance | Delay | Misc | Modeling | Lengthening | Multi-board | Skew | Routing

	Layer	Impedance Template	Min Zo (Ohm)	Max Zo (Ohm)	Min Zo (Ohm)	Max Zo (Ohm)	Min track width (mm)	Max track width (mm)
E LB_LA30	All		70	85	74	87	0.10000	0.20000
E LB_LA30	L1		70	85	87	87	0.20000	0.20000
E LB_LA30	L3		70	85	74	74	0.10000	0.10000
E LB_LA30	L4		70	85	74	74	0.10000	0.10000

Impedance

Finally, the designer can check delays.

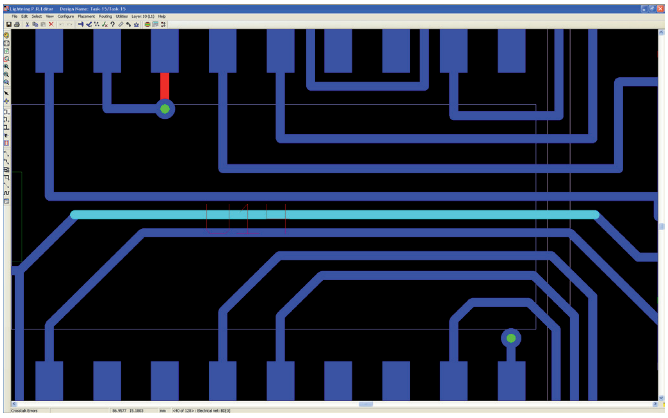
All Constraints | Crosstalk | Distortion | Impedance | Delay | Misc | Modeling | Lengthening | Multi-board | Skew | Routing

	Min delay (ps)	Max delay (ps)	Max skew (ps)	Min relative delay (ps)	Max relative delay (ps)	Min Typical Flight Time (Rise) (ps)	Max Typical Flight Time (Rise) (ps)	Typical Flight Time (Rise) (ps)	Min Typical Flight Time (Fall) (ps)	Max Typical Flight Time (Fall) (ps)	Typical Flight Time (Fall) (ps)	Max skew (ps)
E MCLK1	400	720	200			383	705		633	870		322

Delay

Perform Checking and Review the Results in the Physical Editor

The designer may choose to review the design on the board itself. To do so, the designer checks the nets or the entire board for crosstalk, and then locates the crosstalk with an interactive command that steps through each crosstalk victim. Here is the display that the designer sees:



Interactive Locating of Crosstalk Victims

Resolve Issues and Send Design to the Engineer for Deeper Review

As issues are found, the designer should resolve them, if possible. When the designer saves the design, any color-coded results will persist in the Constraint Manager window for the engineer to examine more closely.

Conclusion

The practice of creating a high-speed digital design requires that both agents, the electrical engineer and the PCB designer, work even more closely. The engineer needs to delve into matters that have typically concerned only the designer, such as stackup, trace widths, and spacings, in order to yield the desired characteristic single-ended and differential pair impedances. The designer needs to understand that routing for delay is different from routing for length and that signals with faster edge rates create more crosstalk than those with slower edge rates. With that in mind and armed with the proper tools, the designer who performs signal integrity screening during layout significantly improves the overall design process. The designer addresses simple SI issues earlier, freeing up the engineer to focus on tougher problems. This practice can minimize the need for rework and reduce the number of large SI review cycles needed. All of this means that the product can be delivered earlier with higher quality, thereby saving time and money.

For more information about Zuken and their solutions visit www.zuken.com

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