TEMPERATURE CYCLING AND FATIGUE IN ELECTRONICS

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ABSTRACT

The majority of electronic failures occur due to thermally induced stresses and strains caused by excessive differences in coefficients of thermal expansion (CTE) across materials.

CTE mismatches occur in both 1st and 2nd level interconnects in electronics assemblies. 1st level interconnects connect the die to a substrate. This substrate can be underfilled so there are both global and local CTE mismatches to consider. 2nd level interconnects connect the substrate, or package, to the printed circuit board (PCB). This would be considered a "board level" CTE mismatch. Several stress and strain mitigation techniques exist including the use of conformal coating.

Key words: temperature cycling, thermal cycling, fatigue, reliability, solder joint reliability.

INTRODUCTION

The excessive difference in coefficients of thermal expansion between the components and the printed board cause a large enough strain in solder and embedded copper structures to induce a fatigue failure mode. This paper discusses the solder fatigue failure mechanism and the associated PTH (plated through hole) fatigue failure. The solder fatigue failure is more complicated due to the many solder materials and different solder shapes. Figure 1 shows an example of a solder fatigue failure in a cross section of a ball grid array (BGA) solder ball with the corresponding finite element model. The predicted location of maximum strain corresponds to the same location of solder fatigue crack initiation.

DISCUSSION

CTE Mismatch

Any time two different materials are connected to one another in electronics assemblies, there is a potential for CTE mismatch to occur. Some of these CTE mismatch interactions can be quite complicated due to the changing properties of materials, complex geometries, and competing material behaviors. For example, the 1st level interconnects called C4 "bumps" connect a flip chip die to a substrate. Many assembly options exist that affect the solder fatigue behavior including use of underfill, corner depopulation and solder mask geometry. Both the global CTE mismatch between the die and substrate need to be considered as well as the local CTE mismatch between the underfill and C4 solder bump. This failure mode is part of the "package level" reliability prediction and is separate from "board level" reliability.

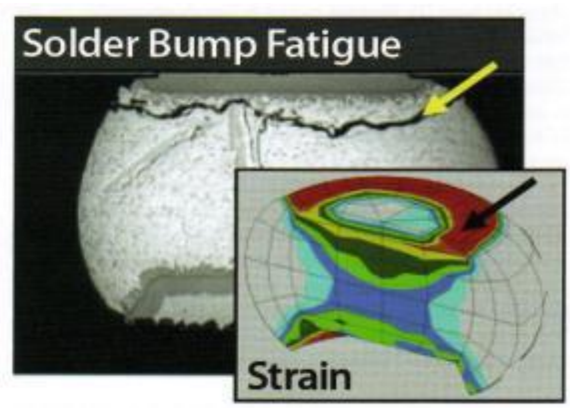

Figure 1 BGA Solder Ball Fatigue and FEA Fracture Model

All the packages, components or structures that are soldered directly to the board can be considered 2nd level interconnects. In the BGA example discussed previously, this would relate to the C5 "balls" that connect the bottom of the substrate to the printed circuit board (PCB). Here too, board level reliability predictions are complicated by mitigation techniques, use of conformal coatings and heat sinks, etc. While BGAs are some of the more complicated components that can suffer from solder fatigue, other components that are much simpler are not immune.

The simplest form of CTE mismatch can be considered in order to illustrate the effect on solder fatigue. In Figure 2, the component is connected to the board with two solder joints. The component and the board are infinitely rigid, the solder joins are symmetric to the component and the CTE of the board is larger than that of the component. In the stress free or "neutral" state, the solder joint is not subjected to any strain. If the temperature is elevated from the neutral state, then the board (higher CTE) will expand more than the component (lower CTE) and the solder joints will have a strain applied to them. If the temperature is decreased from the neutral state, then the board will contract more than the component and the solder joints will again have a strain applied to them. It is clear that any time the temperature changes, the solder joints are stretched one way or another. The neutral point remains at the line of symmetry of the component. The distance from the neutral point to the solder joint is called the "distance to neutral point" (DNP). For most situations, the global CTE mismatch will have a larger effect on components with larger DNP.

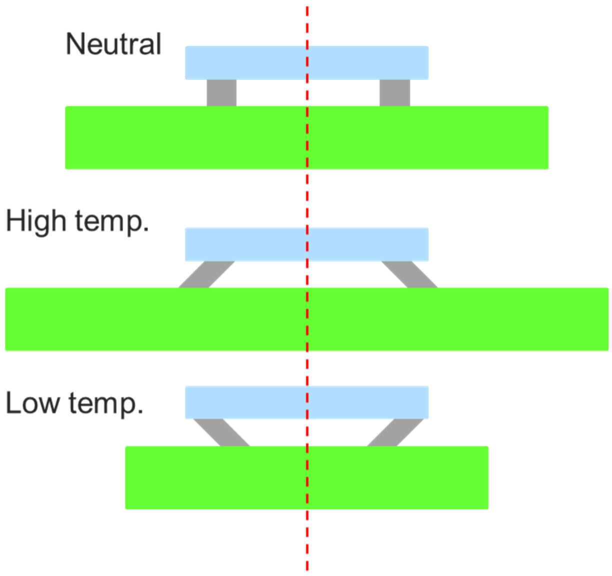

Figure 2 Effect of CTE Mismatch on Solder Joint Strain

Field Conditions

Figure 2 shows that *temperature changes*, not just component shapes or quality, in electronics assemblies are a critical part of the fatigue prediction. To understand the types of loads that an assembly might go through in its intended life, consider the various temperature cycles seen in the field. Field conditions vary widely for different usage and applications even for the same product. Each unique industry segment has a characteristic service life and usage conditions with some examples shown in Table 1.

	Temp range	Cycles/year	Service time	Failure rate
Consumer	0 to 60 °C	365	1 year	1 %
Computer	15 to 60 °C	1460	5 years	0.1 %
Telecom	-40 to 85 °C	365	7 to 20 years	0.01 %
Aircraft	-55 to 95 °C	365	20 years	0.001 %
Automotive	-55 to 95 °C	100	10 years	0.1 %

Table 1 Field Conditions for Various Industries

The list in this table is far from comprehensive but gives insight into the need for understanding the use environment. Specific applications should have detailed specifications. In some products, there will also be different requirements for different life cycle phases. Life cycle phases include validation testing, manufacturing, shipping, storage, usage, and service. The acceptable failure rates in each industry segment also vary widely and require significant differences in product design. It is also possible that in the same product there will be electronics assemblies with different thermal loads. For example, in LCD touch panels, the voltage regulators and networking modules can be at different temperatures at the same time. In some cases, it is possible for special field conditions to exist. Some products, such as smart munitions, launch platforms, AEDs and airbags, experience long periods in storage followed by short periods of usage. In these products, the majority of product life is spent in an inactive state punctuated by short usage periods of critical importance. The electronics need to survive for many years and be reliable at the end. A good design considers all the life phases of the product including test, transportation and storage, not just the use stage, since the failure modes and stressors are different.

Accelerated Life Tests

Testing an electronics assembly for 20 years at one cycle/day is prohibitively expensive. A better approach is to validate the product reliability in some way as early as possible in the design phase. The life test time can be reduced from several years to several weeks or even days. For example, a product that experiences one cycle per day for 1000 days can be tested in six weeks using 15 minute ramps and 15 minute dwells to achieve 24/cycles per day. Life tests can also be accelerated by applying stresses that are beyond normal operation while maintaining the same dominant failure mode. The elevated stress can be achieved by applying a higher temperature and higher load. There are some limitations to how much a life test can be accelerated because competing failure modes can exist in an assembly. Accelerating the test can result in the appearance of different failure modes. However, an accelerated life test may be valid even if another failure mode appears side by side with the desired one.

Table 2 shows an example of JEDEC standard JESD47G Stress-Test-Driven Qualification of Integrated Circuits where equivalent conditions far exceed the actual use conditions. This is for nonhermetic package temperature cycling requirements. For purposes of this standard, solder joint life is well modeled by a Coffin-Manson relation of ΔT^n where n=2.The temperature cycling requirements have been normalized to the historical requirement of 500 cycles of Condition C using the n=2 factor.

The table illustrates how different ranges of increased ΔT can be used to accelerate testing of actual use conditions. Test conditions representative of the field environment are modeled using an acceleration factor derived using physics of failure techniques.

Use Condition	Use Condition Requirement	Equivalent Condition B -55 °C to +125 °C 700 cycles	Equivalent Condition G -40 °C to +125 °C 850 cycles	Equivalent Condition J 0 °C to +100 °C 2300 cycles
Desktop 5 yr Life	ΔT 40 °C 2000 cy	14,175 cy (12,475 cy)* (11,057 cy)**	14,463 cy (12,761 cy)* (11,332 cy)**	14,375 cy (12,675 cy)* (11,250 cy)**
Mobile 4 yr Life	ΔT 15 °C 1500 cy	100,800 cy	102,850 cy	102,221 cy
Server 11 yr Life	ΔT 40 °C 44 cy	14,175 cy	14,463 cy	14,375 cy
Telecom (uncontrolled) / Avionics Controlled 15 yr Life	ΔT 25 °C 5500 cy	36,288 cy	37,026 cy	36,800 cy
Telecom (controlled) 15 yr Life	ΔT 6 °C 5500 cy	630,000 cy	642,812 cy	638,889 cy
Networking 10 year Life	ΔT 30 °C 3000 cy	25,200 cy	25,712 cy	25,557 cy

Table 2 JESD47G Conditions Used in Accelerated Tests
***JESD94, Table 1, Consider desktop with add'l ΔT 8 °C for 31,025 cycles and ΔT 20 °C for 1828 cycles**
**** Consider Desktop with additional ΔT 10 °C for 50,000 cycles**

There are limits on how much a temperature cycle can be accelerated. These limits can be related to melting temperature of the solder alloy, glass transition temperatures of the laminate, use of underfill and others. Performing accelerated life tests can add complications and may require additional steps to validate that the failure mode in the accelerated test is the same as that found in the actual usage condition.

Controlling the Coefficient of Thermal Expansion

The designer or end user has little influence over the component properties because component packaging is typically driven by package level reliability. Complex components need to pass package level qualification tests and there are also a limited number of options for materials at the component level. It is far more common that a board designer can control the PCB properties including glass style, laminate type, copper thickness and board thickness.

Copper has a CTE of approximately 17.6 ppm/°C. Components connected to the PCB have a wide range of effective CTEs. The prevalence of leadless packages with stiffer leads means that more components are susceptible to CTE mismatch problems. There are also an increasing number of larger packages that have an ever larger CTE mismatch effect. In general, the CTE of laminates is decreasing, but PCB laminate manufacturers do not make it easy to determine the true CTE of their laminate. Furthermore, low CTE laminates have their own set of problems and there is a tradeoff between low CTE and cost.

As CTE decreases, both modulus of elasticity and materials costs increase. Increasing modulus results in a more brittle laminate which can result in flexural and drilling challenges.

A realistic target for board level in CTE is between 15 and 17 ppm/°C. Most laminate suppliers only provide CTE values for the in-plane direction as shown in Table 3.

370HR	
Property	Typical Value
Glass Transition Temperature (Tg) by DSC, spec minimum	180
CTE, Z Axis Pre-Tg	45
CTE, Z Axis Post-Tg	230
CTE, X, Y Axes Pre-Tg	13-14
CTE, X, Y Axes Post-Tg	14-17

Table 3 Laminate Properties Provided by Manufacturer

These values are typical for a low resin content laminate (46%-50% resin content by weight, 7628 glass style); however, many popular laminates have much higher resin contents. Higher resin content corresponds to a higher CTE and a lower modulus of elasticity. It is possible to calculate the laminate modulus by taking the resin modulus and adding the glass content in the calculation. FR-4 boards have fibers oriented in both X and Y direction as shown in the Figure 3.

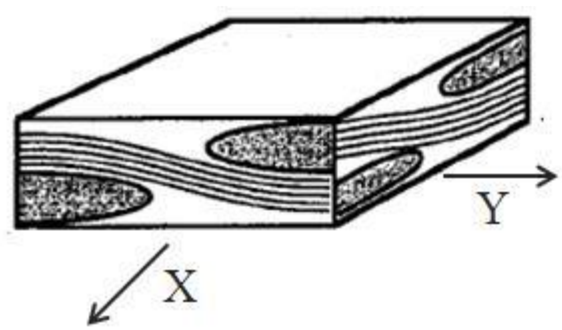

Figure 3 Weave Illustration showing X and Y Fiber Orientation

Then, back calculate the resin modulus (E_m) from the in-plane moduli (E_x and E_y) assuming that half the fibers are oriented in the X direction and half in the Y direction. The in-plane modulus is calculated using Equation 1.

$$E_{x,y} = \frac{V_f E_f}{2} + V_m E_m + \left(\frac{V_f}{2E_f} + \frac{V_m}{E_m} \right)^{-1}$$

Equation 1 In-Plane Modulus Calculation for FR-4 Laminate

Solve for E_m using Equation 2. The positive value for E_m from the equation corresponds to the resin modulus.

$$E_m = \frac{-\left(V_f^{\,2}E_f + 4V_m^{\,2}E_f + 4E_f - 2V_f E_{x,y}\right) \pm \sqrt{\left(V_f^{\,2}E_f + 4V_m^{\,2}E_f + 4E_f - 2V_f E_{x,y}\right)^2 - 4(2V_m V_f)(2\,V_m V_f\,E_f^{\,2} - 4V_m E_f E_{x,y})}}{2(2V_m V_f)}$$

Equation 2 Resin Modulus Value Calculated from In-Plane Modulus Values

These two equations show that the glass style has an effect on the resulting material properties. Consider a variety of glass styles and consider their resin content by weight percent and volume percent as shown in Table 4.

Glass Style	Resin Content [Weight %]	Resin Content [Vol %]
1027	75%	86%
1037	75%	86%
106	72%	84%
1067	71%	84%
1035	70%	83%
1078	68%	82%
1080	64%	79%
1086	63%	78%
2313	57%	74%
2113	55%	72%
2116	54%	71%
3313	54%	71%
3070	50%	68%
1647	48%	66%
1651	48%	66%
2165	48%	66%
2157	48%	66%
7628	48%	64%

Table 4 Glass Styles with Resin Content

Using the previous calculations for each of these glass styles identifies a couple of trends. Modulus decreases and CTE increases as resin content increases, as shown in Figure 4.

Copper content also plays a significant role in PCB properties. The board designer can take the layer stackup with the copper content in each layer and calculate the effective CTE for the board. The original model shown in Figure 2 can be modified to add the board and component properties. These properties can then be used in solder joint fatigue predictions.

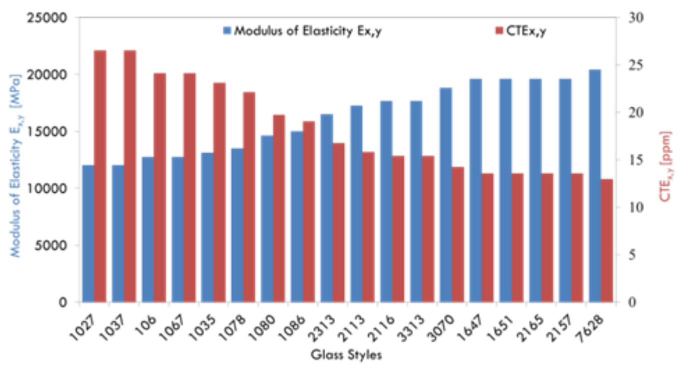

Figure 4 Calculated Moduli and CTEs for Different Glass Styles

Solder Fatigue and Grain Structure

Solder joints are composed of more than solder alone. Solder joints are connected to the PCB via a solder pad that can be made of several alloys and finishes. The component termination can also have different compositions. Once a joint has been formed, the basic construction will have:

1. Base metal at PCB
2. IMC (intermetallic compound) solid solutions between the solder and the PCB base metal
3. Layer of solder that has been depleted due to IMC formation
4. Bulk solder grain structure
5. Layer of solder that has been depleted due to IMC formation
6. IMC solid solutions between the solder and the component base metal
7. Base metal at component termination

Figure 5 shows this composition for BGAs, BTCs (bottom termination components), and other similar structures.

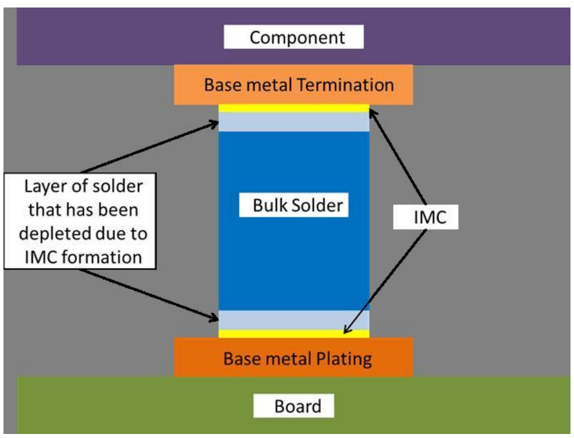

Figure 5 Solder Joint Structure: BGAs, BTCs.

Figure 6 shows a representation of this composition for filleted solder joints.

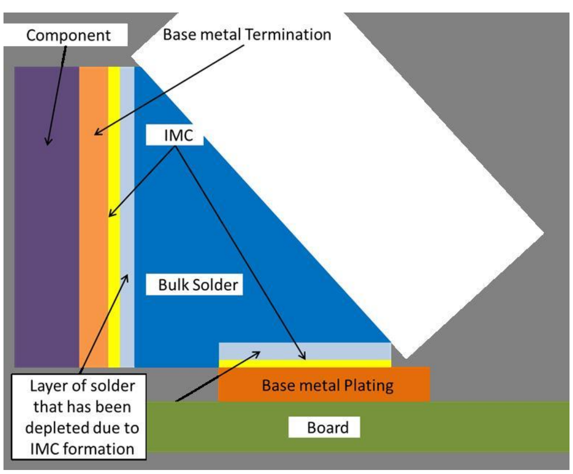

Figure 6 Filleted Solder Joint Structure

Each part of the solder joint is affected by the thermo-mechanical loads in a different way. Solder fatigue in thermal cycling is caused by grain growth. When the solder joint is formed at high temperature, it is in a stress-free state. Some residual stresses build in the solder due to the CTE mismatch as the assembly cools. These residual stresses relax by the creep mechanism. Creep is the tendency of a solid to permanently deform when subjected to a fixed load or the tendency of a solid to relieve stress when loaded at a fixed displacement. The ability to creep typically requires elevated temperature. At higher temperatures, the grains grow faster.

The amount of stress in the solder varies with both the lead style and solder shape. The three types of leads are typically "super compliant", "compliant" and "non-compliant." There is less stress in the solder joint for components with more compliant leads since they have more flexibility. Lead flexibility helps accommodate differences in CTE mismatch. Leadless components can have solder joints with or without fillets. Examples of components with a fillet include chip resistors, chip capacitors, Metal Electrode Face (MELFs) and leadless chip carriers. Examples of components without a fillet include Flip-Chip C4 (Controlled Collapse Chip Connection), BGAs C5 (Controlled Collapse Chip Carrier Connection) and CGA (Column Grid Array). Different surface mount attachment types have significantly different failure modes depending on how the load is distributed within the joint. In the case of uniform load distributions, like in a BGA, the crack formation mechanism is illustrated in Figure 7.

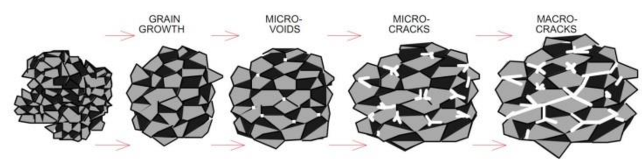

Figure 7 Solder Fatigue Crack Formation in Solder Joints with Uniform Loads

From the original solder joint on the left, the grains grow as the solder joint is stressed. The growing grains cause micro-voids to appear at the grain boundaries. The micro-voids connect with each other to create micro-cracks and eventually macro-cracks. If the load is distributed evenly across the joint, this will happen everywhere at the same time. In BGA balls, this happens in an entire layer of the bulk solder. If the load is not even, then the grain growth and micro cracks are formed in the stress concentration and the micro-crack advances along a crack path.

The speed of crack formation and propagation in the solder can be modeled. One way to predict the solder fatigue is to use a modification of the Engelmaier model. The Engelmaier model is a semi-empirical analytical approach that calculates fatigue using the energy method. Equation 3 gives the calculation to determine the strain range ($\Delta\gamma$) where C is a correction factor (function of activation energy, temperature and dwell time), $\Delta\alpha$ is the CTE difference, h_s is solder joint height (defaults to 0.1016 mm or 5 mils), ΔT is the temperature cycle and L_D is the maximum diagonal distance between solder joints.

$$\Delta\gamma = C\frac{L_D}{h_s}\Delta\alpha\Delta T$$

Equation 3 Strain Gage Equation for Solder Fatigue Model

Next, use Equation 4 to determine the shear force applied to the solder joint. The equation considers the PCB and bond pad stiffness and both shear and axial loads. It also considers the lead stiffness for leaded components. Where F is the shear force L_D is length, E is elastic modulus, A is the area, h is solder thickness, G is shear modulus, and a is edge length of bond pad and the subscripts are: [1] for component, [2] for board, [s] for solder joint, [c] for bond pad, and [b] for board.

$$(\alpha_2-\alpha_1)\cdot\Delta T\cdot L_D = F\cdot\left(\frac{L_D}{E_1A_1}+\frac{L_D}{E_2A_2}+\frac{h_s}{A_sG_s}+\frac{h_c}{A_cG_c}+\left(\frac{2-\nu}{9\cdot G_b a}\right)\right)$$

Equation 4 Equation to Determine Shear Force Applied to the Solder Joint

Using the strain range and shear force, calculate the strain energy dissipated by the solder joint using Equation 5 and calculate the number of cycles-to-failure (N_f), using energy based fatigue models for SAC developed by Ahmer Syed (Amkor technology) or the model for SnPb using Equation 6 or 7.

$$\Delta W = 0.5\cdot\Delta\gamma\cdot\frac{F}{A_s}$$

Equation 5 Strain Energy Dissipated in the Solder Joint

$$N_f = (0.0019\cdot\Delta W)^{-1}$$

Equation 6 Syed Model for SAC Solder Fatigue

$$N_f = (0.0006061\cdot\Delta W)^{-1}$$

Equation 7 Energy-based Fatigue Models for SnPb Solder Fatigue

Using this method allows comparison of the fatigue behavior calculations for an example component. Figure 8 shows the fatigue life of a 2512 Resistor using the different glass styles from Table 4 and two different board thicknesses. The resistor is a low CTE part (alumina, 5.6 ppm/°C) mounted with filleted solder joints. The predicted fatigue life of the component is higher for thinner boards. This highlights why some component manufactures prefer to test on thin laminates.

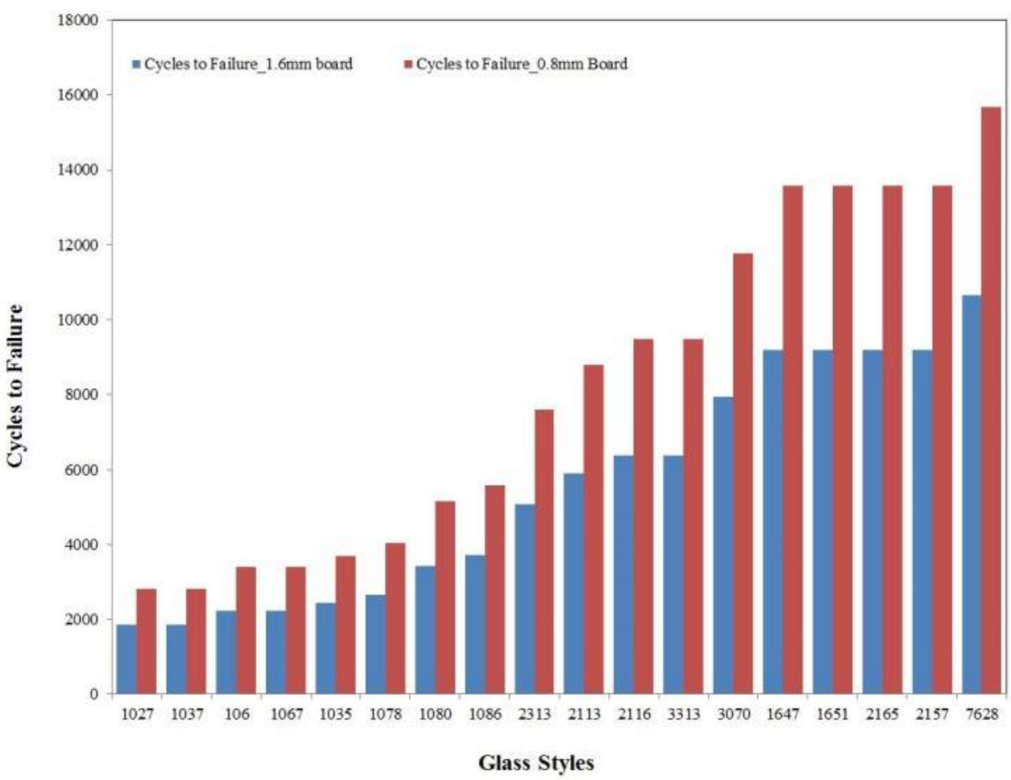

Figure 8 Fatigue Life of a 2512 Resistor Mounted on a PCB with Different Glass Styles & Thicknesses

This method also works to predict the life of leaded components as shown in Figure 9. In this example, TSOP type devices with two different lead alloys (Copper and Alloy 42) were tested to failure. A comparison of the test results is made to the calculated number of cycles to failure.

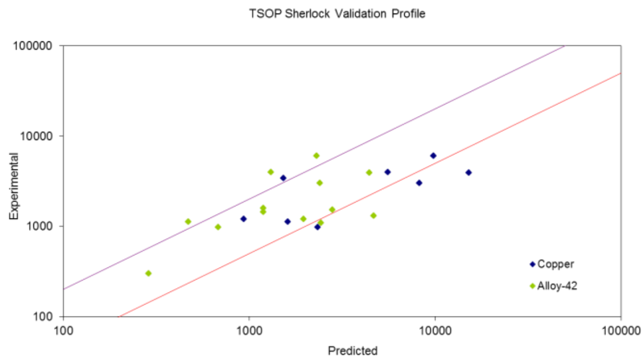

Figure 9 Correlation between Solder Fatigue Model and Experimental Results

It is possible to use analytical energy-based methods to predict some solder fatigue behavior. The solder fatigue model is far from comprehensive though; and, the model does not account for complex mounting conditions such as underfilled components.

SnPb and SAC Solder Alloys

Many solders can be used in electronics today. The two most common alloys have been Tin-Lead (Sn63, Pb37) and Lead-Free (SnAgCu or SAC) solders. Each alloy has different grain structures and different fatigue behavior. Tin Lead solder typically performs better under high stress conditions found in large ceramic devices (stiffer parts) and under large changes in temperature (higher strains). Due to RoHS regulations, most high performance parts are now manufactured with Pb-free alloys. SAC alloys tend to do better for moderate thermal cycles. Figure 10 shows a comparison of SnPb and Pb-free solders for different components.

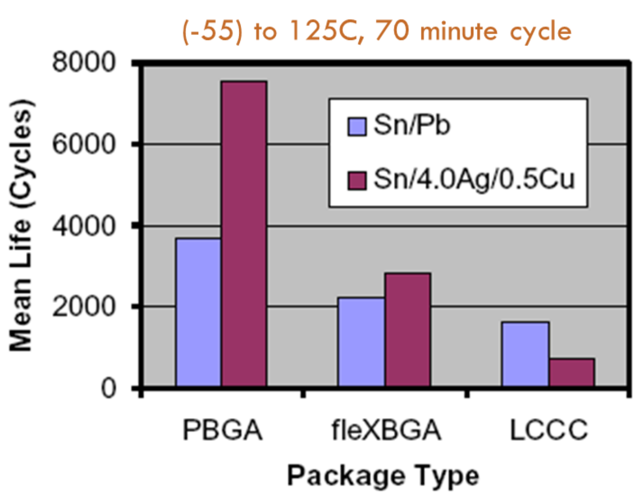

Figure 10 Comparison of SnPb and Pb-free Solder Performance of Three Component Packages

The Pb-free solder performs better than SnPb for the more compliant components. The performance of both solders is decreased for stiffer components; but, the Pb-free solder suffers a larger decrease in life than does the SnPb solder. The dependence of solder performance on the ΔT is not captured in this example since the temperature difference for all three components was from (-55) °C to 125°C. At smaller temperature differences, the Pb-free solder seems better if one looks at the same component with both solder types and varies the ΔT. The next two figures, Figure 11 and Figure 12, show the plot of time to 1% failure of resistors and TSOP devices attached with SnPb solder (shown in red) and two types of Pb-free solders (dashed lines).

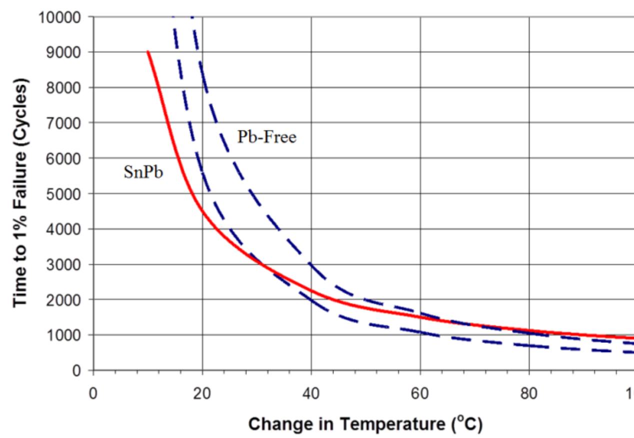

Figure 11 Time to 1% Failure for 2512 Resistors Attached with SAC and SnPb Solder

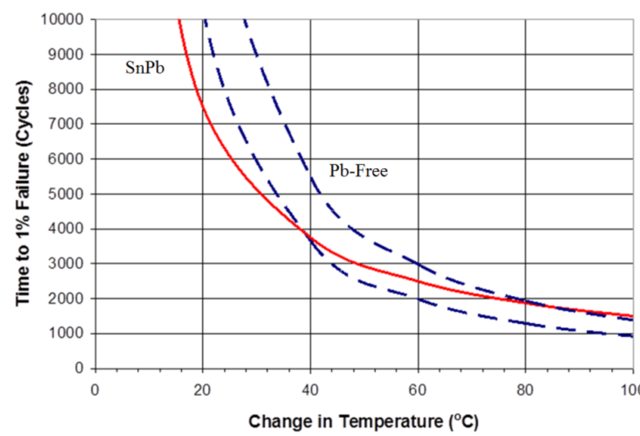

Figure 12 Time to 1% Failure for TSOPs attached with SAC and SnPb with Long Dwells (8 hours)

From Figures 11 and 12, it can be seen that at small changes in temperature SnPb fails first but performs better at higher temperature changes. Longer dwell time allow more stress relaxation of solder and are thought to cause more damage as a result. Longer dwell times at higher temperatures also cause more damage than long dwell times at low temperatures. The solder fatigue failure mode is one of the most dominant ones in electronics. The RoHS legislation and the move to Pb-free solders means that board designers need to plan for solder fatigue during the design phase.

Plated Through Hole Fatigue

Choosing the correct laminate material is critical to the performance of embedded components and not just to the soldered components. The most common embedded component in a PCB is a plated through hole (PTH) or plated through via (PTV). PTHs serve as conductive conduits from one layer of the board to another. They are created by drilling a hole in the board and plating a conductive material inside the hole. There are many combinations of drill diameters, plating thicknesses and materials that can be used in PCBs.

In temperature cycling, the expansion and contraction in the out of plane (z) direction is much higher than that in the in-plane (x-y) direction. The glass fibers constrain the board in the x-y plane but not through the thickness. As a result, stress can build up in the PTH barrel and eventually cause cracking to occur near the center of the barrel. Figure 13 shows a cross section of a PTH.

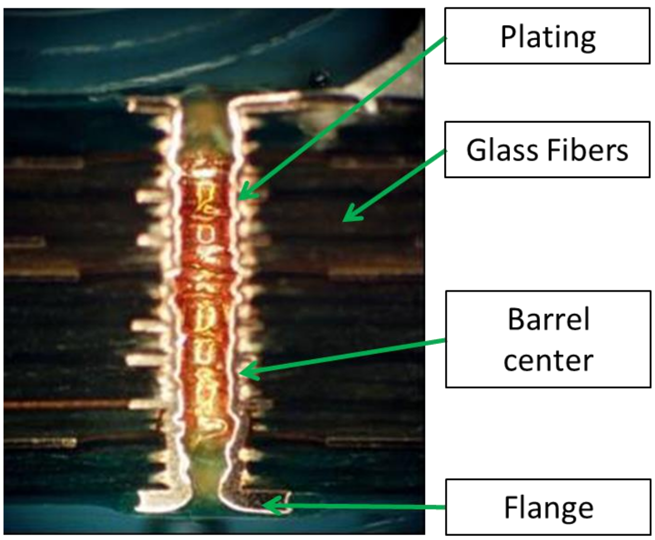

Figure 13 Anatomy of a Plated Through Hole

While there is a tendency for plating to crack towards the center of the barrel, it is possible for cracks to appear in other places in the PTH. One of the difficult aspects of finding a PTH crack is that the failure may only be detected when the board is at high temperature. When the board is then tested for faults at room temperature, the fault is not found because the board has shrunk and the two sides of the crack are now touching.

There is an industry accepted failure model outlined in IPC-TR-579 (Round Robin Reliability Evaluation of Small Diameter Plated-Through Holes in Printed Wiring Boards) in order to predict the appearance of cracks in PTH. This model assumes perfectly elastic deformation when below yield strength (σ_y or S_y) and a linear stress-strain relationship during the failure occurrence. Equation 8 is used to determine stress applied (σ). The plating material used in this example is Copper but any plating material that follows the assumptions will work as well.

For these equations,
σ = barrel stress
S_y = PTH barrel copper yield strength
E subscript denotes epoxy
Cu subscript denotes PTH barrel copper
α_E = CTE of PCB in Z direction
α_{Cu} = CTE of copper
ΔT = temperature range of thermal cycling
A_E = area of influence on PCB
A_{Cu} = area of the copper barrel
E_E = modulus of elasticity of epoxy
E_{Cu} = modulus of elasticity for electroplated copper
h = thickness of the PCB
d = drilled PTH diameter\
t= thickness of the PTH copper barrel
D_f = fracture strain
S_u = tensile strength of the PTH barrel

$$\sigma = \frac{(\alpha_E - \alpha_{Cu})\Delta T A_E E_E E_{Cu}}{A_E E_E + A_{Cu} E_{Cu}}, \text{for } \sigma \le S_y$$

$$\sigma = \frac{\left[(\alpha_E - \alpha_{Cu})\Delta T + S_y \frac{E_{Cu} - E'_{Cu}}{E_{Cu} E'_{Cu}}\right] A_E E_E E'_{Cu}}{A_E E_E + A_{Cu} E'_{Cu}}, \text{for } \sigma > S_y$$

$$A_E = \frac{\pi}{4}\left[(h+d)^2 - d^2\right]$$

$$A_{Cu} = \frac{\pi}{4}\left[d^2 - (d-2t)^2\right]$$

Equation 8: Determination of applied stress according to IPC-TR-579

Then, use the stress value to determine strain range ($\Delta\varepsilon$) as shown in Equation 9.

$$\Delta\varepsilon = \frac{\sigma}{E_{Cu}}, \text{ for } \sigma < S_y \qquad \Delta\varepsilon = \frac{S_y}{E_{Cu}} + \frac{\sigma - S_y}{E'_{Cu}}, \text{for } \sigma > S_y$$

Equation 9: Strain rage equations according to IPC-TR-579

A calibration factor is applied based on the quality index (K_Q~0 to 10) and strain distribution factor (K_d~2.5-5.0) to find the "effective" strain range using Equation 10.

$$\Delta\varepsilon_{eff} = \Delta\varepsilon\left(K_d \frac{10}{K_Q}\right)$$

Equation 10: Effective strain rate calculation

The number of cycles-to-failure (N_f) can then be calculated using Equation 11.

$$N_f^{-0.6} D_f^{0.75} + 0.9\frac{S_u}{E}\left[\frac{\exp(D_f)}{0.36}\right]^{0.1785\log\frac{10^5}{N_f}} - \Delta\varepsilon = 0$$

Equation 11: Number of cycles to failure of a PTH

The IPC-TR-579 standard was based on round-robin testing of 200,000 PTHs performed between 1986 to 1988 with hole diameters ranging from 250 µm to 500 µm, board thicknesses from 0.75 mm to 2.25 mm and plating thicknesses from 20 µm to 32 µm. The advantage of this standard is that it is a straightforward analytical calculation that was validated through extensive testing. The main disadvantage of this standard is that the validation data is over 20 years old. It also can't handle complex geometries of PTH spacing and PTH pads that can impact the lifetime. It can be a bit difficult, but possible, to assess the effect of multiple temperature cycles but using Miner's rule.

Eliminating PTH fatigue completely is impossible. Better reliability can be achieved if the board laminate and PTH plating material have a close CTE value for the out-of-plane direction. The board glass style and resin content can be modified to some degree. Increasing the glass content can help reduce the CTE mismatch but makes it harder to drill the holes into the board. The plating material ductility also affects the life of the PTH. The predicted numbers of cycles to failure are plotted in Figure 14 for different glass styles. The plating material, plating thickness, temperature profile and drill diameters are kept the same.

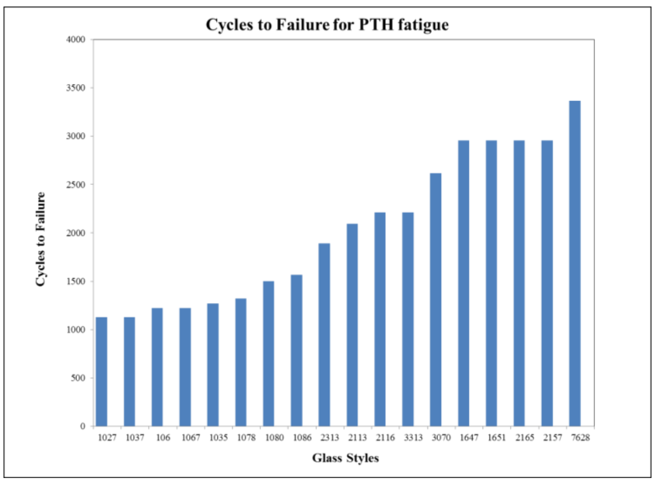

Figure 14 Effect of Glass Style on PTH Fatigue

There is a clear trend for the PTH fatigue performance to improve for low CTE and high modulus glass styles; but, the use of underfills, potting compounds and thick conformal coatings can greatly influence the failure behavior under thermal cycling. Potting materials can cause PCB warpage and tensile stresses on electronic packages that greatly reduce time to failure. Ideally the CTE of the potting should be as close to the PCB as possible. As the CTE mismatch increases, the potting must be more compliant to limit the stresses imparted. Underfill material can improve the stress distribution in solder joints during both temperature cycling and drop testing; however, the appropriate underfill must be selected. Underfills designed for enhancing shock robustness do *not* tend to enhance thermal cycling robustness. Lower CTE & higher Tg in underfill were more effective than other factors in temperature cycle performance. Temperature cycling test results have shown that the filler type underfills provides substantially improved temperature cycling performance over non filler type underfills. Another consideration that complicates the calculations is that any time a material goes through its glass transition temperature, properties change. The analytical computational method will work for most cases where PTH are not soldered or are potted.

SUMMARY

The majority of failures in electronics are caused by thermo-mechanical loads and solder fatigue is the major failure mechanism. The CTE mismatch between the board, component and attach materials creates stresses in the solder and the plating material. Experimental data for solder fatigue predictions and basic models can be used to predict solder fatigue for surface mount components. Board designers can change component placement and board laminate material to alleviate fatigue since component level design changes are usually not an option. The board laminate design also affects PTH reliability. The board designer influences PTH reliability by modifying drill diameters, laminate material, and plating parameters. Solder and PTH fatigue are just two of the many effects of thermo-mechanical loads but they can be predicted and prevented.

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