White Paper on soldering QFN packages to electronic assemblies.

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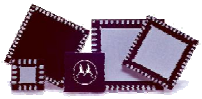
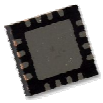


Defect free QFN Assembly



What the Designer needs to know

QFN Description: A QFN package is a QUAD-FLAT-NO LEAD device. This package is small and lightweight and has no leads (unlike a gull wing or J-leaded device). QFN's have a thermal pad (paddle) on the bottom side of the part that offers heat dissipation and grounding. QFN's are popular due to the low power and excellent characteristics provided by the grounding pad. QFN's are also referred to as Micro-Lead frame (MLF).

Figure 1

The problem with soldering QFN packages is that they float, skew and tilt on the 'domed' melted solder during the SMT re-flow process. This floating, skewing and/or tilting will lead to solder bridging or un-solders. These defects are hard to detect until the assembly reaches test. Troubleshooting these elusive defects can be very time consuming and costly leading to rework, replacement parts, possible late deliveries and eventually the high cost of a re-design.

QFN packages are still a relatively new package to the surface mount world and the standards and practices are still being developed. There is no standard that exists (at the time this article was published) in IPC-7351 so there are a variety of land patterns.

Achieving reliable solder joints requires special attention to the following areas:

- The design of the bare PCB board relating to the Pad layout (land pattern)
- The type of Via holes
- The design of the solder-mask layer
- The design of the solder paste stencil
- The Reflow profile
- The solder paste – Must use No-Clean
- Board surface finish
- Component tolerance

This article addresses each of these.

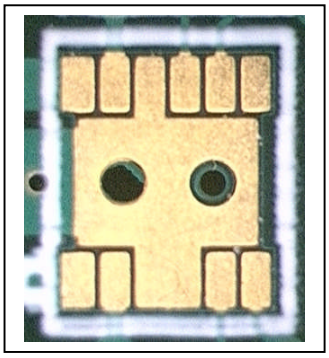


Figure 2

The Pad layout (land patterns) shall be uniform and consistent in size. Trouble occurs when some of the pads are larger (as shown in Figure 2). The 'reflowed' or melted solder spreads out thin on the larger-wider pads and domes up high on the small-skinny pads. The QFN package will float and sit up on the domed solder joints causing unsoldered connections on the wider pads.

Via holes can be designed using one of several fabrication methods. Contact your bare board supplier for the latest in technology, hole sizes and cost considerations. In general the following methods are used:

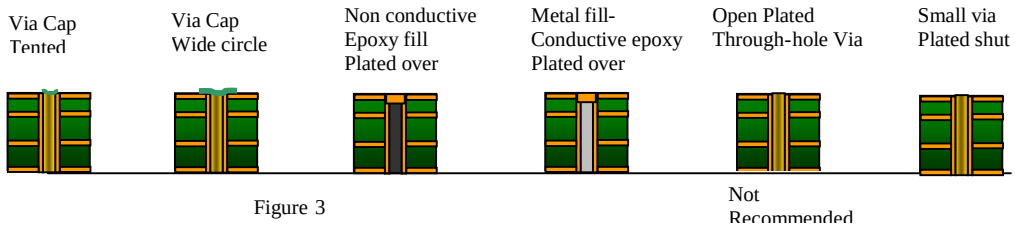


Figure 3

Via holes are needed to improve thermal conductivity and grounding. The quantity of vias to place in the ground pad is based upon the thermal and electrical requirements for each application. Plated over or plated shut works best from an assembly stand point. This prevents solder from being lost down into the Via hole and starving the intended solder connection. The via can be filled with either a conductive or non conductive material and then plated shut leaving a smooth surface. A more costly approach is to drill with a very small drill and then plate the via completely shut with copper. An open unfilled Plated Through-hole (PTH) is not recommended. If you are opting to use an unfilled PTH via make them small (as shown in Figure 5). The Via can also be tented over or 'capped' to prevent the solder from wicking. The cap with be roughly 2 mils in height and will hold the QFN up and have an impact on the standoff height on the Signal pads. Via holes should not be placed near the edge of the Signal pad (as shown in Figure 4) unless it is completed tented or plugged with solder-mask.

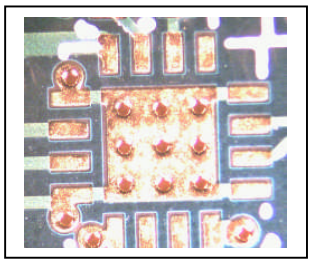


Figure 4 - Poor

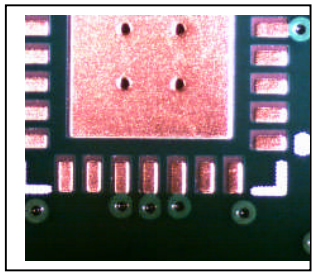


Figure 5

The solder mask layer should be designed to provide consistent and symmetrical pad sizes. When solder mask is used to define the pad size, over a common ground plane, the size of each pad should be the same (as shown in the upper right corner of Figure 6). Also, a 3 Mil solder-mask 'dam' should be provided between each pad. A solder mask dam is not required between metal defined pads however, and often the design opens up the whole area leaving no solder mask between pads. The spacing between pads is critical to prevent bridging (shown in Figures 6 and 7). Maintain a minimum spacing of 7 mils between pads and between the pad and thermal ground plane. Some fabrication shops require an 8 mil minimum space between pads and a 4 mil minimum solder mask dam. In Figure 8, the spacing between

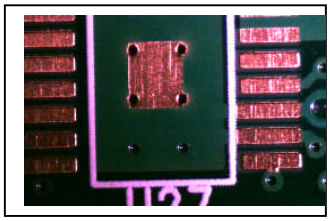


Figure 6

pads was only .005". This makes using a solder-mask dam impossible and leads to solder bridging (shown in Figure 4). In this example, the copper was cut back to provide an .008" space between the pads and between the pads and thermal ground plane (as shown in Figure 7). It is not recommended to use solder-mask to define the window on the thermal ground plane.

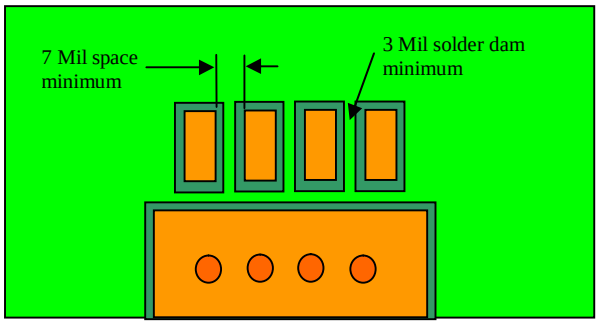


Figure 5

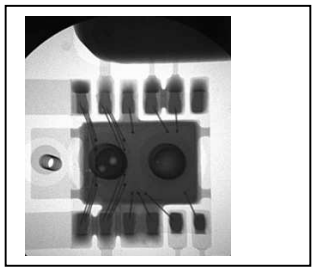


Figure 6

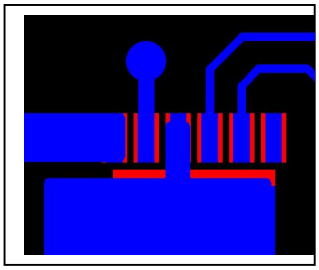


Figure 7

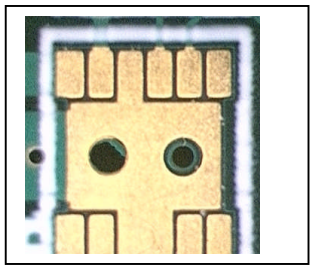


Figure 8

The solder paste stencil needs to be designed with a considerable reduction in the amount of paste applied to the thermal ground plane area. The window pane (shown below in Figure 10) is a common method used. As much as 50% reduction in aperture opening vs. ground pad has been reported. The purpose is to keep the QFN package from floating up and to reduce voiding under the QFN.

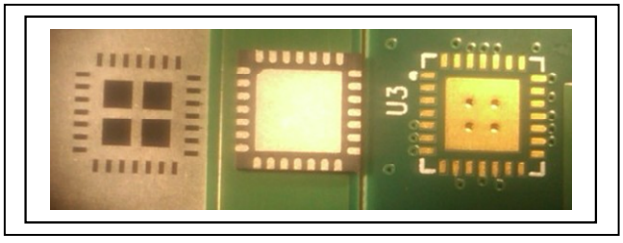


Figure 10 – Stencil, QFN, PCB pattern

A variety of patterns (Figure 12) may be used in the stencil design however the window pane appears to be the most commonly used method. If the design is using tented or capped vias, the stencil needs to avoid printing paste over the solder mask cap. If the design uses a plated through hole as the via, less reduction is needed in the stencil design for the thermal pad. Consideration for the amount of solder lost into the holes is needed.

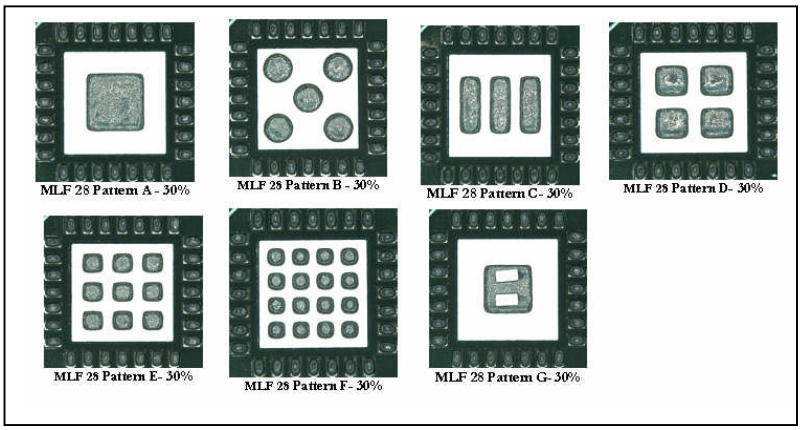


Figure 12 (Courtesy of Rochester Institute of Technology CEMA lab)

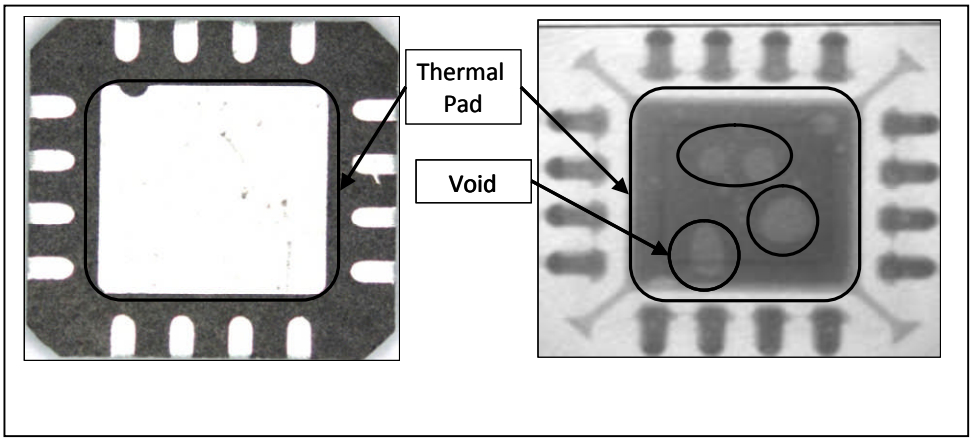


Figure 13 (Courtesy of Rochester Institute of Technology CEMA laboratory)

Voiding is one defect that results from too much solder paste (as shown in Figure 13). Voiding underneath a QFN prevents proper heat sink and grounding properties. Eliminating voids completely is challenging and may not be necessary. If the void is greater in size than the Via pitch, it may impact RF signaling in a high speed application.

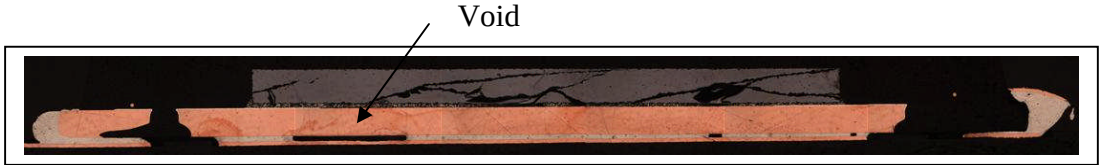


Figure 14 (Courtesy of Rochester Institute of Technologies CEMA laboratory)

The size, shape and stand off height of the solder joint will be a result of multiple variables: the amount of paste applied to both the pad and the thermal ground plane, the Via hole size and whether it is plugged or capped, and the size of the pad. Notice how the pad in Figure 14 is underneath the QFN and also extends beyond the component body. This is a common practice

which allows visual and Automated Optical (AOI) inspection of the solder joint. This may also allow probing however, a probe trace and pad should be added if probing is planned.

The reflow profile should be optimized to minimize voiding and allow the solder joint to dwell above liquidous (See Figure 13) temperature of the solder paste being used.

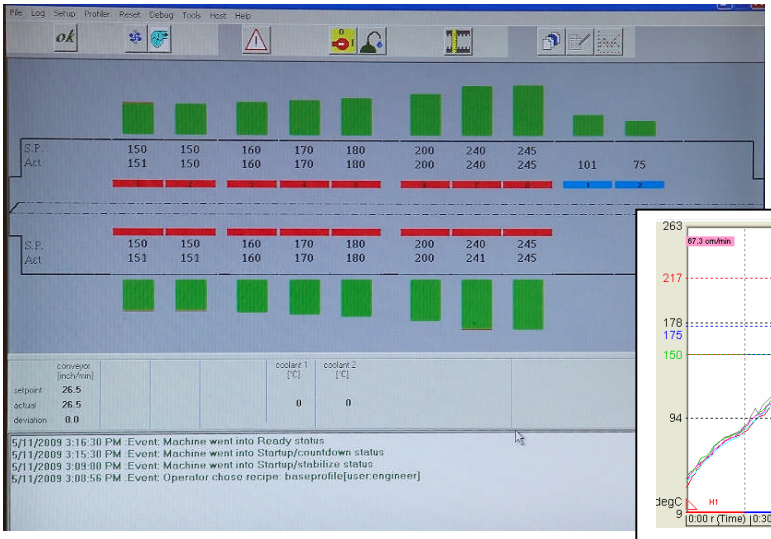


Figure 15 - Reflow Oven parameters. Settings of temperature and conveyor speed

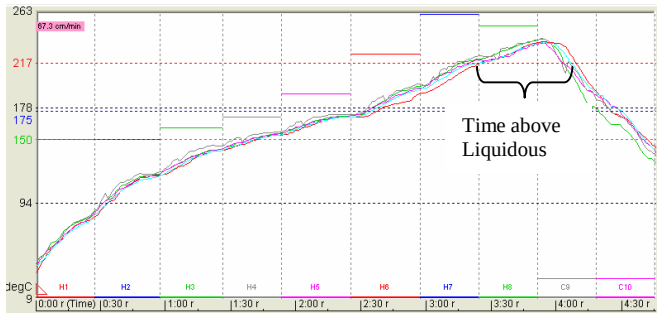


Figure 16 - Resulting Time / Temperature Reflow Profile

Solder paste selection. Cleaning Flux residue from underneath a soldered QFN package is virtually impossible. No Clean solder paste must be used. The gap underneath this part is too small to allow water to impinge underneath and clean flux residues. Using water soluable flux will lead to 'un-cleaned' residues being left underneath this part leading to corrosion.

The surface finish on the PCB shall be flat. Electroless Nickle Immersion gold (ENIG) is commonly used. Organic Solderability preservation (OSP) is very flat and works fine as well as Immersion silver. Hot air solder leveling (HASL) will only work if the fabrication shop can provide consistently flat pads.

Tolerance stack up. The QFN package has a tolerance on the lead width. For example the leads could be .009" +/- .002". The SMT placement machine is extremely accurate however the programmed placement value is CAD data driven. The actual pad size will be based on the PCB fabrication tolerances (over etching or under etching). The combination of these tolerances may stack up to cause a shift or overhang of the part lead to pad which can lead to bridging.

Reworking QFN packages are to be done only be a skilled technician. QFN packages have no leads so hand soldering a QFN using even the smallest solder iron tip is next to impossible. Often the designs do not have the pads extending beyond the component body so there is no metal to heat up using an iron. Using a mini-stencil to apply solder paste to the board proves challenging because the parts are so small and the surrounding area typically has numerous other parts that

would have to be removed. An interesting technique has been found to work well. After removing the QFN the operator must prepare the site on the board by wicking away excess solder and then tinning the pads flat. A mini-stencil is then used to dispense solder paste on to the part (see Figure x). The part is then placed onto the PCB and reflowed using a BGA rework tool.

In summary, the passion and relentless drive to assemble defect free assemblies has prompted the documentation of this article. If you have stories to share in the interest of applying Industries best practices or if you have application questions please contact us at AccuSpec Electronics, LLC.

Courtesy of Amkor

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