Organic Flip Chip Packages for Use in Military and Aerospace Applications

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Reliability needs of High End Commercial Products

• **Server & Telecom (Servers, Routers, Hubs & High Speed Switches)**
  – High reliability requirements
    • Minimum 10 years life
      – Component on PCB stressing from 0 to 100C and 3,600 cycles to first failure
      – Component only stressing from -55 to +125C and 1000 cycles to first failure
  – High power requirements, 50 to 100 watts are common
  – High signal densities, > 1700 signals in a 52.5mm BGA
  – High electrical performance, 12.5 GB/s
  – Companies in these markets are building equipment for satellite applications
  – Stringent Shock and Vibration requirements

• **High End Commercial Applications have driven development of technologies that can bridge to Military / Aerospace**
Wire Bond Packaging: Aerospace

- Aerospace: 1st plastic BGA for Satellite
  - Chip Up
  - > 700 BGA I/O, 42.5mm body
  - > 300 signals
  - 2 signal, 4 layer Cavity PBGA
  - 75 micron lw/ls
  - 16.6mm die
  - Commercial Overmold
Wirebond Build Up Package: Military

- 35mm WB CU PBGA
  - 2-6-2 X Section (10 layer), 7 Signals, 3 Pwr/Gnd
  - 37.5mm body size
  - 864 micron total thickness
  - 69 micron thick top BU layer thickness
  - 75 micron lw, 53 micron ls
  - BU vias are 100 micron CO₂ laser drilled
    - 250 micron pads in outer most BU layers
    - 300 micron (12mil) pads on Inner BU layers
    - Stacked BU vias
  - Core vias are 200 micron dia. mechanical drilled on 400 micron pads

- Can be either WB or FC, SIP or SC

- Glass reinforced Polyimide – Nelco 7000 2HT
  - Er: 4.26 @ 1 to 2.5GHz (50% resin content)
  - Dielectric Loss: .009 @ 1GHz (50% resin content)
  - Tg: >250C
PTFE Based Flip Chip SiP’s: Military

- System in Package (ASIC / CSP memory and decaps)
  - Server Processor Packages:
    - 18 mm die size
    - 2 signal layers, 280 signals
    - 250 micron die pad pitch
    - CSP memory
    - Top and bottom decaps
    - 630 I/O SMT PGA connector
## Weight Comparisons for Plastic vs Ceramic 40mm body size

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Approximate substrate weight (gm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ceramic (30 layer, alumina, 10mil/layer)</td>
<td>48.0</td>
</tr>
<tr>
<td>Ceramic (15 layer, alumina, 10 mil/layer)</td>
<td>24.0</td>
</tr>
<tr>
<td>PTFE BGA 9 layer substrate</td>
<td>2.3</td>
</tr>
<tr>
<td>Thin core build up 10 layer substrate</td>
<td>2.9</td>
</tr>
<tr>
<td>Thin core build up 6 layer substrate</td>
<td>2.0</td>
</tr>
</tbody>
</table>
High End Telecom and Server Applications using Flip Chip Plastic

- Drivers are similar to Military/Aerospace
  - Package shrink is critical, weight not as large a concern
  - High speed signals with low noise
    - Clean eye’s at 12.5 Gb/s in production
    - 600 differential pairs are common
  - High BGA/LGA/PGA I/O with min. 10 yr field life
    - 52.5 mm, 2577 BGA I/O, 1 mm BGA pitch in high frequency routers
    - 90nm Si technology
    - 25 micron lw/ls
    - 200 micron Flip Chip die pad pitch, 16 rows deep
  - Low volume applications, some need to remain on shore
Highlights of Advanced Plastic Flip Chip Packaging

- 50 micron UV laser drilled vias
  - Fine pitch (less than 200 micron), for full access to wiring planes

- 12 micron thick Copper Conductors
  - 25 micron Line Width

- Thin Core and Coreless Technologies

- Thin Substrates (0.4 to 0.6 mm thick)

- Build up dielectric layer thickness available 35 to 50 microns

- Low-stress PTFE and Particle Filled Epoxy Dielectrics
  - Low-k dielectrics: High Frequency, Low-Noise applications
  - \( Er = 2.7 \) for PTFE, \( Er = 3.7 \) for thin-core buildup

- Solder Bumped Copper Die Pads
Overview: Typical PTFE 9 layer Cross Section - HyperBGA®

Substrate thickness - .47 mm
Overview: Typical Thin Core 10 layer Cross Section - CoreEZ®

- Solder mask - PSR4000 15 μ thick
- Build up layer 1
- Build up layer 2
- Build up layer 3
- DriClad, 35/50 μ thick
- Outer Core dielectric
- DriClad, 35/50 μ thick
- Inner Core
- 100/150 μ thick
- Thermount
- Core Cu
- 12 μ thick
- Copper-filled stacked micro-via
- Substrate Thickness – 0.55 mm
### Typical PTFE Package Reliability Performance

<table>
<thead>
<tr>
<th>Test</th>
<th>Format</th>
<th>Duration</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preconditioning - JEDEC Level 3</td>
<td>Component</td>
<td>96H</td>
<td>N/A</td>
</tr>
<tr>
<td>Thermal Cycle (0/100°C)</td>
<td>Card</td>
<td>3600 Cycles</td>
<td>pass</td>
</tr>
<tr>
<td>Power Cycling (25/125°C)</td>
<td>Card</td>
<td>3600 Cycles</td>
<td>pass</td>
</tr>
<tr>
<td>Deep Thermal Cycling (-55/+125°C)</td>
<td>Component</td>
<td>1000 Cycles</td>
<td>pass</td>
</tr>
<tr>
<td>Wet Thermal Shock (-40 / +125°C)</td>
<td>Component</td>
<td>100 Cycles</td>
<td>pass</td>
</tr>
<tr>
<td>T. H. &amp; B. (85 °C / 85%RH/3.7 V)</td>
<td>Card</td>
<td>1000 Hours</td>
<td>pass</td>
</tr>
<tr>
<td>HAST (110 °C / 85%RH/3.7V)</td>
<td>Card</td>
<td>264 Hours</td>
<td>pass</td>
</tr>
<tr>
<td>Pressure Pot (121 °C / 100% RH/2atm)</td>
<td>Component</td>
<td>96 Hours</td>
<td>pass</td>
</tr>
<tr>
<td>High Temp. Storage (150 °C)</td>
<td>Component</td>
<td>1000 Hours</td>
<td>pass</td>
</tr>
<tr>
<td>Low Temp. Storage (-65°C)</td>
<td>Component</td>
<td>1000 Hours</td>
<td>pass</td>
</tr>
<tr>
<td>Shock/Vibration JEDEC</td>
<td>Component</td>
<td>various</td>
<td>pass</td>
</tr>
</tbody>
</table>

Component level testing is die assembled to substrate with underfill, lid and BGA balls, card level testing is component assembled to PCB.
# 0 to 100°C Accelerated Thermal Cycle Reliability

Component Attached to PCB

<table>
<thead>
<tr>
<th>Failure Mode</th>
<th>Ceramic BGA ATC Life (cycles)</th>
<th>PTFE BGA ATC Life (cycles)</th>
<th>Thin Core Build Up ATC Life (cycles)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package Internal</td>
<td>&gt;10,000</td>
<td>&gt;10,000</td>
<td>&gt;5000</td>
</tr>
<tr>
<td>Flip Chip Joint</td>
<td>&gt;10,000</td>
<td>&gt;10,000</td>
<td>&gt;5000</td>
</tr>
<tr>
<td>BGA Corner Joint</td>
<td>800 to 2,000</td>
<td>&gt; 10,000</td>
<td>&gt;5000</td>
</tr>
<tr>
<td>BGA Chip Edge Joint</td>
<td>&gt;10,000</td>
<td>&gt;10,000</td>
<td>5000; extendable to 10,000 with optimized design</td>
</tr>
</tbody>
</table>

- Includes Precondition Stress as JEDEC-020C Moisture Resistance level 4 with 3x Reflows
- Package size 42-52mm; Both PTFE and Thin Core exceed ceramic package reliability
## Flip Chip Package Wireability Comparison

<table>
<thead>
<tr>
<th>Substrate</th>
<th># of Signal layers</th>
<th>Signal Wiring Escapes per mm of die edge per layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ceramic, 30 layers</td>
<td>12</td>
<td>2.7</td>
</tr>
<tr>
<td>PTFE BGA, 9 layers</td>
<td>2</td>
<td>4.4</td>
</tr>
<tr>
<td>Thin Core Build Up 6 layers</td>
<td>2</td>
<td>5.9</td>
</tr>
<tr>
<td>Thin Core Build Up 10 layers</td>
<td>4</td>
<td>7.0</td>
</tr>
</tbody>
</table>
Organic Flip Chip Package Outgassing Performance

- **Materials**
  - Rogers 2800 PTFE
  - Asahi APPE
  - Driclad Epoxy
  - Thermount 55LM
  - PSR4000

- **Maximum of 1.0% Total Mass Loss**
  - All materials & finished substrates < 1.0%

- **Maximum 0.1% Collected Volatile Condensable Materials**
  - All materials & finished substrates < 0.1%
Evaluation of Materials Subjected to Various Radiation Levels

- Evaluated PTFE BGA (HyperBGA®) and Thin Core (CoreEZ®) materials radiation response
  - Radiation Exposure: Co60 Gamma:
    - Control
    - 32, 50, 100, 300, 500, 700, 1000 and 5000 krad TID
  - PTFE Materials evaluated: Rogers 2800, Asahi APPE
    - Results: Many applications will be unaffected by radiation
      - APPE has no measurable degradation to 5 Mrad
      - R2800 shows gradual loss of ductility with exposure
  - Thin Core Build Up Materials Considered: Thermount 55LM, Particle Filled Driclad Epoxy, PSR4000
    - Results: No measurable change of mechanical properties through 5 Mrad
Material Ductility Test with tensile stretch of film sample – PTFE example

Sample geometries:

½” wide, 6” length
Thickness as used in application, <0.010”

Monotonic Stretch to Failure
Crosshead rate: 0.025”/min
5-10 samples per condition, average failure strain found

Criteria for failure – onset of load loss

Moving Crosshead
Material Sample
Fixed Crosshead

Endicott Interconnect
EI’s packaging performance after radiation exposure

Material Degradation

Radiation Dosage (Co60 Gamma - Krads)

- Thin Core Soldermask PSR4000
- Thin Core Buildup Driclad
- Thin Core Thermount
- PTFE Package APPE
- PTFE

✓ Ductility performance indicates package performance in thermal cycling

- Thin Core Build Up appears to be a good choice for Rad Hard and Strategic apps.
  - materials show no ductility degradation with radiation level
- PTFE appears to be best suited for Rad Tolerant applications
  - PTFE ductility is higher than all other materials below 300K rad exposure
  - PTFE predictably degrades significantly above 300Krad exposure levels
Conclusions

• Flip Chip PBGA Packages are Suitable for Military / Aerospace Applications
  – Reliability
  – Wireability
  – Outgassing
  – Radiation Exposure

• Significant Weight Savings Realized with PBGA Packages

• Advantage to Overall Life Costs and Performance
Acknowledgements

For controlled material radiation exposure, outgassing, sample design and analysis, and helpful review / comments

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