

# Laser-Based Methodology for the Application of Glass as a Dielectric and Cu Pattern Carrier for Printed Circuit Boards

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## Abstract

Glass offers a number of advantages as a dielectric material, such as a low coefficient of thermal expansion (CTE), high dimensional stability, high thermal conductivity and suitable dielectric constant. These properties make glass an ideal candidate for, among other things, package substrate and high-frequency PCB applications. We report here a novel process for the production of printed circuit boards and integrated circuit packaging using glass as both a dielectric medium and a platform for wiring simultaneously. An ultrafast laser is used to etch away the desired pattern (pads, wires and vias) in the glass, and copper plating is “seeded” through the laser-based deposition of copper droplets. The seeded area is then plated using electroless plating followed by electroplating. Demonstrations of fine pitch wires, variable diameter through holes and blind vias, and a multilayer stack are shown. The deposits have a resistivity less than a factor of 1.5x that of bulk copper for 5-10 mm wires. Plated lines in borosilicate glass of 7-10  $\mu\text{m}$  width and 5-20  $\mu\text{m}$  depth and line spacing down to  $\sim 10 \mu\text{m}$  are demonstrated, as well as vias with a top diameter approaching 100  $\mu\text{m}$  for 150  $\mu\text{m}$  thick glass and 40  $\mu\text{m}$  for 50  $\mu\text{m}$  thick glass. The process presents the potential for significant material savings in terms of base materials, process chemicals, and waste disposal/recycling costs (glass is on the order of 100-fold less expensive than some current high-frequency dielectrics, and wet processes account for a large part of standard PCB/substrate manufacturing). Additionally, the processes are amendable toward other dielectric materials such as FR4, PI, and PTFE-based materials.

## Introduction

Increased demand for high data transmission rates is driving the development of smaller PCB features. Electrical circuits are reaching the physical limitations of traditional PCB dielectric materials under which electromagnetic compatibility can be controlled. Additionally, a high-density of features, such as in advanced flip chip packages, require substrates with low CTE, high dimensional stability, high thermal conductivity and suitable dielectric constant. Glass offers a number of advantages in this regard,<sup>1</sup> including that it is very stable in terms of electrical properties, moisture absorption, and aging, and has a CTE similar to that of silicon, making it ideal for IC packaging. Furthermore, the dielectric constant of glass is, in some instances, lower than that of FR4. This, coupled with a low loss tangent, and low materials cost compared to high-performance materials, make glass suitable for high-frequency applications.

Many different approaches have been taken toward the realization of conductive plating of glass substrates, including: chemical vapor deposition, evaporation and sputtering;<sup>2,3</sup> chemical, mechanical, and laser roughening to improve electro- and electroless plating, laser direct-write techniques (*vide infra*), including sintering of metallic powders;<sup>4</sup> and using self-assembled monolayers to better adsorb catalysts for electroless plating.<sup>1</sup> Difficulties with glass metallization arise from chemical and mechanical incompatibilities between brittle, stiff glass and the metal, such as CTE incompatibility and strong interfacial stresses. Smooth glass surfaces present no possibility of mechanical interlocking; so metal films can easily separate from the substrate.

We report here a novel method for metallization of glass dielectrics involving laser-induced forward transfer (LIFT) of metallic foils to seed electroless plating, thereby forming strongly anchored conductive patterns. The specific techniques examined here allow for plating of conductive traces and vias, multilayer all-glass structures and multilayer mixed-material structures. In LIFT, the desired material for deposition is adhered to a transparent carrier; this substrate is referred to as the “donor.” A laser is focused through the transparent carrier layer of the donor onto the material, resulting in transfer of the material to a “receiving” substrate. The LIFT technique applied to conductive metals was first described in 1986 by Bohandy *et al.*, for the forward transfer of copper onto silica substrates using an ArF excimer laser,<sup>5</sup> and has since been applied to deposit a variety of materials onto many different substrates,<sup>6,7</sup> including organic and biological materials.<sup>8</sup> Printing of conductive inks and nanopastes has been a focus of recent research in LIFT applications.<sup>9</sup> Techniques that utilize conductive inks offer the promise of a high degree of shape and size control for the deposited material (for example, using spatial light modulators), but the inks themselves have conductivities several orders of magnitude less than their bulk counterparts, some of which can be mitigated through *in situ* laser curing of the deposited ink.<sup>10</sup> LIFT has also been used for preparing embedded components, by direct-writing conductive inks to make connections between already embedded components,<sup>11</sup> or by using LIFT to place the components themselves.<sup>12,13</sup> Copper beams can be laser cut, bent, and deposited using LIFT, but require conductive glues for adhesion.<sup>14</sup> Most similar to the technique described in this report is an approach that uses LIFT to

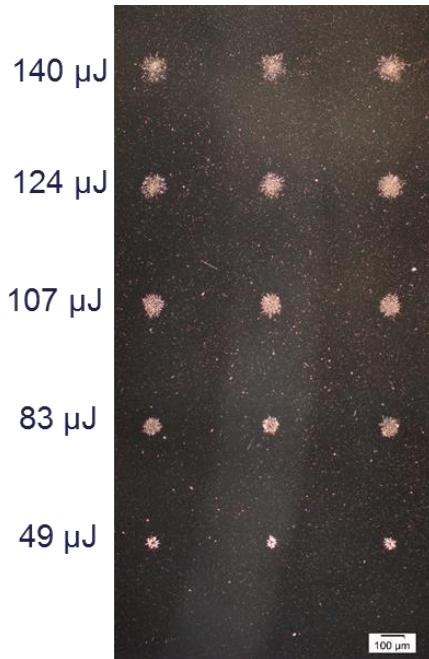
deposit palladium droplets,<sup>15</sup> in which excimer lasers were used to decompose a palladium acetate film on a transparent substrate to palladium particles and deposit them on quartz, ceramic, and polymer substrates. The palladium droplets can act as catalysts for the plating of copper, nickel, and gold. This approach is limited by the low abundance, and correspondingly high cost, of palladium (around \$650 per ounce at the time of writing).

### Plating on Glass

The seeding methods described below can be carried out on flat, smooth glass substrates, but the metals plated on these surfaces lack mechanical stability and dimensional control. As a result, a typical approach requires laser ablation of the glass substrate to produce unplated features (pads, wires and vias), followed by application of the following seeding method. Laser glass ablation was carried out on a company system, employing a laser operating at 515 nm with pulse duration of 800 fs. A typical glass substrate used in this work is a microscope cover slide (either soda lime or borosilicate glass), cleaned by rinsing with methanol and wiped dry using a lens wipe, and handled only with gloved hands. The 150  $\mu\text{m}$  thick glass slides used in this work for the demonstrators are production borosilicate glass coverslips with low iron content. The 50  $\mu\text{m}$  glass is a production alkali-free glass with a thermal expansion coefficient matching that of silicon for chip packaging applications. Typical glass ablation parameters are 1 MHz pulse repetition rate, 3  $\mu\text{J}/\text{pulse}$  and a feed rate of 500-1000 mm/s for a spot size of 12-15  $\mu\text{m}$ . When operating with the focus at the top of the glass substrate, trenches can be made in borosilicate glass using these parameters that are  $\sim 7 \mu\text{m}$  wide and  $5 \mu\text{m}$  deep in a single pass; additional passes can be employed to deepen the trench without significantly affecting the width. Narrower and shallower features can be made by lowering the pulse energy or defocusing the beam. The same parameters can be used for producing pads and vias by utilizing a 7  $\mu\text{m}$  pitch, and cross hatching the fill lines provides the best results. Vias are produced by applying the crosshatch pattern multiple times or by using a racetrack pattern, and scanning the Z range of the substrate while undertaking this process improves the shape of the via. Larger pulse energies are required as the via diameter approaches the thickness of the glass piece (*i.e.*, the aspect ratio nears 1). Blind vias can be drilled using either the company system described above, or the company's CO<sub>2</sub>-based microvia platform, employing a 9.3  $\mu\text{m}$  CO<sub>2</sub> laser.

Laser seeding for electroless plating was carried out as follows. A high power diode-pump solid state green laser operating at 30 kHz and 50-200  $\mu\text{J}/\text{pulse}$ , with *ca.* 11 ns pulse width, was focused to a 30-40  $\mu\text{m}$  diameter spot onto a thin copper foil laminated onto a glass slide, melting the copper and directing the material toward the desired substrate. To prepare this donor substrate, a 4% aqueous solution of poly(vinyl alcohol) (PVA) was spin coated onto a 1 mm thick borosilicate glass slide and the film allowed to dry for several hours to produce a uniform coating about 1  $\mu\text{m}$  thick. The production foil, as received, consisted of a 10  $\mu\text{m}$  thick copper foil bound to a 35  $\mu\text{m}$  "carrier" layer of copper. The thin foil was laminated onto the PVA layer using a hot press operating near the melting point for PVA for several minutes. For this, the 10  $\mu\text{m}$  copper layer was placed in contact with the PVA layer, and the carrier side is facing out. After lamination, the carrier layer can be easily peeled away leaving the thin layer adhered to the glass supporting substrate. Optimum laser processes utilize bite sizes (beam displacement between pulses) that are 50-75% of the focused spot diameter. Figure 1 shows deposited copper on a flat borosilicate glass surface using the method described above, with no offset between the forward transfer substrate and the receiving substrate. The process utilizes a single laser pulse with 30  $\mu\text{m}$  focused spot at the work surface with variable pulse energies. The scale bar is 100  $\mu\text{m}$ . The Figure shows that the method has a resolution (deposited spot diameter) of  $\sim 50 \mu\text{m}$  at low pulse energies; at higher pulse energies the feature size increases. The transferred copper is strongly anchored (it passes a typical tape test), and conductive patterns can be made directly from this technique using multiple passes and/or the proper pitch, although these multiple deposits are not structurally strong on smooth glass surfaces. Figure 1 also shows that there is unbound copper dust between the anchored features. This can easily be removed by gently wiping the surface.

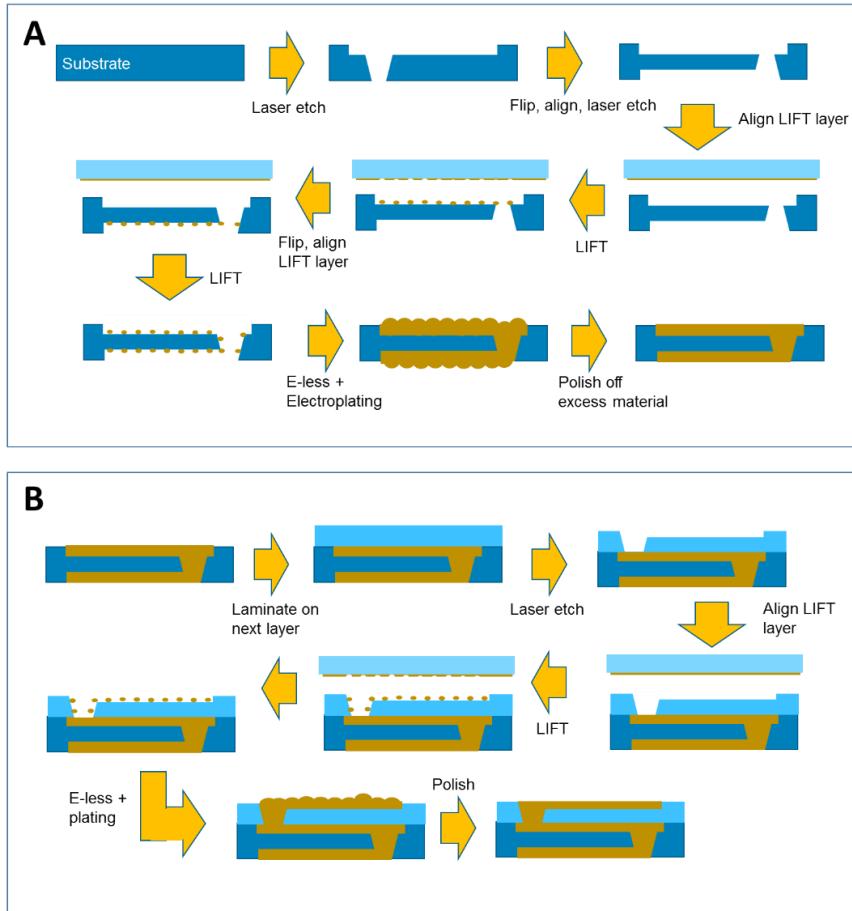
A company micromachining platform was utilized for copper forward transfer in instances that required precise alignment of the donor substrate. The system utilized a third-harmonic Nd:YAG laser (355 nm) with pulse repetition frequencies up to 90 kHz, pulse duration  $\sim$ 10 ns,  $\sim$ 12  $\mu\text{m}$  focused beam diameter, and maximum average power of around 11 W. The same donor substrate described above can be utilized with proper laser dosing conditions, *i.e.*, using sufficiently large bite sizes to minimize damage to the receiving substrate and sufficiently low pulse energies to maintain good resolution of the deposited copper. Other forward transfer processes that employ different lasers, process parameters (including laser wavelength, pulse duration, energy, pulse repetition rate, as well as offset of the substrates), and forward transfer substrates have been successfully implemented toward this approach and can offer seeding resolution below 10  $\mu\text{m}$ . These methods are the subject of a future paper.



**Figure 1.** Copper deposits made on a smooth borosilicate glass surface using a 532 nm, 11 ns, 30 kHz Nd:YAG laser focused to a 30  $\mu\text{m}$  spot on a 10  $\mu\text{m}$  copper foil adhered with a 1  $\mu\text{m}$  PVA layer to a 1 mm thick borosilicate glass slide. The pulse energy used to make each row of features is given in the Figure.

The copper deposits made using this technique act as seeds for the electroless plating of copper. A mismatch in resolution between the ablated features and that of the copper seeds may require polishing of the surface after forward transfer such that copper seeds only remain within the features. A second polishing step can be applied after copper plating to eliminate any unwanted connections or growth of the copper outside of the laser ablated boundaries. The entire process is shown schematically in Figure 2. Electroless copper plating was carried out after seeding using standard recipes.<sup>16</sup> A typical recipe utilizes distilled water as the solvent, copper(II) sulfate pentahydrate as the copper source, potassium sodium tartrate as a chelator, and formaldehyde as a reductant. The pH of the aqueous solution is raised with sodium hydroxide to tune the reduction potentials to drive the plating reaction. The plating was carried out at room temperature in a 200 ml borosilicate glass beaker with magnetic stirring at 200 rpm. All solvents and plating chemicals used in this work were reagent grade. After a thin copper layer is deposited from the electroless plating process, copper electroplating, which offers much faster plating rates than electroless plating, can be carried out to build up thicker copper layers. After plating, polishing can be carried out to prepare a smooth surface with recessed conductive features, suitable for further layer build up. The process can be repeated, drilling blind vias instead of through holes, to build up layers to prepare all-glass or mixed-material multilayer structures. Modified methods can be used for making structures with embedded components in all-glass structures.

The methods described above (laser ablation followed by laser forward transfer of a thin metallic foil and then plating) can also be applied to traditional and high performance dielectric materials, as well as to the plating of various metals. Details of this work will be shared in an upcoming paper.



**Figure 2. Glass/copper process steps for preparing (A) a two-layer structure from a single piece of dielectric material and (B) the general technique for creating multiple layers.** In (A), features (wires, pads, and through holes) are made on both sides of the substrate using a laser. Copper seeds are then planted using laser forward transfer of a thin foil.

The copper droplets have good adhesion to the substrate but are too disperse to make a conductive feature. The substrate is placed in an electroless copper plating bath and copper grows on the seeds, and excess copper can be polished off to make a smooth surface suitable for further layer build up or passivation. To make multilayer architectures (B), additional layers are laminated onto the completed construct from (A), and laser etching, seeding, and plating steps are repeated.

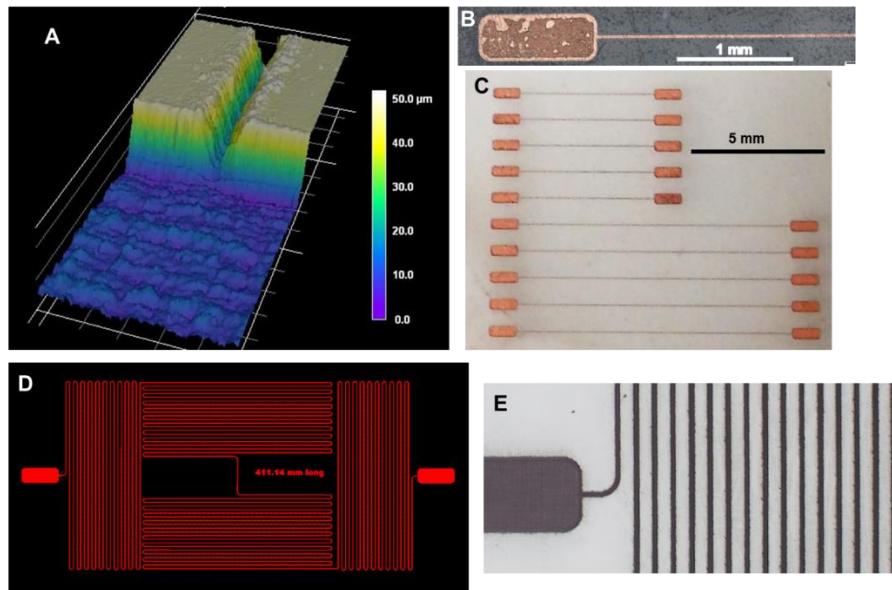
Resistivity measurements of the copper deposits after electroless plating were done using 4-point probe measurements. A simple design of two  $1000 \times 400 \mu\text{m}$  pads connected by a 5 mm or 10 mm long wire 25  $\mu\text{m}$  wide was used (Figure 3, A-C). Prior to plating, the areas of the cross sections of the wires were determined using a scanning laser microscope. The resistivity is calculated according to equation 1.

$$\rho = (V * \sigma) / (I * L) \quad (1)$$

Where V is the measured voltage across the wire,  $\sigma$  is the cross sectional area of the wire, I is the applied current, and L is the length of the feature. Profile measurements were carried out on a production scanning laser microscope. Cross sections of the engraved features were analyzed using the production analysis application. For the resistivity measurements, cross sectional areas were measured at 10 different locations in the wire to obtain an average value, which is reported with  $\pm 1\sigma$ . The wires have a cross section that is an isosceles triangle approximately 25  $\mu\text{m}$  wide and 25-30  $\mu\text{m}$  deep, with a measured cross section of  $3.53 \pm 0.38 \times 10^{-10} \text{ m}^2$ . Four point probe measurements employed a production DC power supply for both establishing currents from 50-200 mA across the plated features and recording the voltage drop. The reported resistivity values are the average of 4 measurements carried out at different applied currents for each sample to gauge the error in the resistance measurements; standard deviations of the resistance were less than 1% of the average (Table 1). The calculated resistivity values were between 1-1.5x the bulk copper value of  $1.68 \times 10^{-8} \Omega\text{m}$  (at 20 °C). The majority of the error in the resistivity measurements arises from uncertainty in the area of the wire's cross section.

**Table 1.** Resistivity measurements of 10 mm and 5 mm wires embedded in glass.

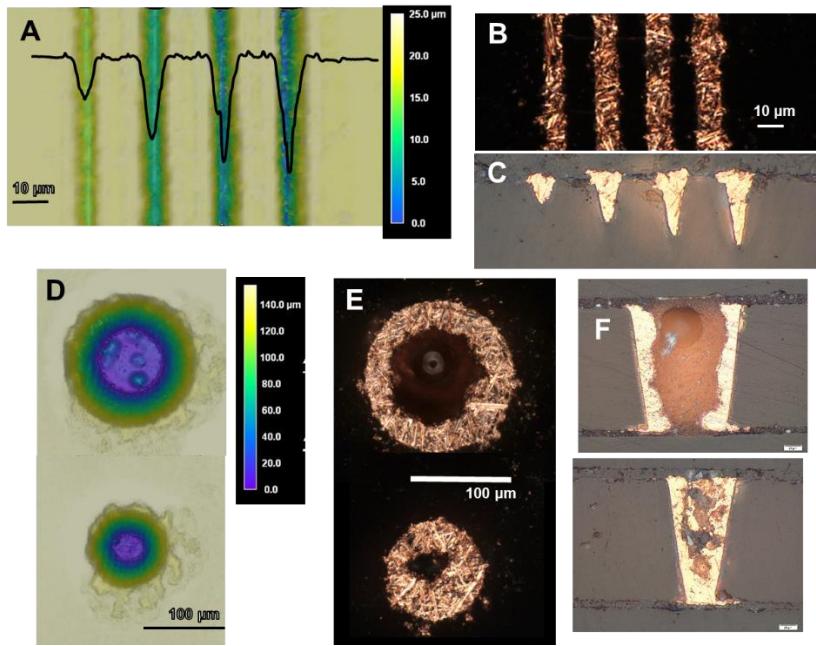
Sample	Wire Length (mm)	Resistance $\Omega$	Resistivity $\Omega \cdot m \times 10^{-8}$	% bulk value
1	10	$0.593 \pm 0.003$	$2.08 \pm 0.23$	124
2	10	$0.723 \pm 0.005$	$2.55 \pm 0.28$	152
3	5	$0.284 \pm 0.003$	$2.01 \pm 0.22$	119
4	5	$0.279 \pm 0.002$	$1.97 \pm 0.22$	117



**Figure 3. Resistivity measurements.** (A) Height measurement of the intersection of the laser-etched wire and pad. (B) Optical microscope image of a plated wire and pad. (C) Patterns with 5 and 10 mm long wires used for resistivity testing. (D-E) Long wire pattern and detail under optical microscope after laser patterning. The pitch between the lines is  $100 \mu\text{m}$  and the total length  $411.14 \text{ mm}$ .

A second pattern was employed for resistivity testing (Figure 3, D-E) that consisted of 5 mm lengths of wire separated by  $100 \mu\text{m}$  with a total length of a  $411.14 \text{ mm}$ . The dimensions of the wire were measured at 10 different positions, yielding a width of  $24.3 \pm 2.2 \mu\text{m}$ , depth of  $38.9 \pm 2.9 \mu\text{m}$  and cross sectional area of  $6.08 \pm 0.51 \times 10^{-10} \text{ m}^2$ . For these dimensions a pattern consisting of bulk copper would have a resistance of  $10.7 \pm 0.9 \Omega$ . Resistance measurements using a multimeter for 4 of these patterns gave a value of  $24.1 \pm 0.6 \Omega$ , about 2.25 times the value expected for bulk copper in this geometry.

A major advantage to having wires embedded in a dielectric material is the ability to finely control the geometry of individual wires and the pitch between wires, thereby enabling a more predictable total Cu volume for any given pattern. Figure 4 demonstrates wires having a very fine pitch and controllable depth. The lines are 1–4 passes using  $3 \mu\text{J}$ , 1 MHz, 500 mm/s on the company system. After 1 pass the trench is about  $8 \mu\text{m}$  wide and  $7 \mu\text{m}$  deep. The width increases somewhat upon subsequent passes, and the increase in depth saturates with the number of passes such that at the 4<sup>th</sup> pass the trench is  $9.5 \mu\text{m}$  wide and  $20 \mu\text{m}$  deep. The lines are separated by about  $10 \mu\text{m}$ . Figure 4 also demonstrates plated through holes of  $133$  and  $87 \mu\text{m}$  diameter (at the laser entrance side) in  $150 \mu\text{m}$  thick borosilicate glass. In both cases the sidewall angle is around  $82^\circ$ , such that at the exit the diameters are  $85 \mu\text{m}$  and  $41 \mu\text{m}$ , respectively. Through holes have also been drilled in  $50 \mu\text{m}$  thick glass with a top diameter of  $40 \mu\text{m}$  and an exit diameter of  $16 \mu\text{m}$  using the company system (not shown).

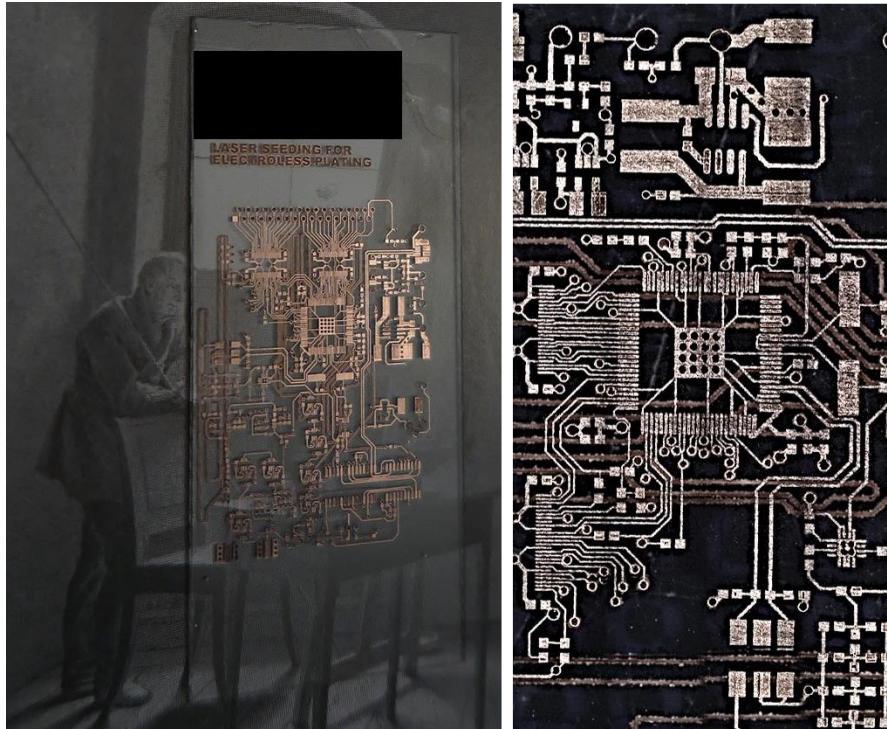


**Figure 4. A-C. Fine pitch lines and variable via sizes. Trenches in the glass are made with 3  $\mu$ J, 1 MHz, 500 mm/s and 1-4 repeats of the pattern on the company system. A. Height measurements of the etched glass. B. Dark field optical microscope image of the wires. C. Cross sections of the wires. D-F. Through holes in 150  $\mu$ m thick borosilicate glass with 150 and 100  $\mu$ m top diameters.**

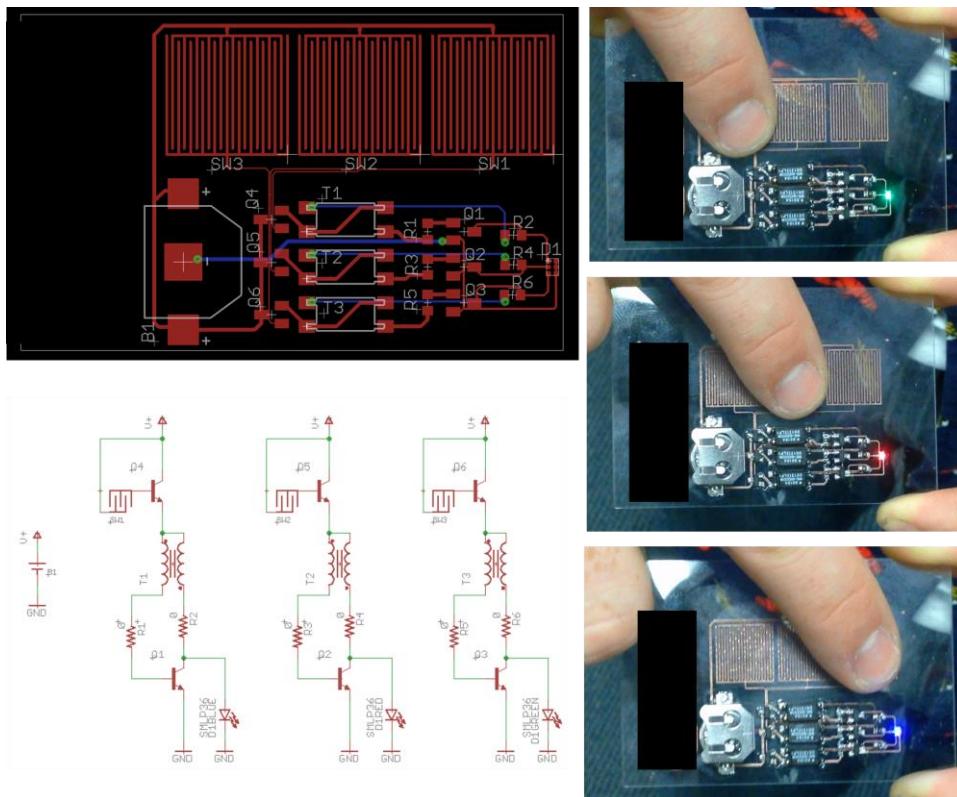
Applying the laser-based glass etching and copper seeding methods outlined above, a two-sided PCB pattern measuring 20 x 35 mm was prepared (Figure 5). The pattern is an actual circuit design, albeit scaled down to ~25% of the original size so that it can fit on a 22 x 50 mm borosilicate glass coverslip 150  $\mu$ m thick. The smallest features in this design are ca. 35  $\mu$ m wide. The pads, wires and alignment points of the design were machined using a single set of laser parameters, utilizing a 7  $\mu$ m crosshatch pattern within the individual polygons. Next, the vias were drilled using a different set of parameters. The piece was flipped over and aligned using the alignment marks made on the top of the glass piece, and the wires, pads and additional text on the bottom were machined. After the forward transfer process, both the top and bottom were gently polished to remove excess copper from the surface, leaving only copper seeds in the laser machined areas. Plating was carried out in an electroless plating bath.

To illustrate the capabilities and gain insight as to whether the adhesion of copper to a glass substrate holds up to direct heat from a soldering iron, a two-layer circuit board was designed and built. This circuit, known as a “Joule Thief,” operates in a similar way to a boost converter, in that it takes a smaller DC voltage and uses inductive spiking to generate a larger voltage via a transistor used for switching and a transformer. The design has three parallel circuits, which control an individual color of a common cathode RGB LED, and a resistive touch pad activates each circuit. A 1.5 V button cell battery was used to power the circuit, and the switching frequency was measured to be approximately 400 kHz. Although the circuit itself has a relatively low parts count and does not require a two-layer PCB design, a two layer board was designed to demonstrate the capabilities of creating plated through-holes. Trace widths on the board range from 100 – 400  $\mu$ m (4 mils to 16 mils), which were created without issue using the methods described above.

During the assembly of the circuit board, the quality of the adhesion of copper to the glass substrate was observed to be similar to that of copper on FR4. There were no traces or pads that peeled off and some pads went under multiple temperature cycles (up to approximately 300 °C) with no issues. The design of the board and photographs of the completed board operating are shown in Figure 6.

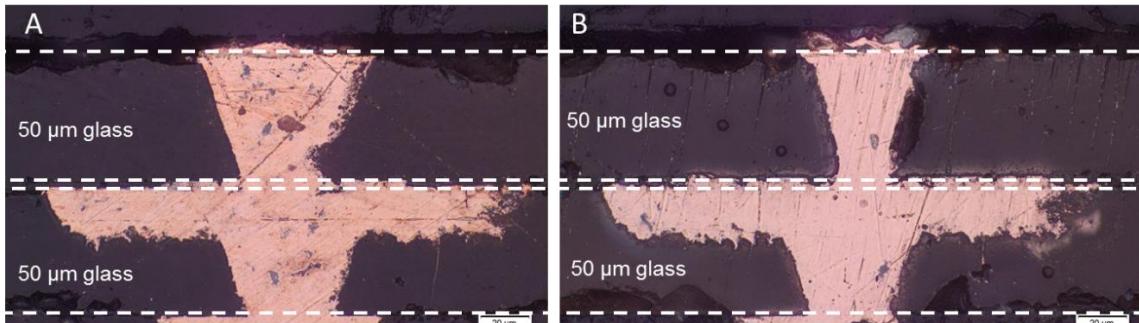


**Figure 5.** Images of a two-sided demo pattern on a 150  $\mu\text{m}$  thick glass cover slip. The total pattern is approximately 20 x 35 mm and the glass is ablated using a 7  $\mu\text{m}$  crosshatch pattern within the individual polygons. Left: Photo of the plated design imposed against a grayscale image. Right: Composite optical microscope image detailing a portion of the pattern.



**Figure 6.** Resistive touchpad RGB LED demonstrator, plated on 1 mm thick borosilicate glass. In the upper left picture the red features are on the front side of the board, the green circles are through holes, and the blue features are on the back side of the board. The series of photographs shows that each touch pad activates a single LED.

Multilayer PCB architectures can be built up by aligning and glueing additional layers of glass onto plated glass layers and repeating the methods outline above. Figure 7 demonstrates drilling and plating of blind vias in order to build up multiple glass layers. A pattern with a 200  $\mu\text{m}$  diameter pad with 50  $\mu\text{m}$  diameter through via was made in 50  $\mu\text{m}$  thick glass using the company system operating at 1 MHz, 3-4  $\mu\text{J}$  with a feed rate of 1 m/s. The piece was then seeded and plated as described above. Optical glue was spin coated onto a second piece of glass such that the thickness of the glue was less than 5  $\mu\text{m}$ , and this piece of glass was then affixed to the plated piece. The pattern was aligned and blind vias drilled such that the glass was removed without damaging the copper pad underneath. Blind via drilling with the company system was carried out using parameters similar to those used for the through holes. Alternatively, the high reflectivity of copper and the high absorption cross section of glass to mid-IR wavelengths makes the company's CO<sub>2</sub>-based microvia platform an ideal solution for blind via drilling in this application. 50  $\mu\text{m}$  top diameter vias with 35  $\mu\text{m}$  bottom diameter were drilled using the company system. For both blind via drilling methods the vias prepared were amendable toward forward transfer of copper and subsequent plating, as shown in Figure 7.



**Figure 7. Blind vias and multilayer stack using 50  $\mu\text{m}$  thick glass. The dashed lines indicate the edges of the glass pieces and middle glue layer. In both A and B, the bottom 50  $\mu\text{m}$  thick glass was machined using a company system to prepare an embedded pad 20  $\mu\text{m}$  deep and 200  $\mu\text{m}$  in diameter. A through via was then drilled from the bottom of the pad, and the piece seeded and plated using laser forward transfer followed by electroless plating. After gluing on the top 50  $\mu\text{m}$  thick glass, blind vias were drilled using either the company 1 system (panel A), or the company's CO<sub>2</sub>-based microvia platform (panel B).**

### Comparison with Standard Practices

Besides describing a unique method for creating PCBs and IC packaging with few of the current lithographic and wet process constraints, the process described in this paper represents a facile method for the introduction of glass dielectric materials into traditional PCB fabrication lines. As an example, a multilayer board with a high-frequency glass layer could be built up by first applying the etching, seeding, and plating techniques described herein to a thin glass substrate, followed by lamination of additional glass or more traditional dielectrics onto the glass layer. The laminated layers would then be etched, drilled, and plated using typical processes. Furthermore, the method can be modified to prepare embedded components in all-glass structures.

An important point of comparison between laser seeding for electroless plating and typical PCB fabrication techniques is that unlike typical processes, the laser seeding for electroless plating process requires no photolithography steps, no catalyst for electroless plating, and no copper etching steps:

- Rather than undertaking photolithographic steps, the pattern of wires, pads and vias is directly etched by laser ablation into the dielectric material. The line width and spacing of the features is limited by the processing laser, process parameters, and the physics of the laser-material interaction. Rather than developing an entirely new chemical/material set for further advancing the miniaturization of PCB features, advances in laser technology, pulse shaping, and beam positioning can drive this trend.
- Tin and palladium chemistry are removed from the electroless plating process. Cleaning, conditioning, microetching, catalyst pre-dip, catalyst activation, and acceleration steps are all eliminated from the electroless plating process line. Hazardous and costly chemicals are removed from the process stream.
- There is no copper etching required. The copper that is deposited represents all of the copper in that layer of the board.

It is apparent then that this process represents a “green chemistry” approach, *i.e.*, an approach that aims to minimize both the use and disposal of hazardous materials: the best green chemistry approaches are those that avoid hazardous materials altogether. The process also presents the opportunity for substantial base material savings, with glass being up to 100-fold more affordable than current high frequency dielectrics, and energy savings through the absence of thermal lamination

processes. The best analysis would be a total life cycle analysis for an all-glass or glass core PCB to explore the process rates, throughput, and energy and material requirements for the laser seeding process compared to those of typical PCB fabrication. An effort is currently underway to make this analysis, but the biggest difference between the two processes is readily apparent: there are currently no methods in place for incorporating glass dielectrics into traditional PCB fabrication lines, and the methods described in this paper offer a pathway to make this possible.

## Conclusions

This paper details a new methodology for the plating of conductive features onto glass dielectrics. A laser is used to ablate material from a glass substrate in the desired pattern, and copper is “seeded” into these features using laser-induced forward transfer of a copper foil. The copper droplets, or seeds, that are deposited act as sites for the growth of copper in electroless plating processes. Using thin borosilicate glass substrates, we demonstrated this process for the preparation of conductive thin wires, through holes, bind vias, and multiple-layer architectures. The process can be applied toward dielectrics other than glass as well. Material costs, hazardous waste, and waste recycling streams are significantly reduced compared to traditional PCB fabrication processes. Future work will be aimed at better understanding the throughput and yield of this process, especially with comparison to typical PCB fabrication.

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## Outline – DoE Overview

- Why we're interested in glass
- Basic process- 1 layer
  - *Laser-induced forward transfer and examples*
- Advanced Process – 2 layers
- Advanced Process – Multiple layers

## Glass Advantages

**Glass is great for high-density, high-frequency applications:**

- Low cost
- Very stable in terms of electrical properties, moisture absorption, and aging
- CTE similar to that of silicon, making it ideal for IC packaging
- Dielectric constant of glass is, in some instances, lower than that of FR-4
- low loss tangent



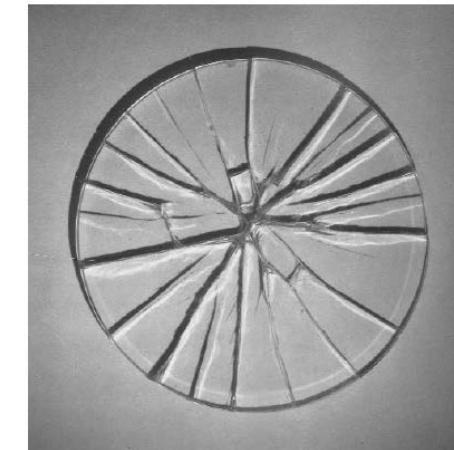
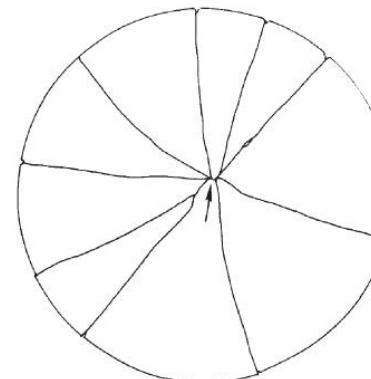
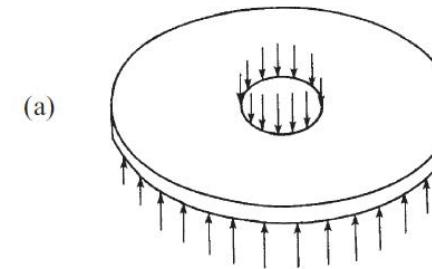
Ref: [1]

Xiaoyun Cui, PhD thesis, Loughborough University, 2010.  
Lampeonneud, C. et al. *Journal of Crystal Growth*, 1992, 121(1-2), 223-234.  
Pulker, H.K., Coating on Glass. 1984, Elsevier.

# Glass Disadvantages

## Difficulties working with glass:

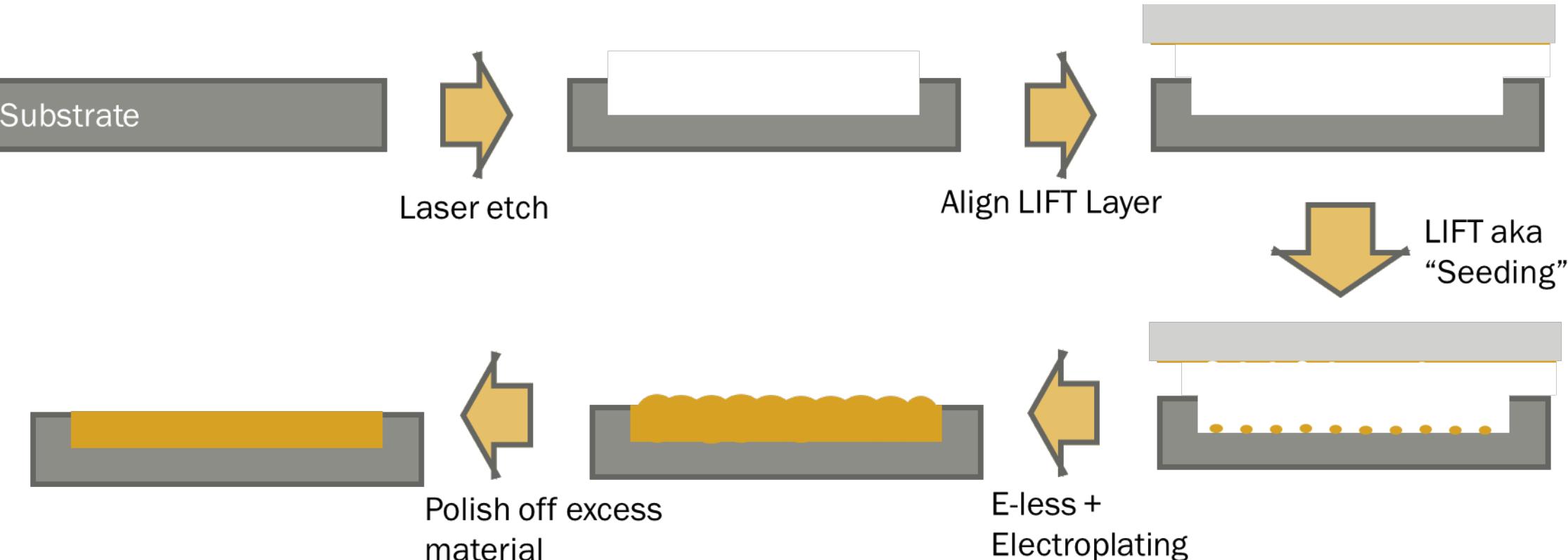
- Chemical and mechanical incompatibilities between brittle, stiff glass and the metal, such as CTE incompatibility and strong interfacial stresses.
- Smooth glass surfaces present no possibility of mechanical interlocking, so metal films can easily separate from the substrate.



(b)

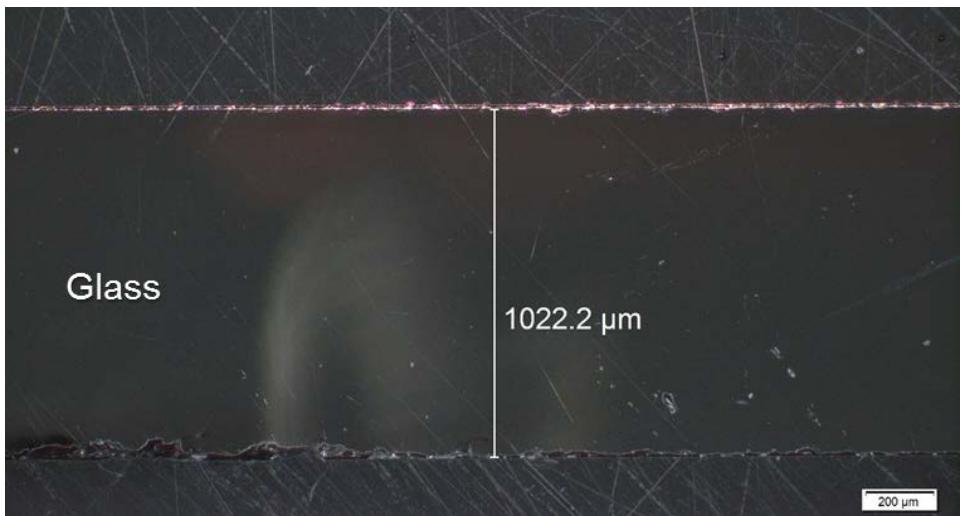
(c)

## “Seeding” Process

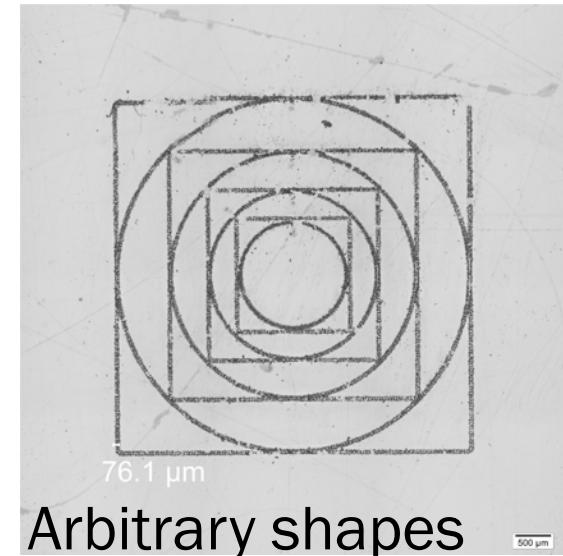
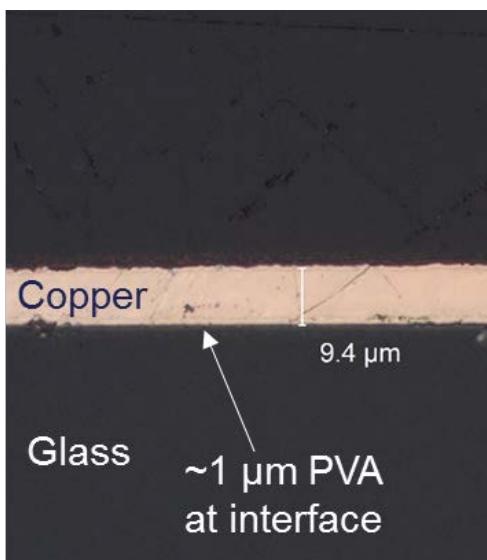


## Laser-Induced Forward Transfer (LIFT)

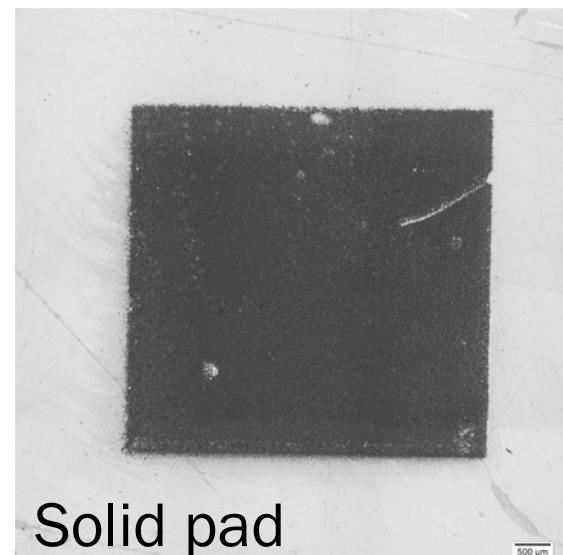
(1) A copper foil is laminated onto a 1 mm thick piece of borosilicate glass.



(2) A laser focused through the glass onto the copper foil transfers copper onto a receiving substrate.



Arbitrary shapes



Solid pad

## Laser/Material Simulation

25um glass (aSiO<sub>2</sub>\_532nm)

Epoxy - 1um

10um copper (Cu\_532nm\_T)

Air- 50 um

Glass - receiving substrate, 25 um thick (aSiO<sub>2</sub>\_532nm)

General parameters:

Initial mesh size = auto

Highest level of mesh refinement = 4

# proc = 4

Initial temp = 293 K

M2 = 1.2

Beam profile = Gaussian

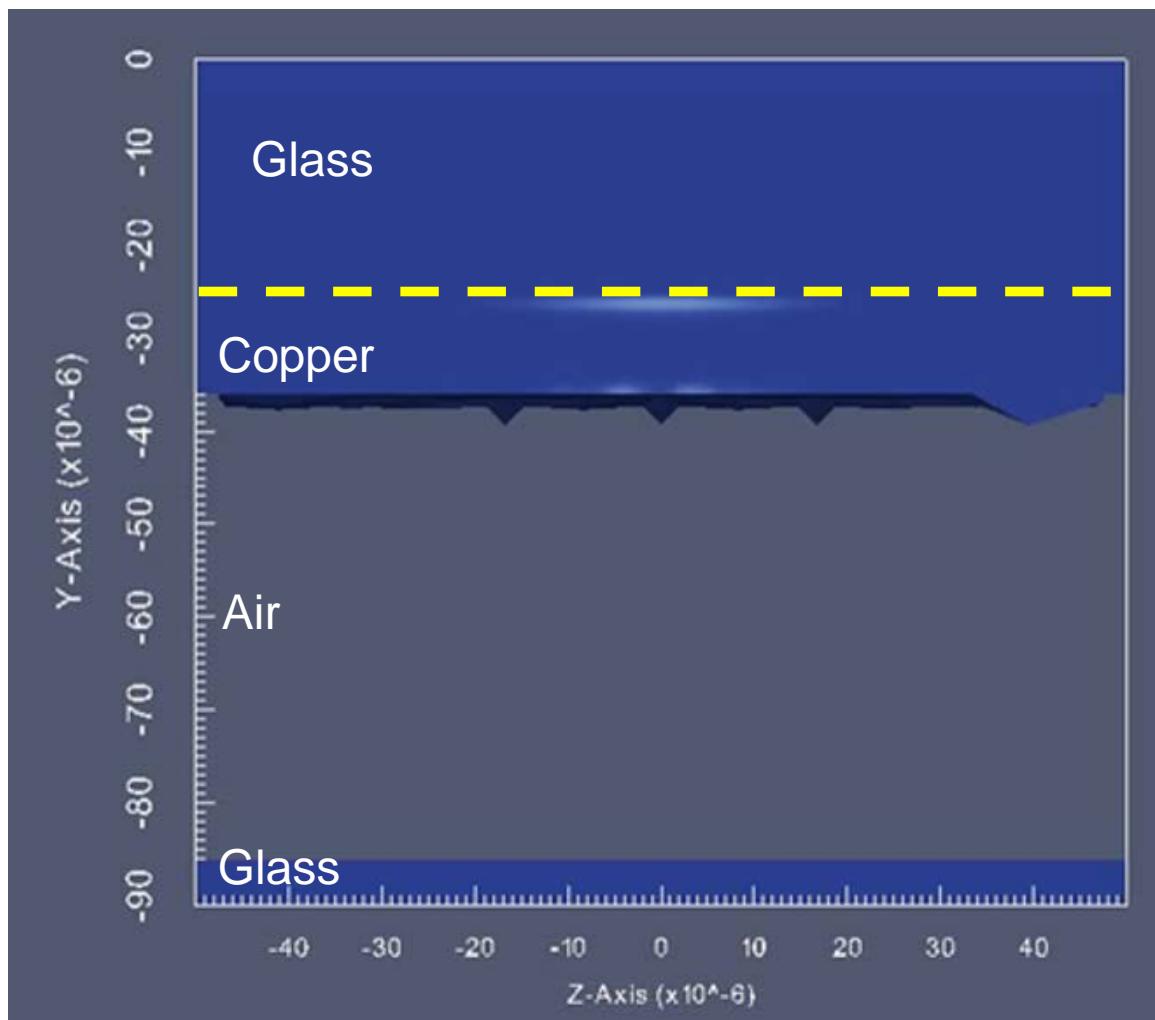
Wavelength = 532 nm

Energy = 175uJ

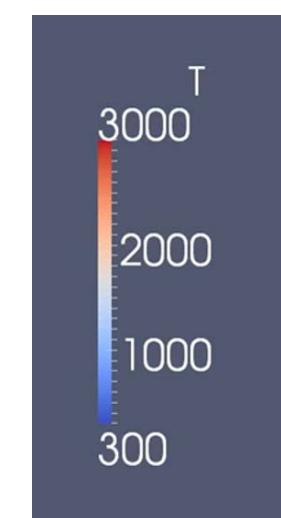
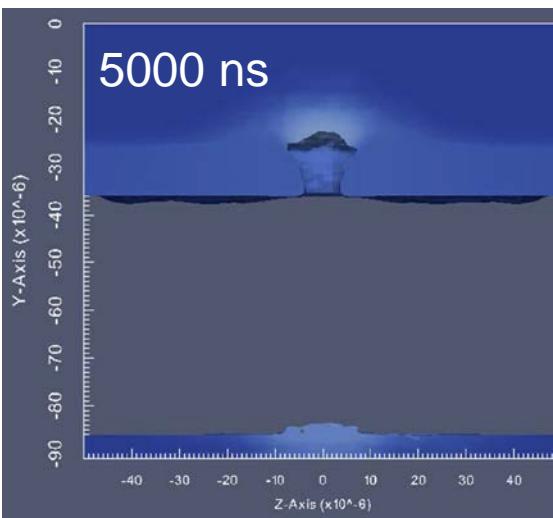
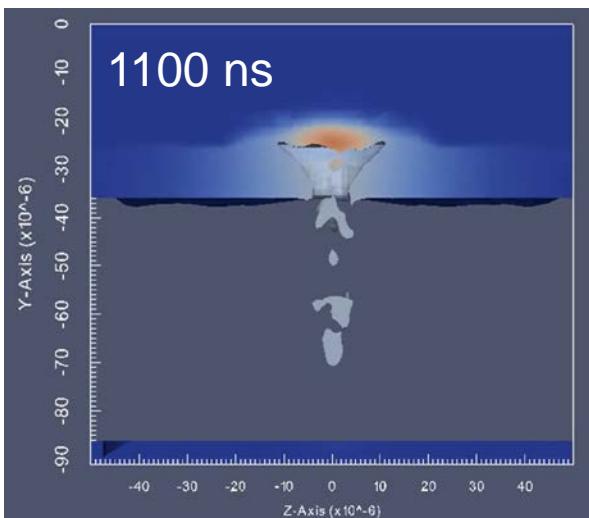
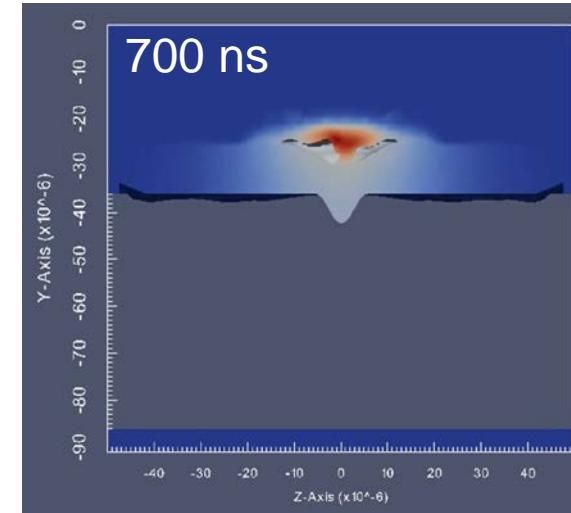
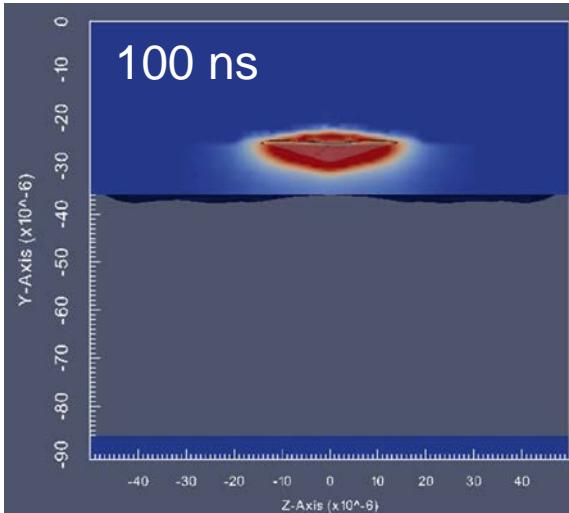
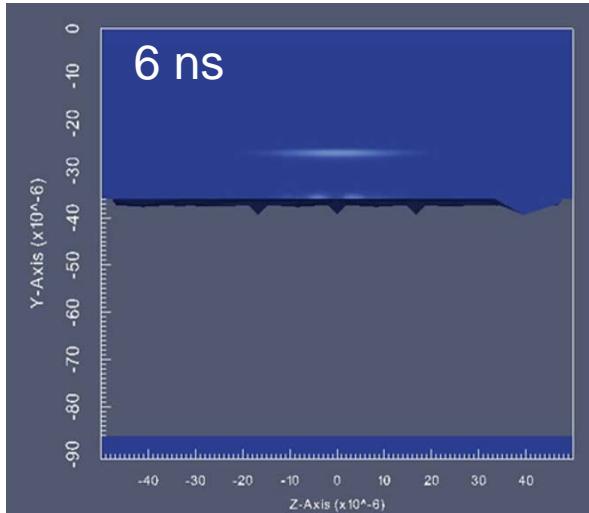
Spot size diameter at top of work surface = 31.4um

Temporal shape = Gaussian

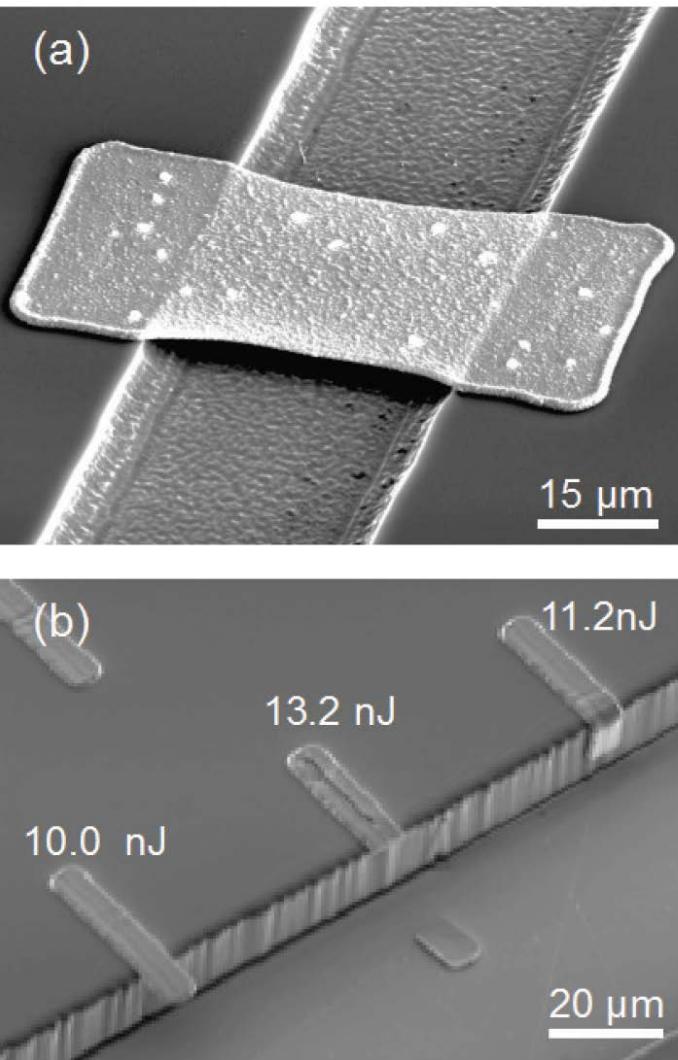
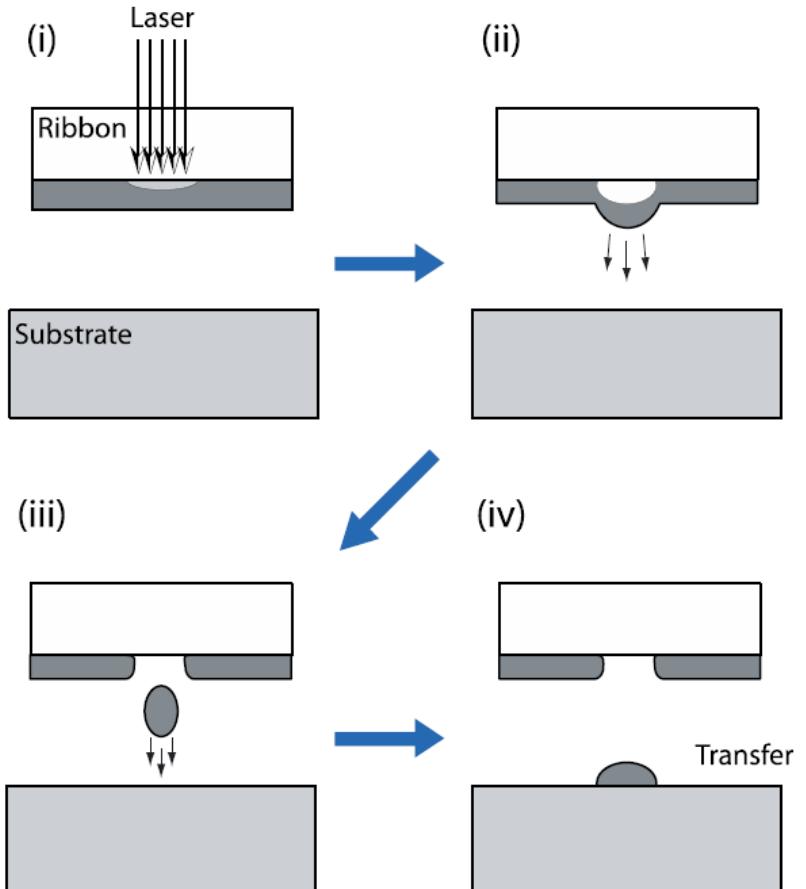
Pulse width = 11 ns



## Laser/Material Simulation



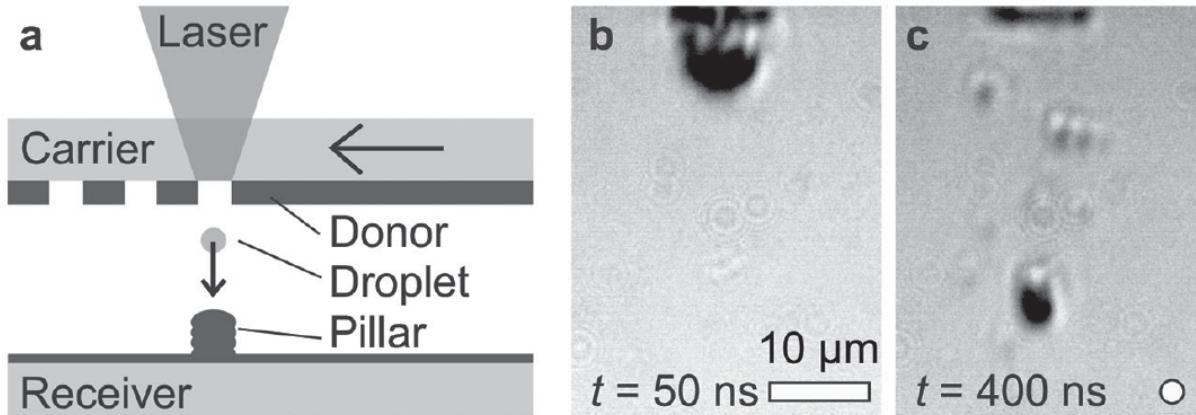
## LIFT Example #1



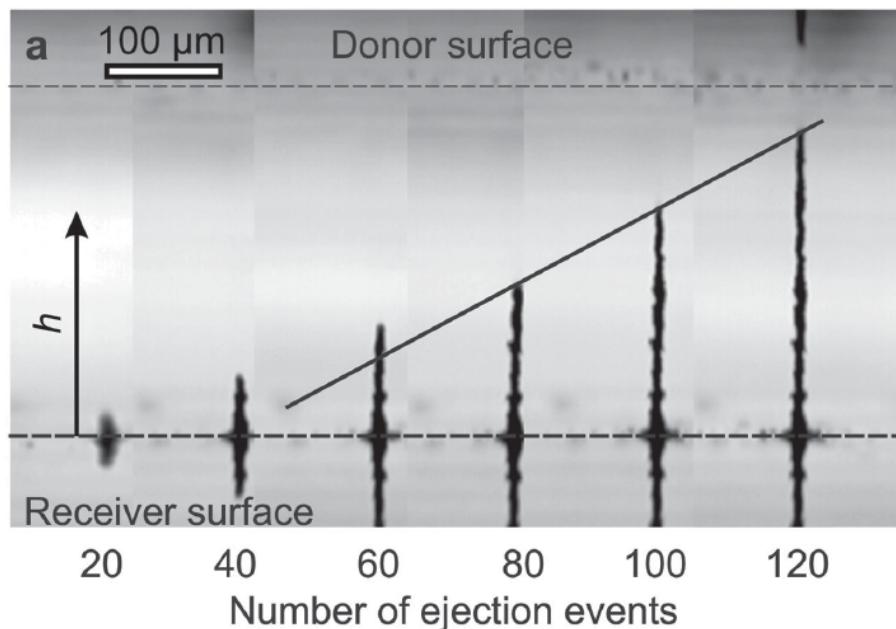
Single pulse LIFT of Ag nanopastes to make bridging, cantilevered, and folded structures.

Piqué and Kim, *JLMN* 2014, 9 (3), 192-196.

## LIFT Example #2



Snapshots of LIFT in action.



Using LIFT to build high aspect ratio copper pillars.

Visser et al., *Adv. Mater.* **2015**, 27, 4087-4092.

## Lasers Used In DoE Trials

### Glass Ablation

*Company system:* 515 nm, 800 fs pulse duration, 1 MHz max pulse repetition rate, ~10 µJ max pulse energy, 12-15 µm focused spot

*Company system:* 9.3 µm CO<sub>2</sub> laser

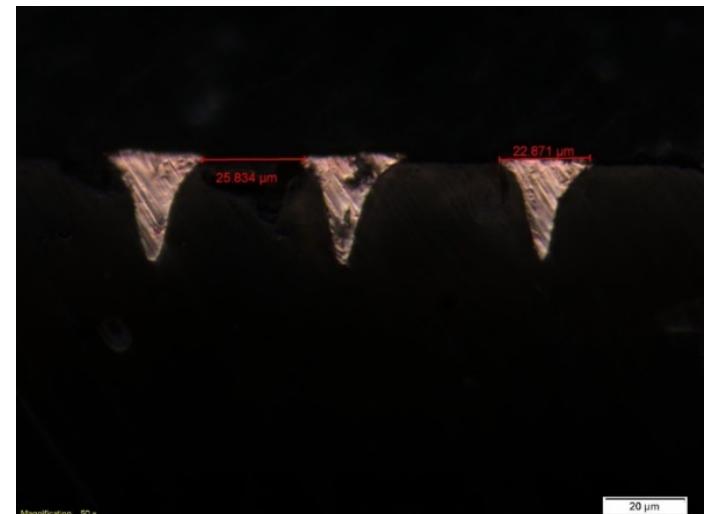
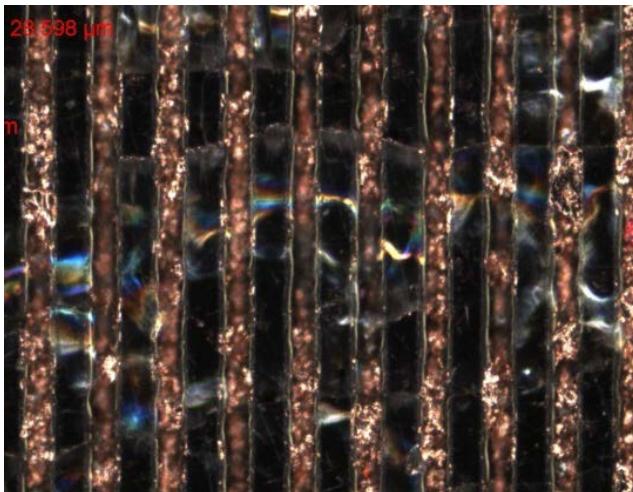
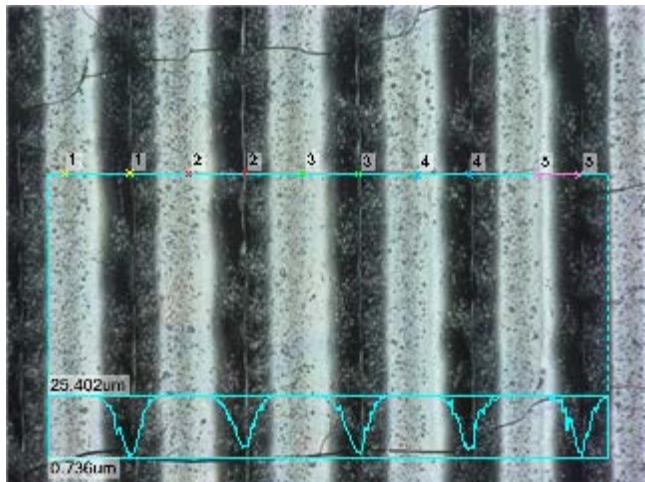
### LIFT

*Company system:* 355 nm, up to 90 kHz, ~10 ns, max. 11 W

*Lab system:* 532 nm, 30 kHz, max. 200 µJ/pulse, ~11 ns pulse duration, 30-40 µm diameter focused spot



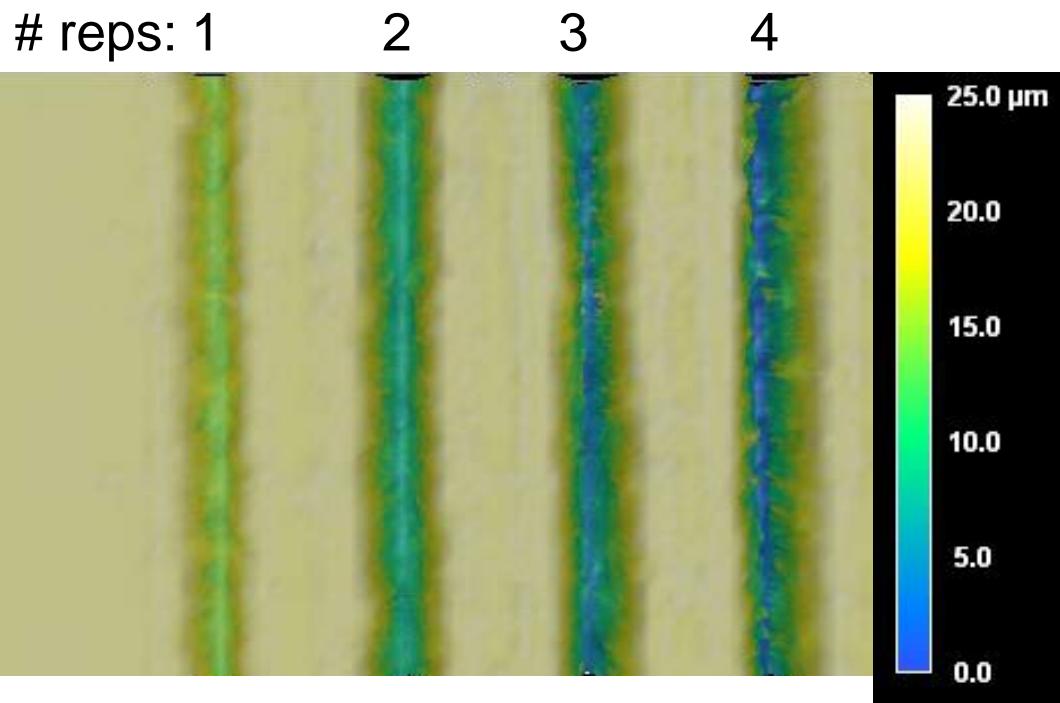
## Ablation, Seeding, Plating



Borosilicate glass sample: 25/25  $\mu\text{m}$  L/S and about 25  $\mu\text{m}$  deep.

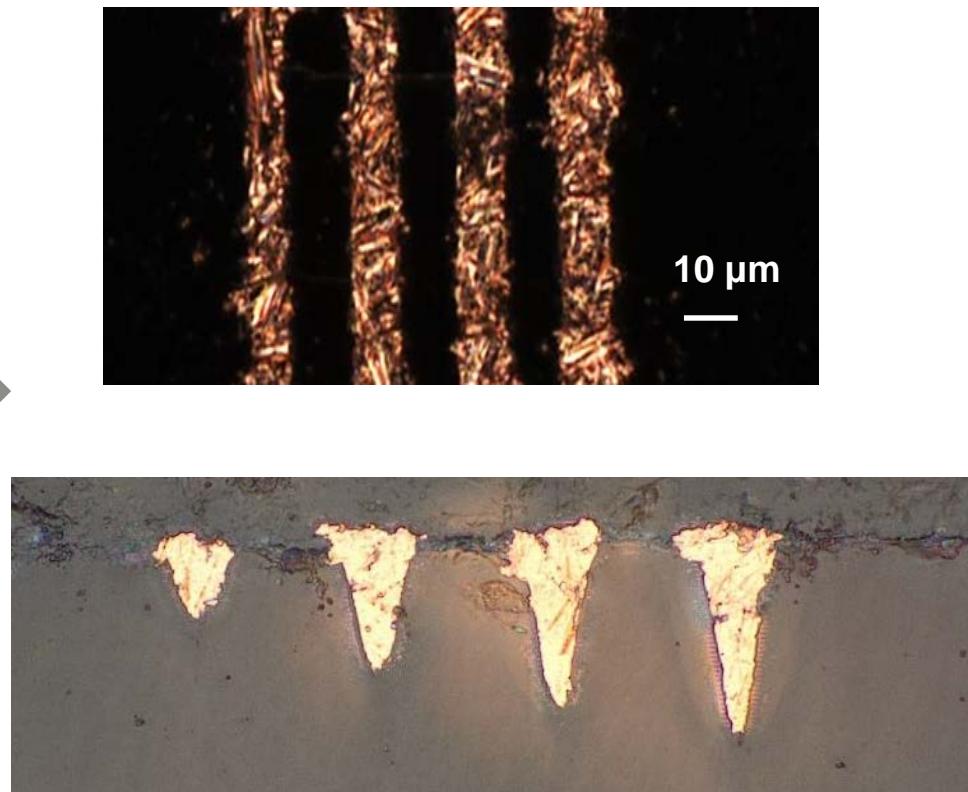
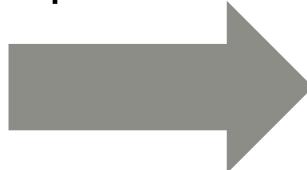
Trials have successfully demonstrated features down to  $\sim 5 \mu\text{m}$  wide/ 5  $\mu\text{m}$  spacing.

## Ablation, Seeding, Plating

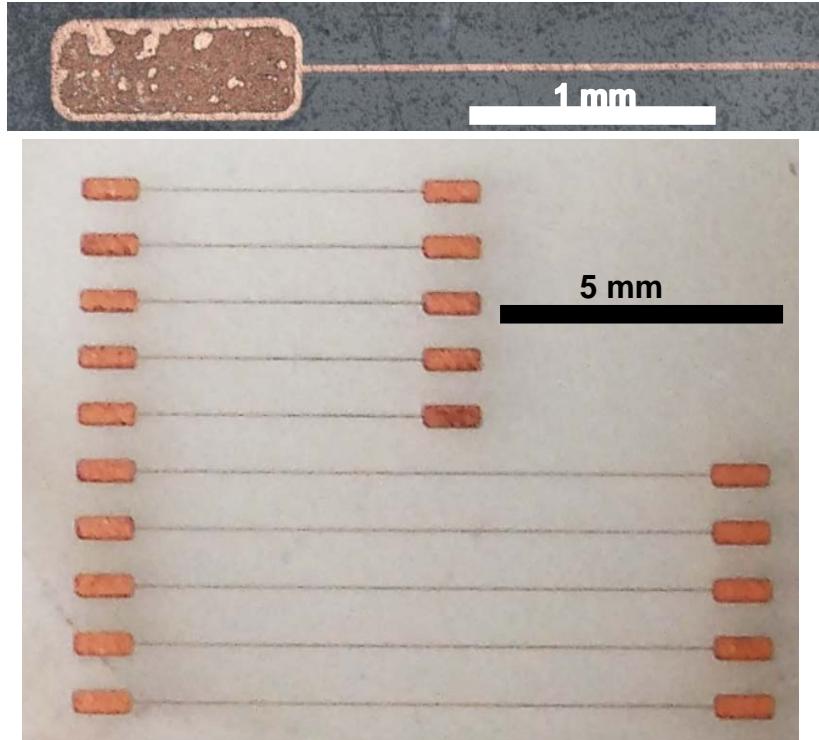
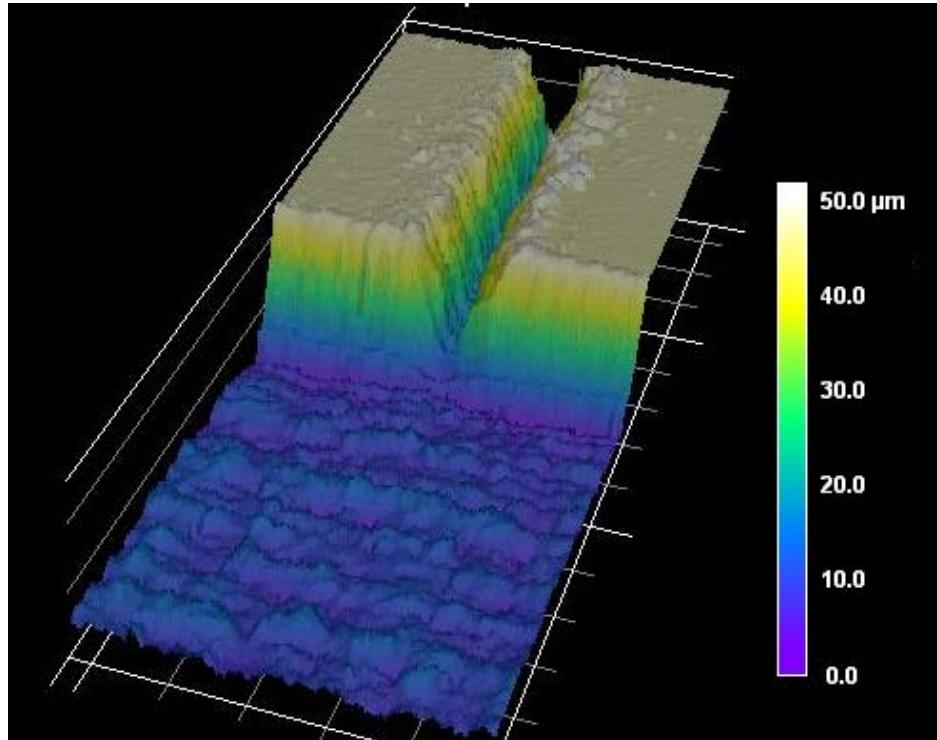


515 nm, 800 fs, 1 MHz, 3  $\mu\text{J}$ , 500 mm/s

Seeded  
and  
plated

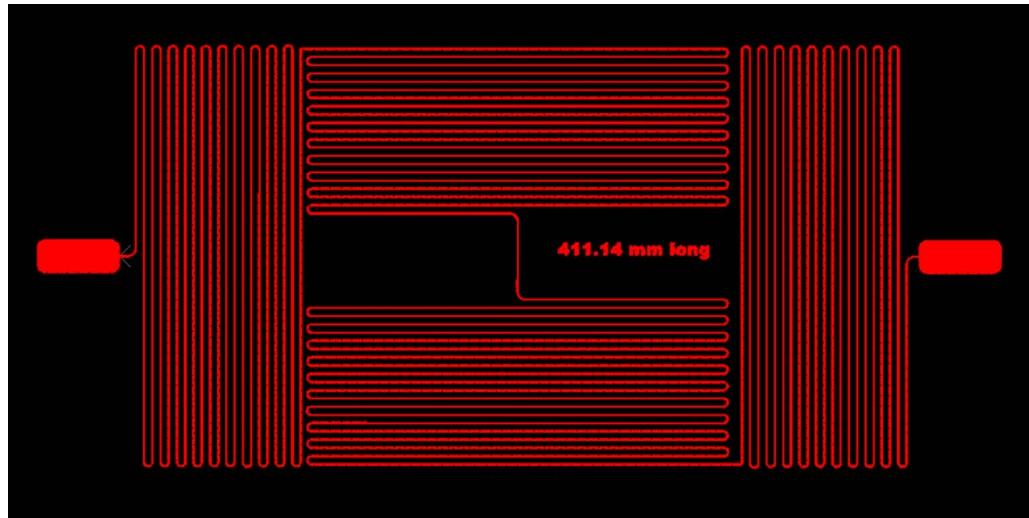


## Conductivity Tests

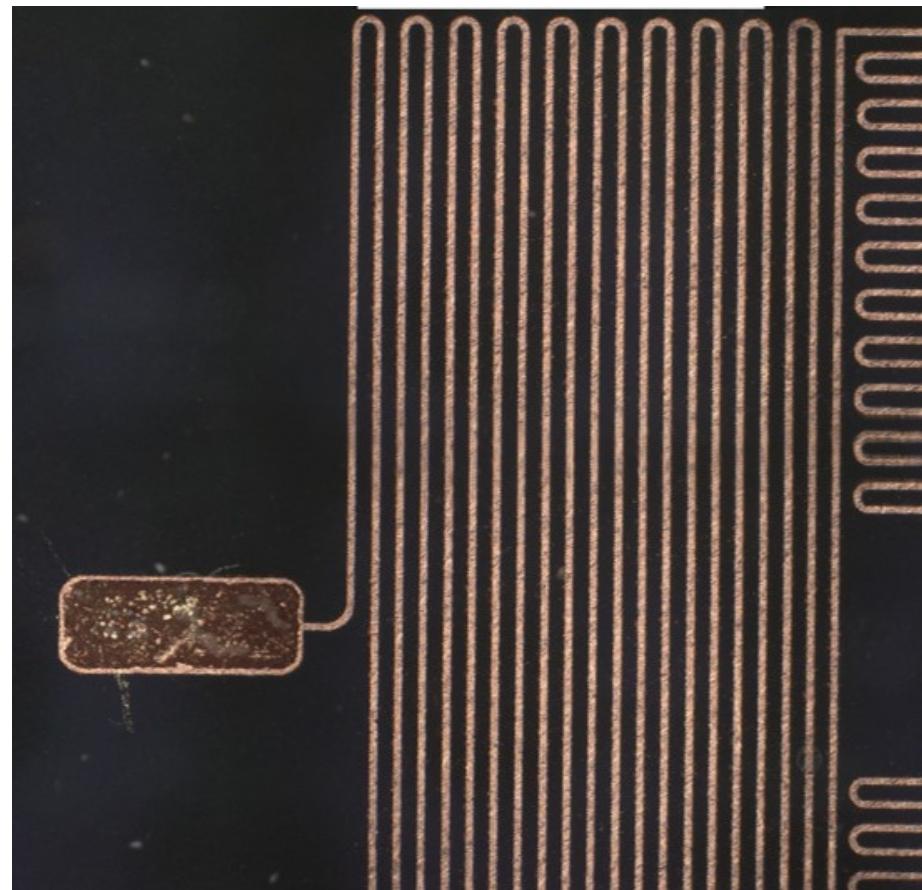


4 point probe resistivity measurements gave values 1 – 1.5x that of bulk copper for 5 and 10 mm wires.  
The wires are ~25  $\mu\text{m}$  wide.

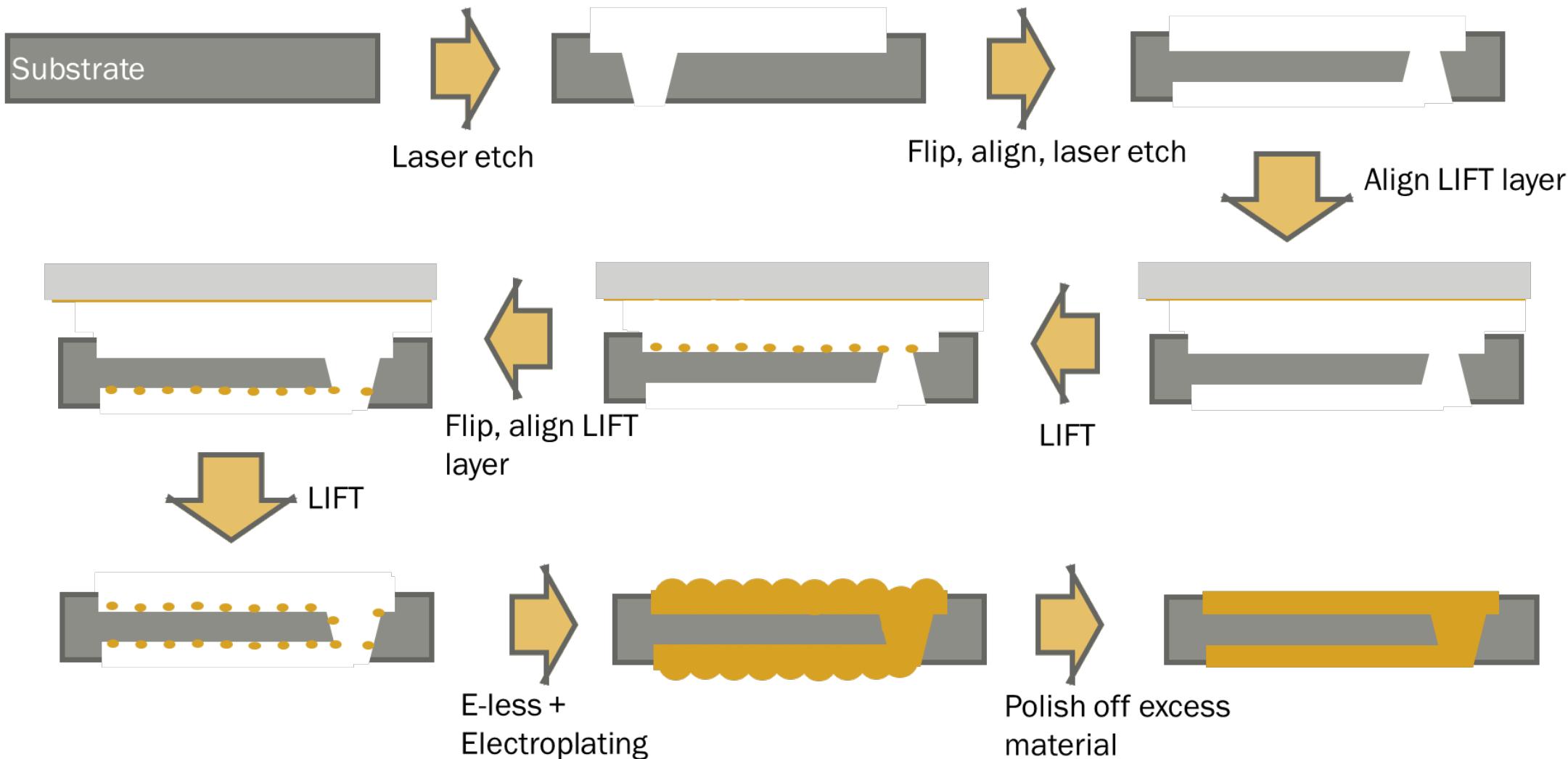
## Conductivity Tests



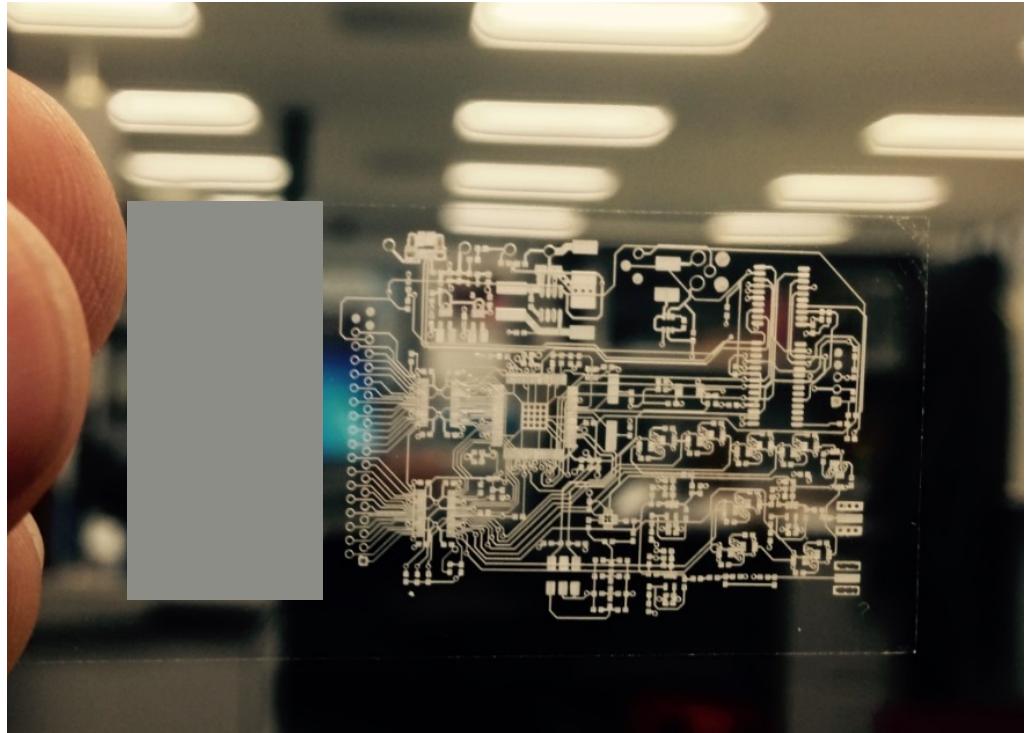
For these dimensions a pattern consisting of bulk copper would have a resistance of  $10.7 \pm 0.9 \Omega$ . Multimeter resistance measurements for 4 of these patterns gave a value of  $24.1 \pm 0.6 \Omega$ , about 2.25 times the value expected for bulk copper.



## Advanced Patterning Process

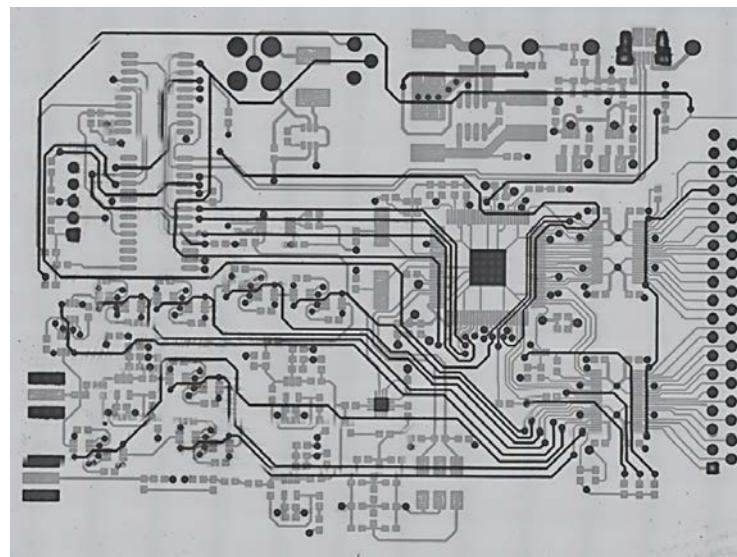
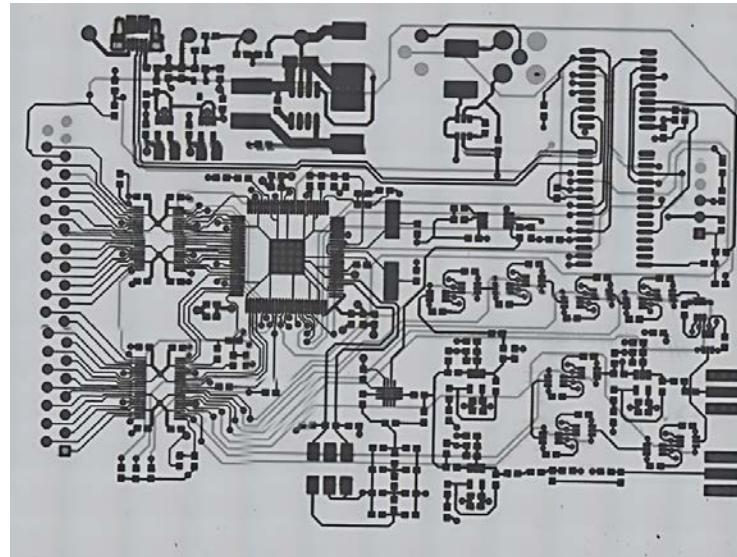


## Advanced Patterning Process



Glass etching with 515 nm, 800 fs, 1 MHz,  
3  $\mu$ J, 500 mm/s.

Front, back, and through holes on 150  $\mu$ m  
thick borosilicate glass.



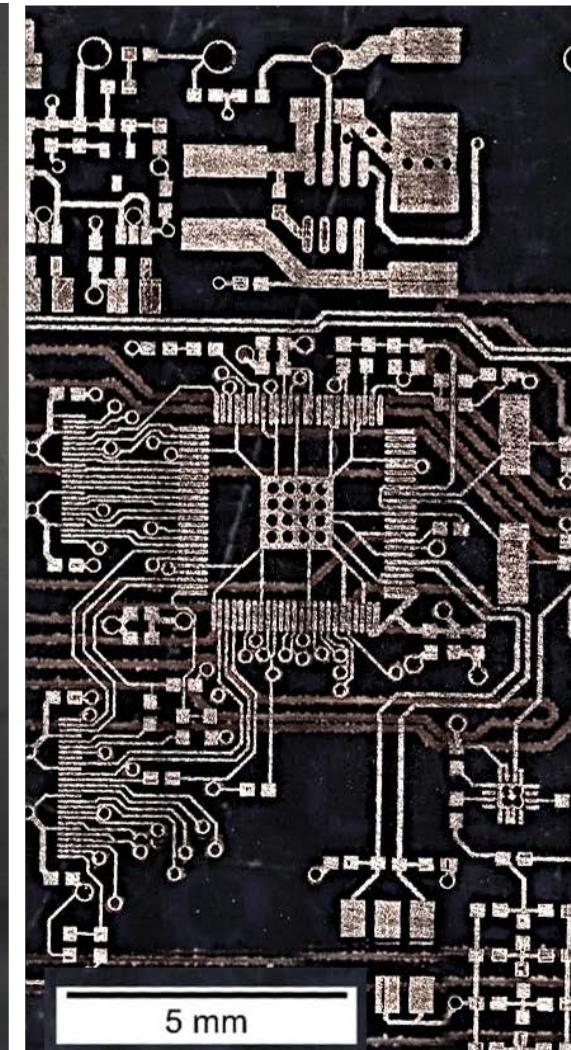
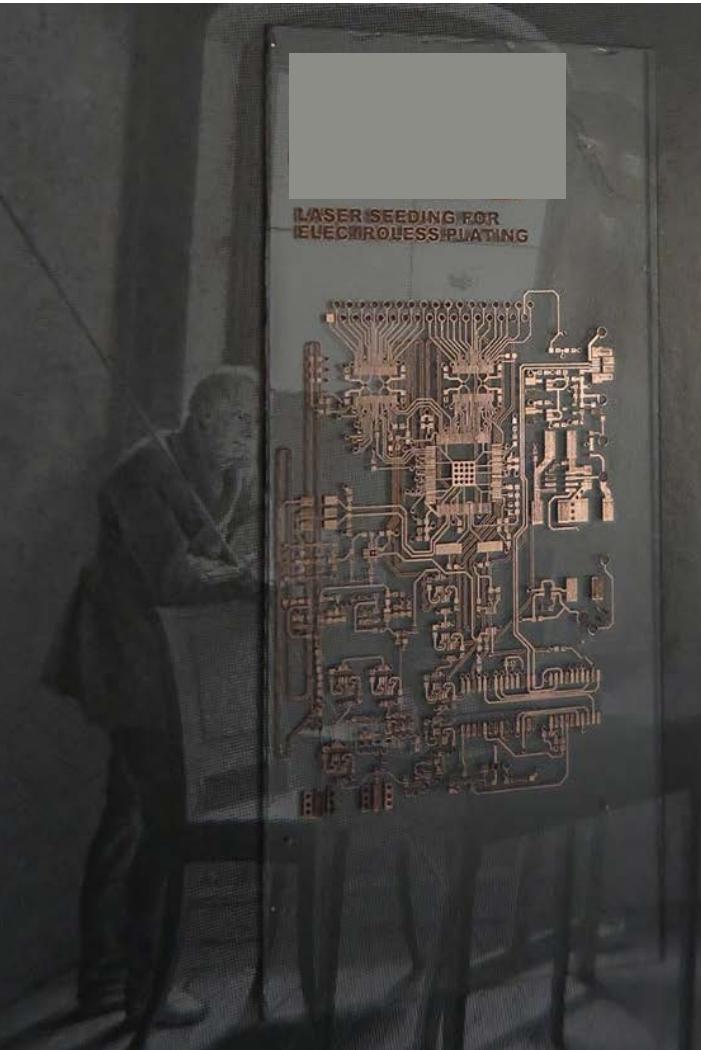
Composite optical  
microscope images

## Advanced Patterning Process

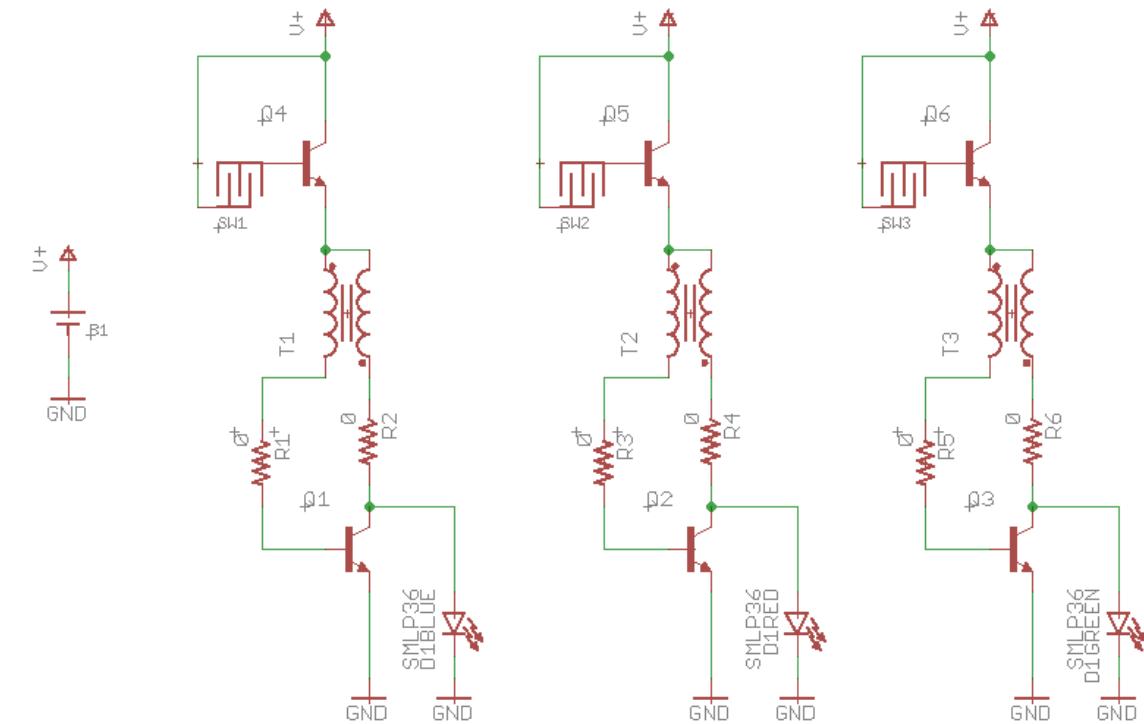
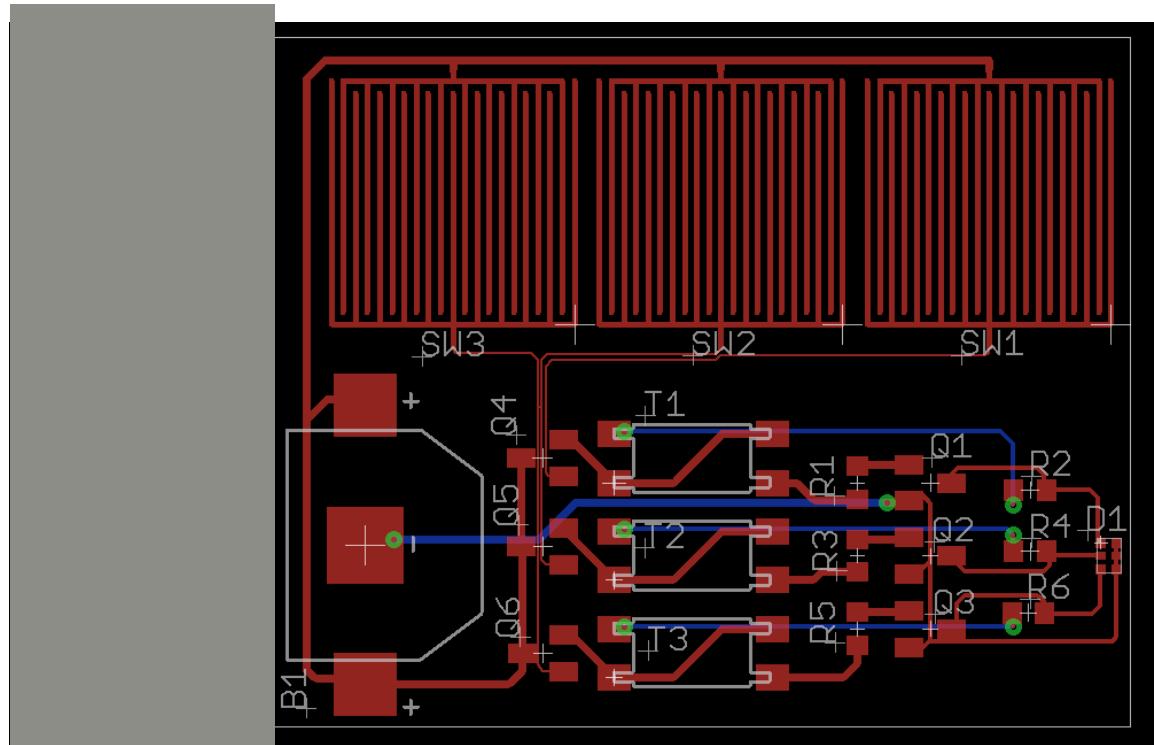


↑ Plated through holes in 150 µm thick borosilicate glass. The holes are plated in an in-house electroless plating bath without electrolyte monitoring.

Plated 2-sided circuit board design. →

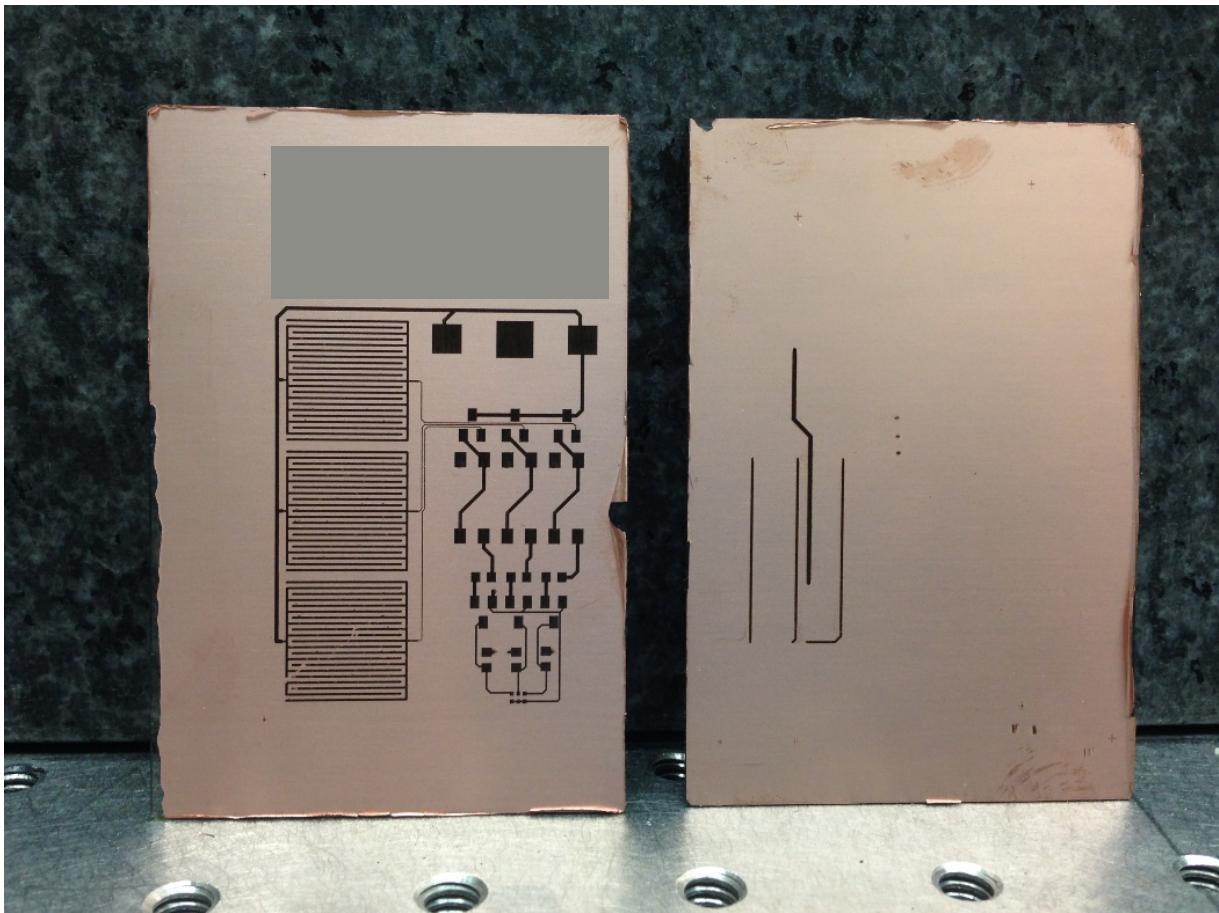


## Functional Demonstrator

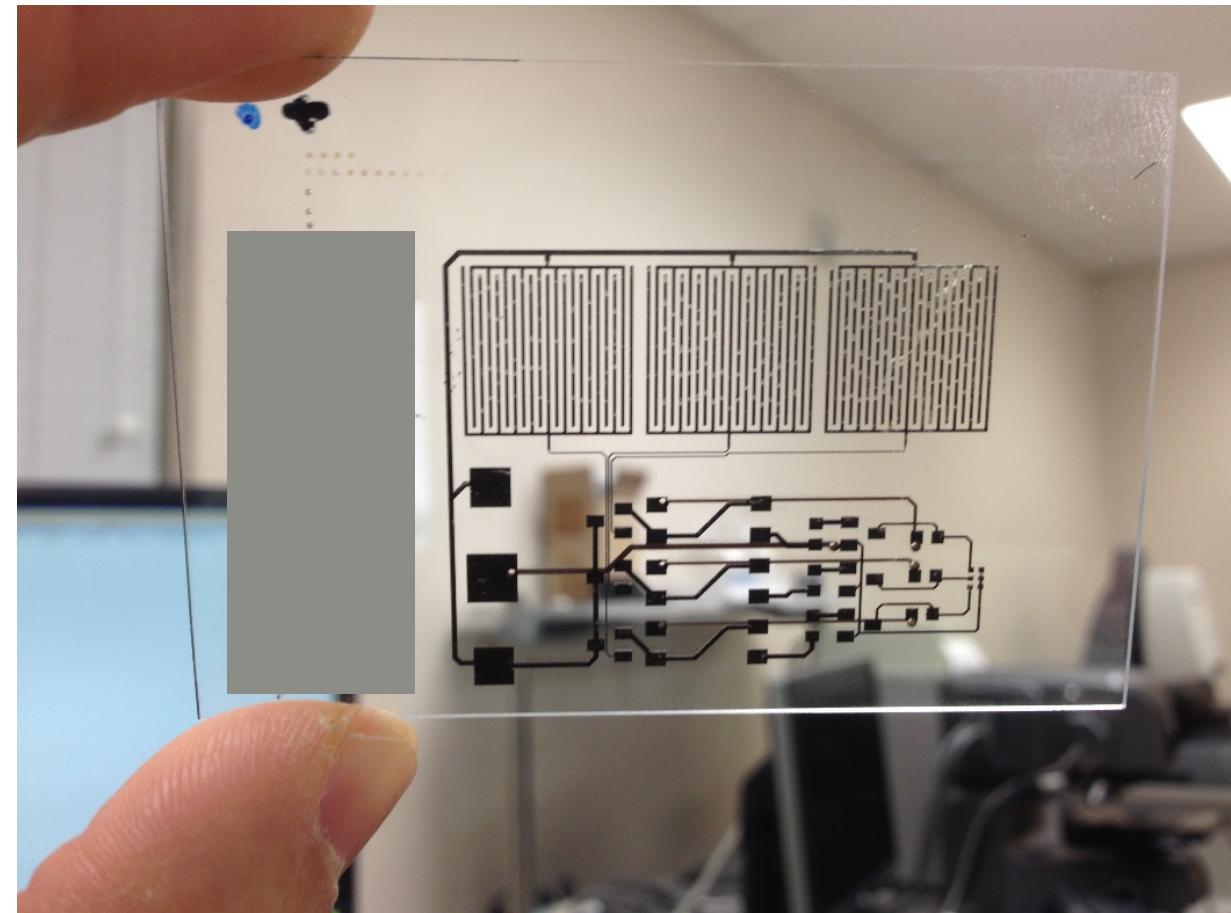


Design for RGB LED “touch pad” demonstrator.

## Functional Demonstrator



Donor substrates



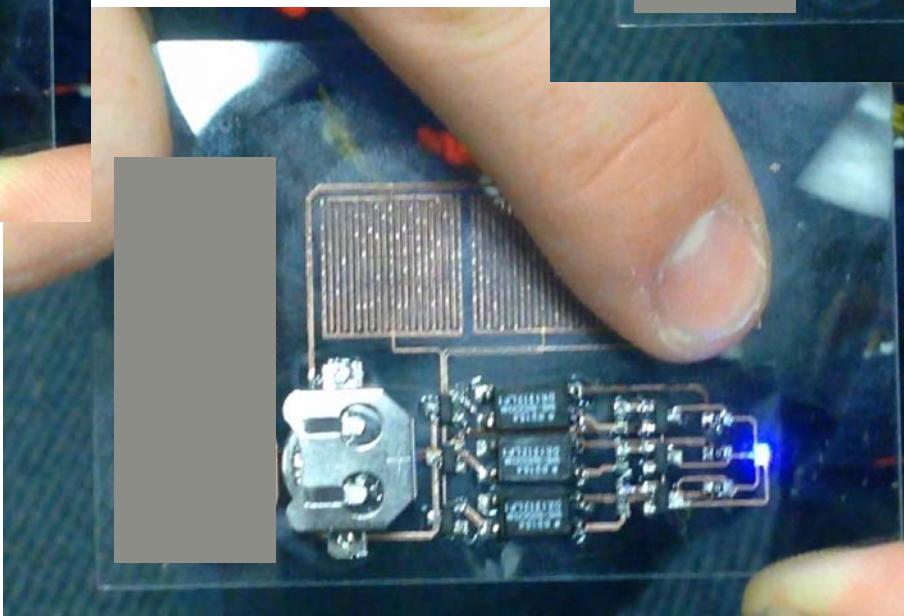
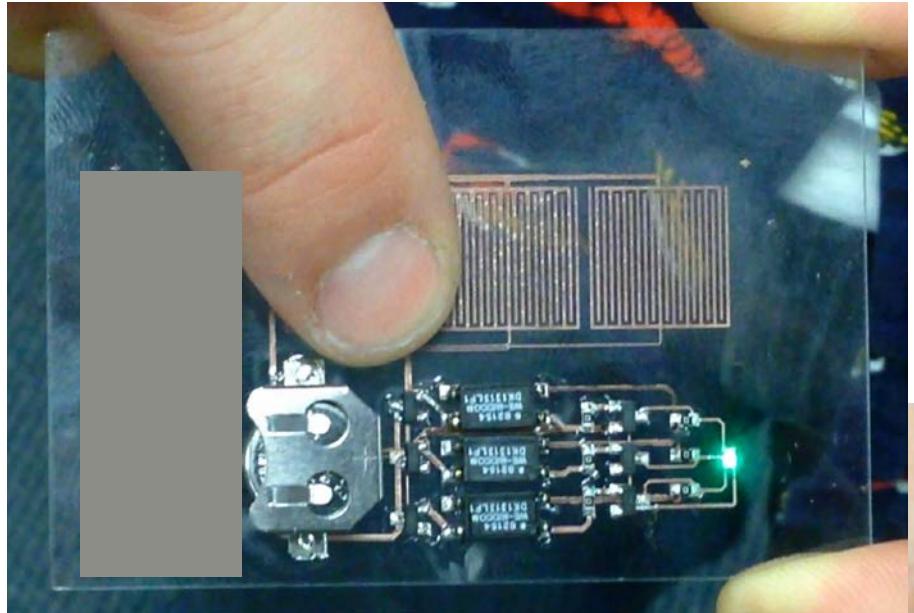
“Seeded” glass slide



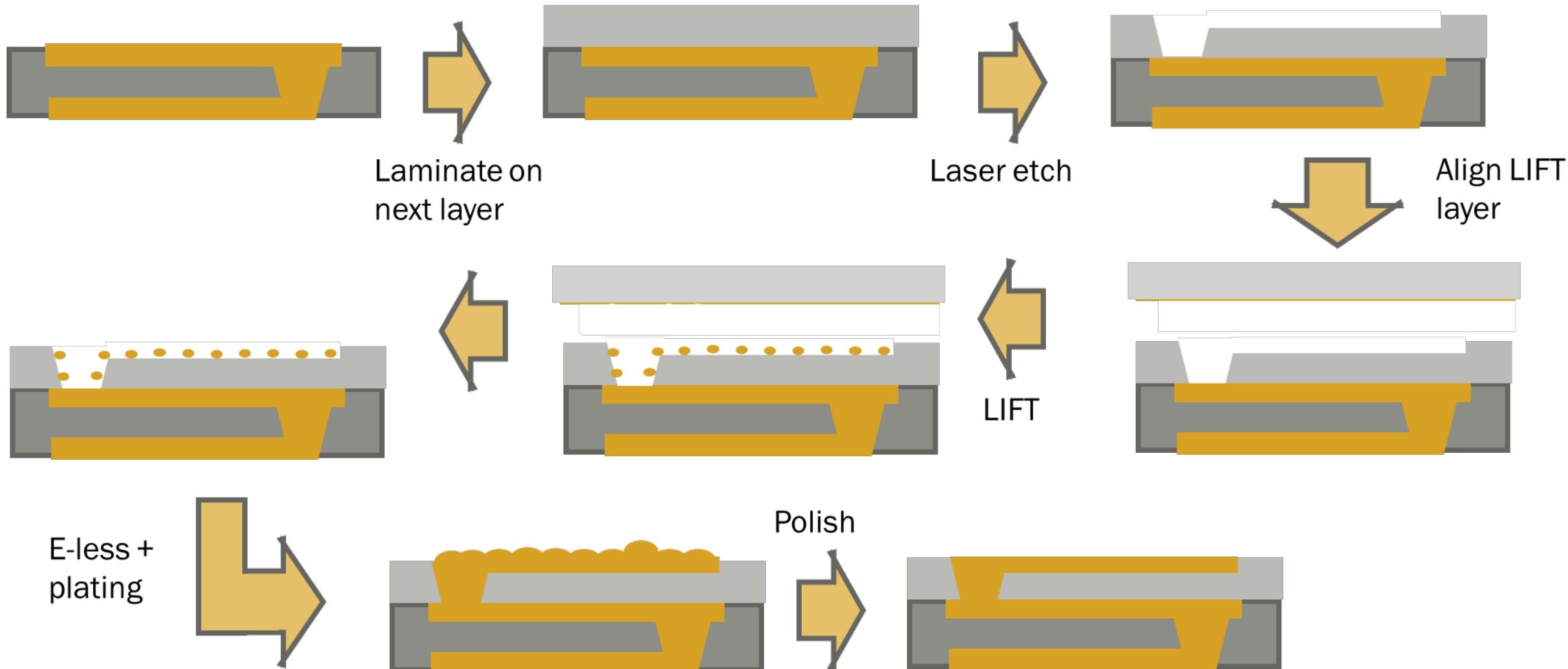
# TECHNOLOGY'S TURNING POINT

# TURN ELECTRONICS MANUFACTURING INSPIRATION INTO INNOVATION

# Functional Demonstrator



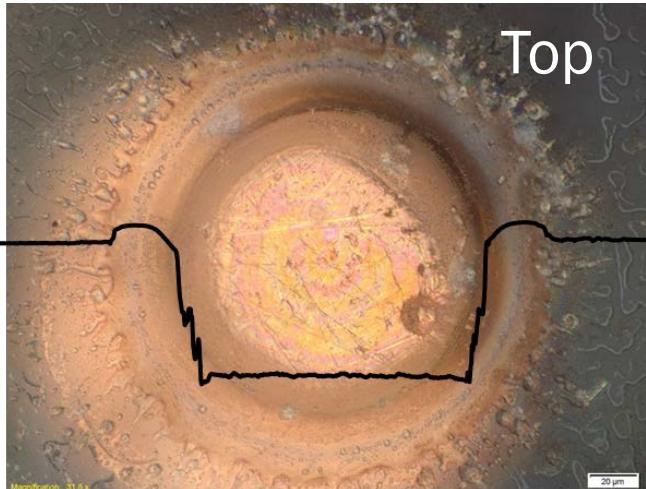
## Advanced Multilayer Process



## Advanced Multilayer Process

Blind Vias in  
Glass with 9.3  
 $\mu\text{m}$   $\text{CO}_2$  laser

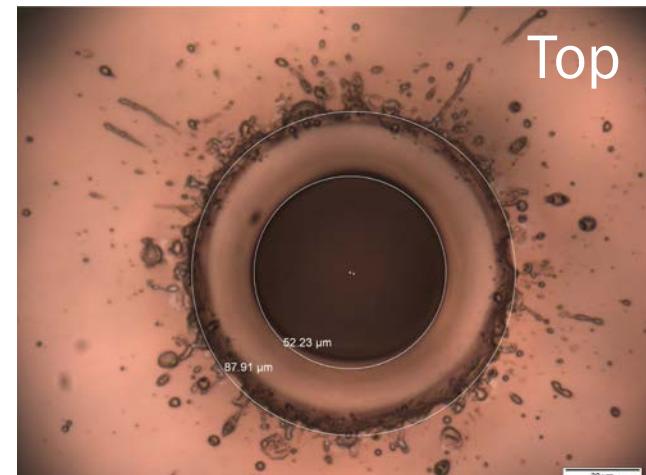
135  $\mu\text{m}$



Top

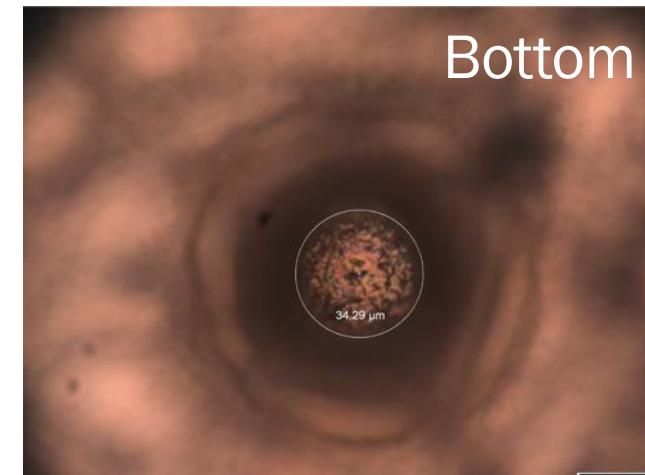
Bottom

50  $\mu\text{m}$

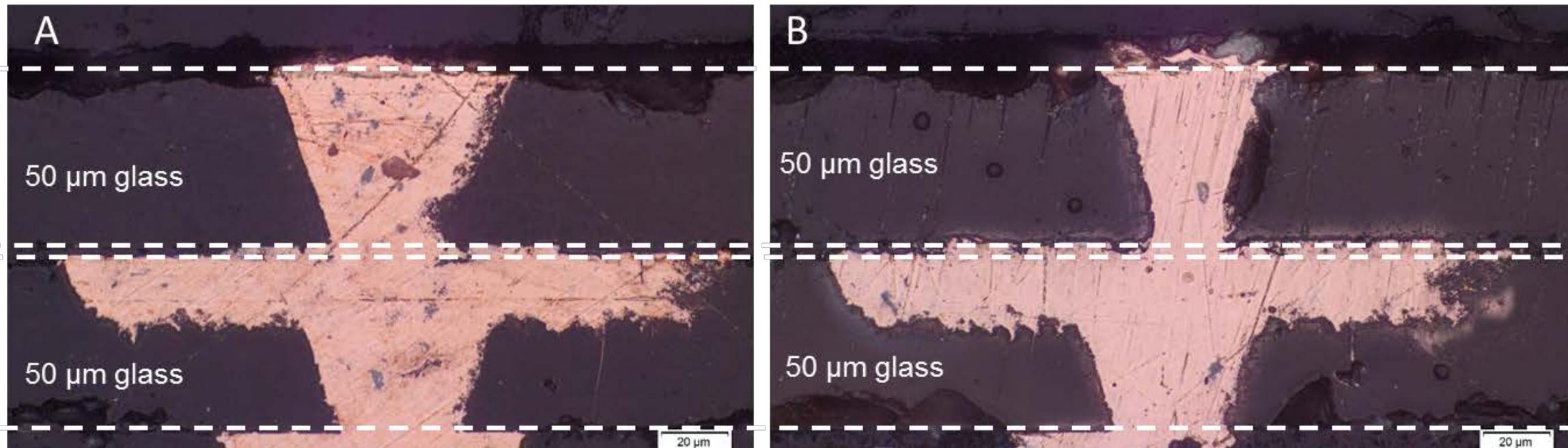


Top

Bottom

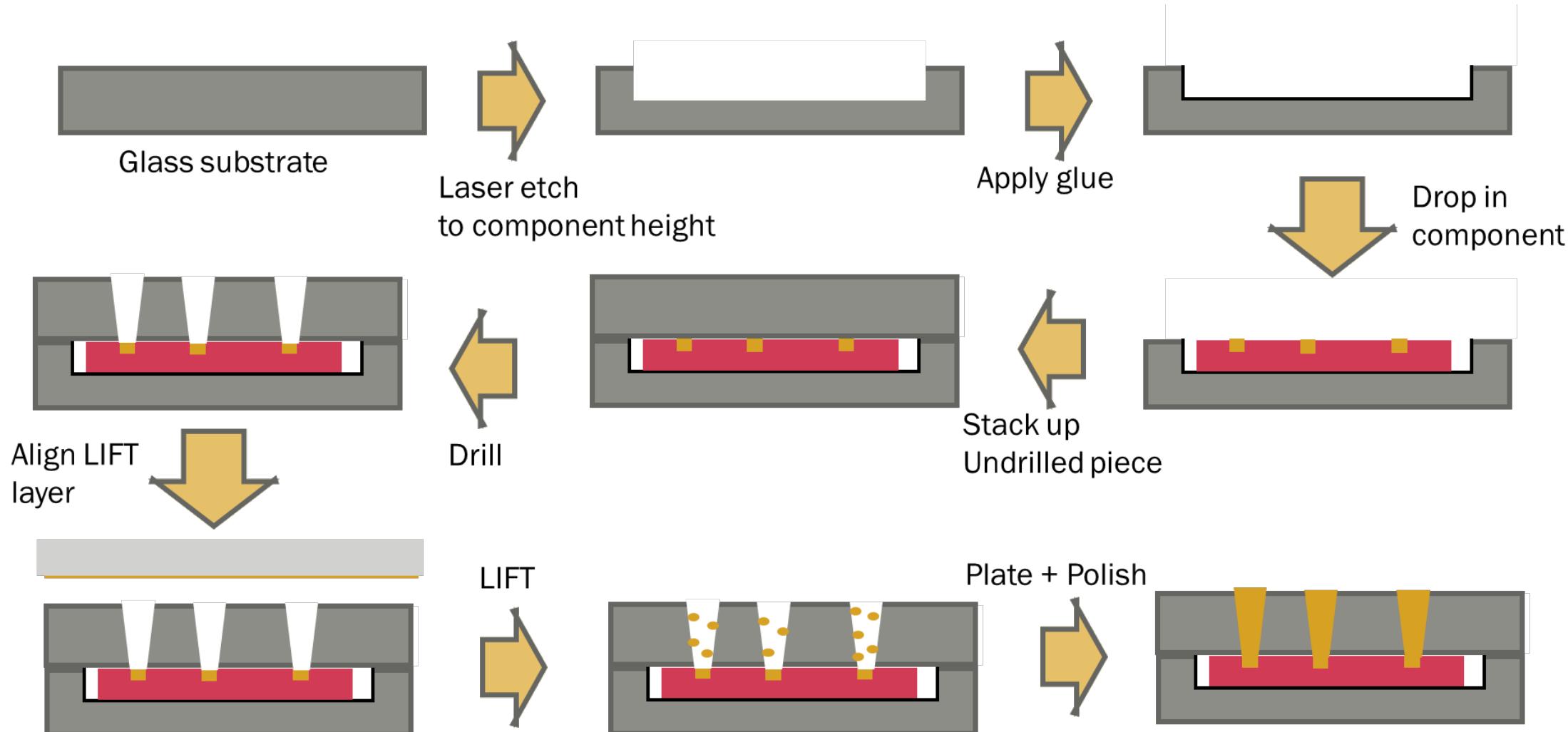


## Advanced Multilayer Process



Bottom layer etched with 515 nm, 800 fs system. Blind via drilled with 515 nm, 800 fs system in (A) and with the company's CO<sub>2</sub>-based microvia platform in (B).

## Process Application: Embedded Components



## Comparison to Traditional PCB Fab

- No photolithography steps—features are etched directly into the dielectric
- Many pre-plating steps are eliminated
- No copper etching steps
- Electroless and electroplating baths can be used without modification
- Still working on understanding process rates compared to traditional fabrication



Avoiding many process materials that need to be recycled or are hazardous—“Green Chemistry”

## Future Work

- Additional base material compatibility
- Seeding with other conductive materials
- Reliability testing
- 2D/3D applications
- Continued development expected with multiple cross-functional partners

## References

- [1] Corning Willow Glass