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Pb-Free Reflow, PCB Degradation, and the Influence of Moisture Absorption

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Abstract

Introduction

The cracking and delamination of printed circuit boards (PCB) during exposure to elevated thermal exposure, such as reflow and rework, have always been a concern for the electronics industry. However, with the increasing spread of Pb-free assembly into industries with lower volume and higher complexity, the occurrence of these events is increasing in frequency. Several telecom and enterprise original equipment manufacturers (OEMs) have reported that the robustness of their PCBs is their number one concern during the transition from SnPb to Pb-free product. Cracking and delamination within PCBs can be cohesive or adhesive in nature and can occur within the weave, along the weave, or at the copper/epoxy interface (see Figure 1). The particular role of moisture absorption and other PCB material properties, such as out of plane expansion on this phenomenon is still being debated.

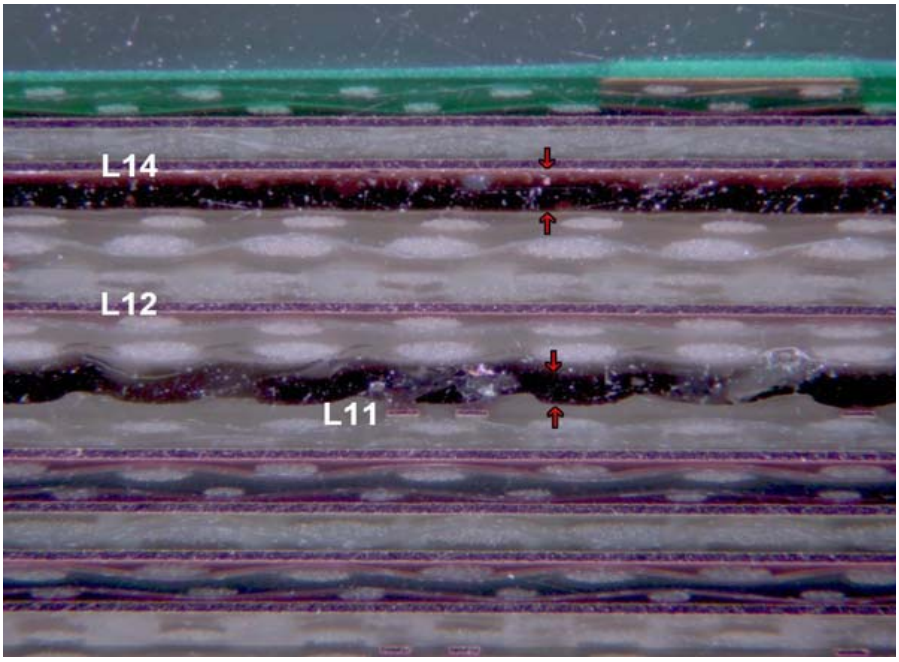


Figure 1: Optical micrograph of cross-sectioned 16 layer PCB that experienced delamination during reflow.

An example of the complexity and uncertainty of the drivers for this phenomenon can be found in a case study involving a contract manufacturer. As seen by the acoustic image in Figure 2, the CM was experiencing pervasive delamination after exposing a circuit card assembly (CCA) to Pb-free reflow. The CCA was 14 x 18 inches and 90 mil thick and was fabricated with laminate material with a Tg of approximately 180C. Cracking or delamination during reflow tends to be an overstress mechanism and can therefore be described as a stress vs. strength phenomenon. That is, either the environmental stress was higher than expected or the material strength was lower than expected.

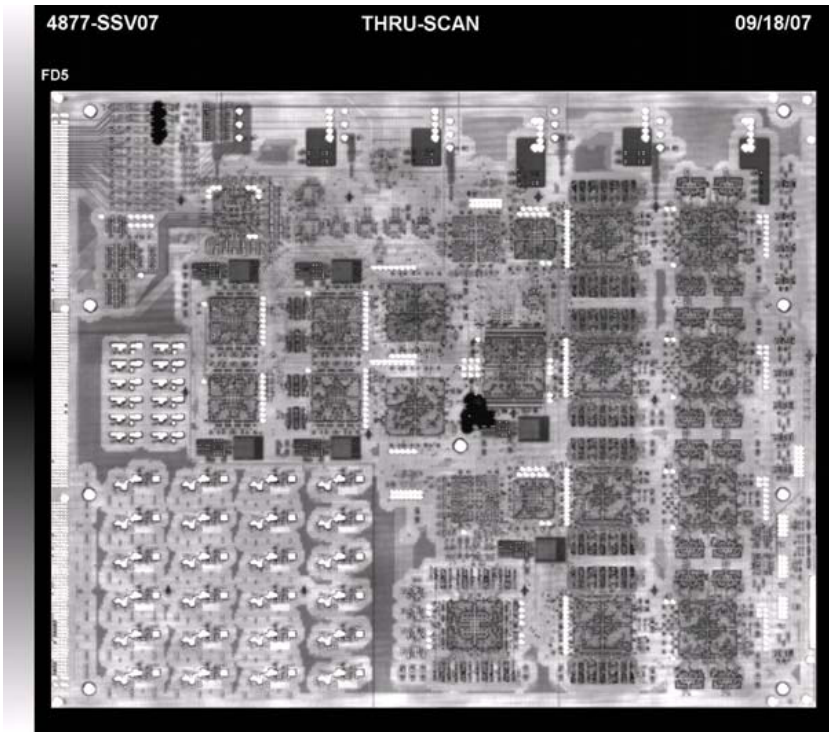
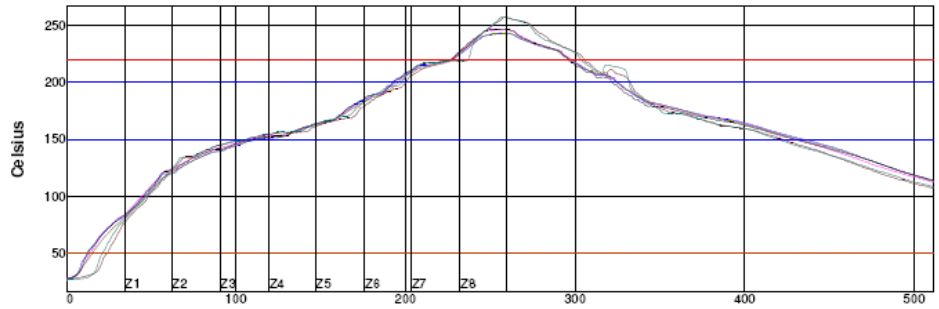


Figure 2: Through scan acoustic image of printed circuit board. The delaminations are highlighted in red

The environmental stress during reflow would be driven by either the temperature profile (ramp rate, maximum temperature, time above liquidus) or the presence of volatiles within the printed board stack up. The reflow profile is displayed in Figure 3. The primary parameters of the reflow profile were within nominal ranges, including:

- Ramp rates between 2 to 3ºC per second
- Time above liquidus between 45 to 90 seconds
- Peak temperature below 260ºC.



PWI= 249%	Max Rising Slope		Soak Time 150-200C		Reflow Time /220C		Peak Temp		Tot Time / 50C	
U49	2.2	-28%	86.5	-12%	70.4	131%	246.5	93%	517.5	88%
U68	2.1	-29%	80.4	-32%	70.1	129%	243.2	45%	531.9	93%
U 104	1.9	-35%	84.2	-19%	69.9	128%	243.4	49%	530.5	93%
UU 70	2.2	-27%	82.6	-25%	69.3	125%	246.6	94%	537.9	96%
U 41	2.5	-17%	93.4	11%	78.5	177%	257.1	244%	515.0	87%
Raw Card C 360	2.5	-16%	91.7	6%	65.8	104%	257.4	249%	528.6	92%
Delta	0.6		12.9		12.7		14.2		22.9	

Figure 3

To test for volatiles, a syringe was used to extract chemistry from the delamination sites. The specific extraction process involved a solvent rinse and the resulting solution was analyzed using gas chromatography / mass spectroscopy (GCMS). No contaminants, such as H_2O or monomer chemistry, were detected. Further surface analysis of the delaminated interface, after peeling of the PCB, through FTIR and SEM/EDAX also did not reveal any contamination chemistries or indications of insufficient polymerization. In addition, the dual location of the delamination sites, one at the edge and one at the center of the board, would seem to rule out moisture absorption immediately before reflow as a cause of increased stress as moisture tends to diffuse along the routed or scored edges of the PCB.

Decreased material strength of the printed board can be driven by a number of factors, including

- Non-optimized epoxy formulation
- Non-optimized glass surface treatments
- Absorption of moisture before epoxy cure
- Insufficient epoxy cure (B-stage)
- Surface contamination (copper or epoxy)
- Non-optimized oxide treatment
- Non-optimized lamination

Identification of the actual cause of decreased strength can be guided by observing the delaminated surface. While one of the delaminated sites showed some evidence of insufficient wetting between the epoxy and glass fiber, the other site provide no indication of a cause for decreased material strength.

Despite limited evidence of the influence of moisture on the observed delamination, including the controlled storage conditions and the relatively short time between PCB fabrication and CCA manufacturing, the CM experienced a definitive reduction in the occurrence of delamination after all PCBs were subjected to baking for 48 hours at 125ºC. A complete elimination of delamination was observed after decreasing the peak reflow temperature to 245ºC, in addition to the previously mentioned baking step.

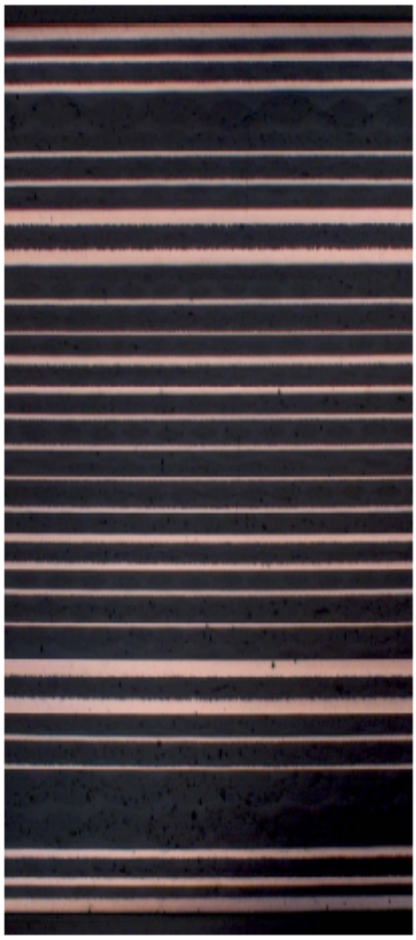
Given the discrepancies or conflicting evidence in this case study and others, a more controlled research study to assess the influence of moisture and PCB delamination was initiated.

Coupon Design

Two coupon designs, standard and advanced, were utilized to investigate the effect of Pb-free solder reflow on the degradation of printed circuit boards (PCBs). Degradation was induced using humidity preconditioning and reflow simulation, and characterized through changes in capacitance and observations of cracking or delamination.

The PCBs used were composed of 26 layers of copper foil, with varying thicknesses of 0.5 oz, 1.0 oz and 2.0 oz. The dielectric between each layer was composed of an IT-180 material with one or two plies of different glass fabrics (106, 1080, 7628, and 2116) varying in thicknesses of 3 mil, 4 mil, 5 mil and 14 mil. The total thickness of the coupon was 150 mil and a detailed coupon stack-up is shown in Figure 4.

Each coupon contained three sections and a total of six test structures were incorporated into the design, as pictured in Figure 5. The three sections of the PCBs all consisted of the basic shield-over-shield copper plane design; however, they differed in their content of plated through holes (PTHs) and non-functional pads. Section 1 contained only copper planes, which resulted in the largest shield-over-shield capacitance measurements and facilitated observation of clear trends for this data. Section 2 contained copper planes, PTHs and nonfunctional pads on every layer, allowing capacitance measurements to be made for both shield-over-shield and PTH-shield trends on the same coupon. Lastly, section 3 contained copper plains, PTHs and nonfunctional pads on every other layer. This design can be utilized for conductive anodic filament (CAF) testing; however, this data has not yet been obtained and will be the focus of future studies.



1	0.65	foil 1/2 oz	
	3	prepreg	1 x 1080
2	0.65	1 oz	
	4	core	
3	0.65	1 oz	
	14	prepreg	2 x 7628
4	0.65	1/2 oz	
	4	core	
5	0.65	1/2 oz	
	5	prepreg	2 x 1080
6	2.4	2 oz	
	4	core	2 x 106
7	2.4	2oz	
	5	prepreg	1080 + 211
8	0.65	1/2 oz	
	5	core	1 x 2116 H
9	0.65	1/2 oz	
	3	prepreg	1 x 1080
10	1.4	1 oz	
	4	core	2 x 106
11	1.4	1 oz	
	3	prepreg	1 x 1080
12	0.65	1/2 oz	
	5	core	1 x 2116 H
13	0.65	1/2 oz	
	5	prepreg	1080 + 211
14	0.65	1/2 oz	
	5	core	1 x 2116 H
15	0.65	1/2 oz	
	3	prepreg	1 x 1080
16	1.4	1 oz	
	4	core	2 x 106
17	1.4	1 oz	
	3	prepreg	1 x 1080
18	0.65	1/2 oz	
	5	core	1 x 2116 H
19	0.65	1/2 oz	
	5	prepreg	1080 + 211
20	2.4	2 oz	
	4	core	2 x 106
21	2.4	2oz	
	5	prepreg	2 x 1080
22	0.65	1/2 oz	
	4	core	
23	0.65	1/2 oz	
	14	prepreg	2 x 7628
24	0.54	1 oz	
	4	core	
25	0.65	1 oz	
	3	prepreg	1 x 1080
26	0.65	foil 1/2 oz	

Figure 4: Representation of coupon stack-up and physical parameters of the different layers.

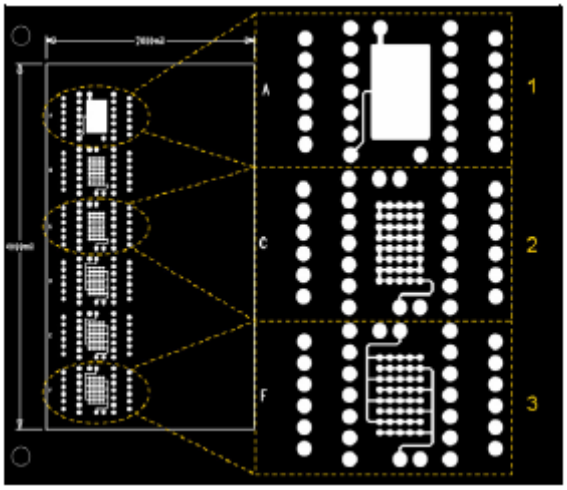


Figure 5: Schematic representation of the PCB coupons. Test structures are labeled A-F and a representative coupon from each of the three sections is displayed to the right of the image.

In addition to the three sections of the PCBs, six test structures were present on each coupon and their layout is shown in Figure 6. Test structure A, located on section 1 of the PCB, contained only the basic shield-over-shield design for both the standard and advanced coupons. Test structures B and C, located on section 2 of each PCB; contained PTHs and internal planes that varied slightly in their dimensions depending on the coupon type. On the standard coupon, the pads had a 27-mil diameter, a 78-mil pitch, a 15-mil drill diameter and a clearance of drill+10mil. The advanced coupon design differed with respect to test structures B and C in only the drill diameter and clearance parameters, which had a value of 12 mil and drill+7mil respectively. Test structures D, E and F, present on section 3 of the coupons; consisted of PTHs with no internal

planes. The standard coupon differed from advanced in the third section of the PCB in that it had a 40-mil pitch while the advanced board had a 32-mil pitch.

The current design of these PCBs allowed for the measurement of capacitance across the internal plans and between PTHs and internal planes as diagramed in Figure 7. The different dimensions of the test structures present on the standard and advanced coupons allowed investigation into how the size of the PTHs can affect the degradation of the board manifested through changes in capacitance and physical board mutations. Limitations arose during this experiment because test structures A, B and C all have their layers shorted together through the nets A1-A2, B1-B2 and C1-C2, respectively. This design allowed for the measurement of capacitance across all layers as a whole but not across individual layers. Therefore, although we had the ability to detect the presence of shorts, cracking and delamination, we were not necessarily able to determine the exact location of the failure.

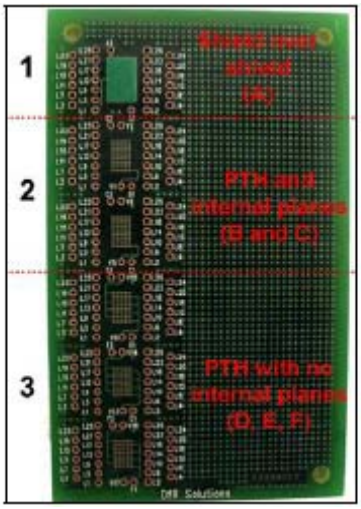


Figure 6: Image of tested PCB coupons with the three sections and corresponding test structure location labeled.

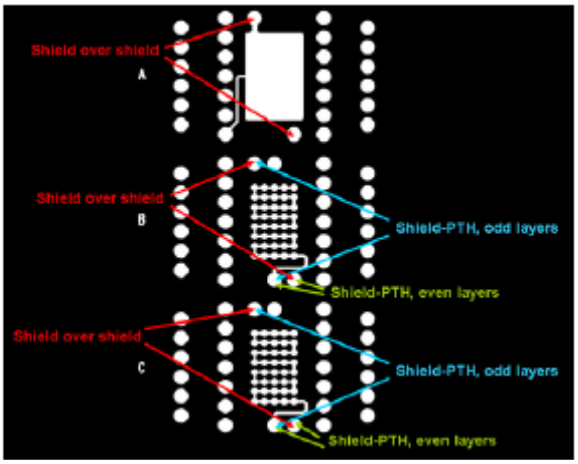


Figure 7: Schematic depicting how the capacitance measurements were obtained

Experimental Procedure:

The reflow oven used was a bench top model pictured in Figure 8. The oven was calibrated using an external thermocouple to verify the accuracy of the oven's temperature as reported by the computer's software. To control for variability of the internal temperature of the reflow oven, the internal temperature sensor was tightly secured to the tested PCBs to make sure that the PCB surface temperature was what drove the ramp rate of the reflow cycle. This technique ensured that the PCBs reached the desired temperature throughout the cycle and eliminates the variability that would occur if the thermocouple was not consistently placed for each cycle.

The oven was utilized during the study to simulate reflow cycling on the PCBs. To do this, two different reflow profiles were created which differed only in their peak temperature. The first reflow profile consisted of a peak temperature of 260°C (Figure 9) while the second profile consisted of a peak temperature of 280°C (Figure 10).

Figure 8: Benchtop reflow oven

Reflow Profile 1:

	Temperature (°C)	Time (s)
Parameter 1	160	90
Parameter 2	260	60
Parameter 3	260	15

Figure 9: 260°C reflow profile.

Reflow Profile 2:

	Temperature (°C)	Time (s)
Parameter 1	160	90
Parameter 2	280	60
Parameter 3	280	15

Figure 10: 280°C reflow profile.

A 4263B LCR model capacitance meter was used to obtain capacitance measurements throughout the study. This model has a 0.1% basic accuracy and all measurements were taken at the 100 kHz setting. The capacitance meter was calibrated to determine its relative accuracy for measuring small capacitance changes. To do this a 22pF NPO ceramic capacitor was used as a standard. It was determined that the capacitance meter was accurate to within 2% (measured 22pF +/- 2%) for Cs measurements and accurate to within 5% (measured 22pF+/- 5%) for Cp measurements. All capacitance measurements taken during this study were of Cs and not Cp capacitance.

Phase 1: The effect of peak reflow temperature on the rate of degradation

Phase 1 consisted of two tests that investigated the effect of simulated Pb-free reflow cycling on capacitance measurements of both standard and advanced boards. The first test involved cycling 5 advanced coupons through 30 reflow cycles with a peak temperature of 260°C. This test was modified and repeated, in which 5 more advanced coupons were subjected to 12 reflow cycles with a peak of 280°C. The shield-over-shield capacitance on test structure A was measured out of the package and directly after each reflow cycle. It is important to note that test structure A is identical for both the standard and advanced coupons and that all capacitance measurements for these and subsequent experiments were taken at room temperature (26°C +/- 2°C).

The second test of phase 1 investigated the effect of reflow cycling on the different test structures present on the PCBs. This process involved subjecting 5 standard coupons to 15 reflow cycles with a peak temperature of 260°C. As with the first test, shield-over-shield capacitance was measured directly out of the package and after each reflow cycle for test structures A, B and C. In addition to this, the shield-PTH capacitance was also measured out of package and after each reflow cycle for test structures B and C. This allowed observation into the effect of temperature cycling on the fidelity of different test structures present on both the standard and advanced coupons.

Phase 2: The effect of moisture absorption on the rate of degradation
Phase 2 tested the moisture sensitivity of the different test coupons. Three boards were used per experimental condition, (MSL1, MSL2 and MSL2) which differed based on the time of pre-bake, relative humidity, temperature and length of exposure as outlined in Figure 11. These profiles were based on the standards laid out in J-STD-020C. All boards were initially dried at 125°C and allowed 15 minutes after removal from pre-bake before humidity testing began.

Profile Name	Pre-bake	Experimental Conditions
MSL1	88hr at 125°C	85°C/85%RH, 168 hours
MSL2	88hr at 125°C	85°C/60%RH, 168 hours
MSL2a	72hr at 125°C	60°C/60%RH, 120 hours

Figure 11: The moisture sensitivity profiles used during this experiment are displayed. .

Three boards were cycled through each of the different moisture sensitivity profiles and afterwards weight gain and shield over-shield capacitance was measured on test structure A. Additionally, the boards that were subjected to the MSL2a profile had shield-over-shield capacitance as well as PTH-shield capacitance obtained for test structures B and C.

Results (Phase 1-Test 1): The effect of peak reflow temperature on rate of degradation of test structure A
The data demonstrates that a steady decrease in shield-over-shield capacitance occurred in the boards subjected to the 260°C profile as the number of reflow cycles increased (Figure 12). Although there was no specific number of reflows at which the capacitance measurements dropped-off, the trend in the data suggests that this decrease would continue to occur as more reflow cycles were conducted.

When the peak temperature of the reflow cycle was increased to a value of 280°C, the same general trend was observed although the degradation occurred about fifty times faster (Figure 13). This was shown by the fact that only 12-13 reflow cycles of the second profile were needed to cause a comparable decrease in capacitance to what was previously observed in the first profile with 30 reflow cycles. The normalized capacitance of the 280°C profile showed a marked decrease after 4 reflows equal to about 0.5% on average, and then capacitance decreased gradually with each additional reflow cycle. The data from both tests of phase 1 suggests that an inverse relationship exists between these two variables and as the peak reflow temperature is increased within the range tested, the amount of reflows necessary to cause a comparable decrease in capacitance is reduced.

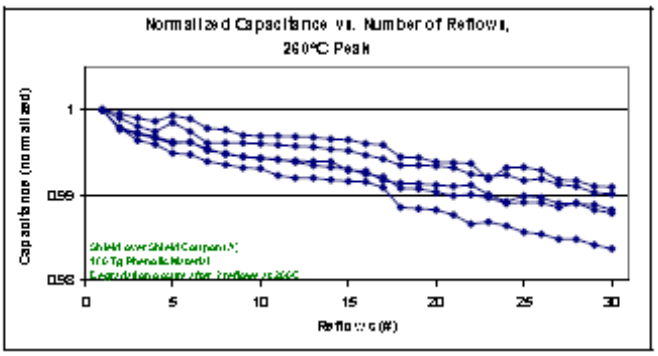


Figure 12: The relationship between the normalized capacitance and increasing reflow cycles, repeated 30 times with a peak temperature of 260°C preformed on 5 advanced coupons.

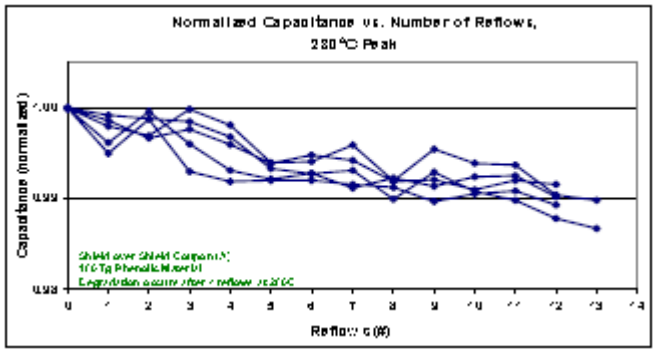


Figure 13: The relationship between the changes in the normalized capacitance as a result of 12 reflow cycles with a peak temperature of 280°C performed on 5 advanced coupons.

Results (Phase 1-Test 2): the effect of peak reflow temperatures on test structures A, B and C

The effect of repeated reflows on shield-over-shield capacitance between test structures A, B and C, was obtained during this phase of the investigation. Data was also collected on the measured shield-PTH capacitance of test structures B and C. This allowed comparison of shield-over-shield capacitance changes and shield-PTH capacitance changes across multiple test structures on the same board. Also by measuring these parameters on test structures B and C, both shield-over shield and shield-PTH capacitance measurements could be analyzed and compared from the same test structure.

The results obtained showed that different test structures degrade at different rates as apparent in Figure 14. From these results, it is clear that test structure B degraded the most followed by test structure A and then test structure C. Test structure B had an average rate of degradation of almost five times that of test structure A, and test structure C had rate of degradation about three times that of test structure A. This suggests that some inherent difference with the design of these test structures resulted in differential rates of degradation.

The overall changes in shield-PTH capacitance (Figure 15) were much greater than the shield-over-shield capacitance changes across all test structures (Figure 14). After just one reflow cycle, the degradation observed in the PTH-shield nets was comparable to the degradation observed in shield-over-shield capacitance nets after 15 reflow cycles. The PTH-shield capacitance also decreased most dramatically after 4 reflows and continued to decrease as the boards were subjected to an increasing number of reflow cycles. The data for the shield-PTH capacitance changes also appeared much more variable compared to the shield-over-shield data, with one board showing a much larger decrease in capacitance on all PTH-shield nets compared to the others.

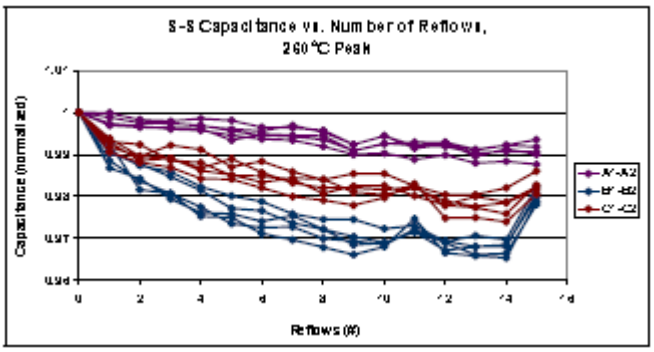


Figure 14: The results of 5 standard boards through 15 reflow cycles with a peak temperature of 260°C. The shield over shield capacitance was measured before testing and after each cycle for test structures A, B and C.

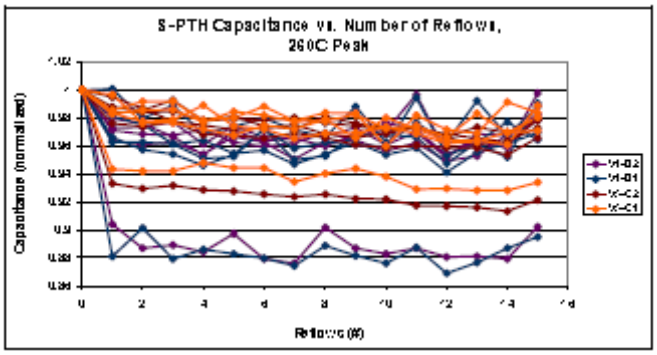


Figure 15: The relationship between the measured Shield-PTH normalized capacitance changes that occurred after 15 reflow cycles at a peak temperature of 260°C.

Results (Phase 2): Moisture Absorption results

Moisture absorption was measured as the percent weight increase of the PCBs. This data was then used to measure the effect of increased moisture absorption on the capacitance of the test coupons after repeated reflows. Also, different moisture sensitivity profiles were utilized in order to observe which parameters would result in the greatest amount of moisture absorption. As shown in Figure 16, as either the relative humidity or temperature of the moisture sensitivity profile is increased, the percent weight gain by the PCBs is also increased. This is apparent because the PCBs subjected to the MSL1 profile had the largest percent weight gain of the three profiles. The MSL2 profile had a larger percent weight gain compared to MSL2a profile and since these profiles only differed by the temperature of the moisture sensitivity profile, it demonstrates that with increased temperature alone, more moisture absorption can be achieved. When subjected to any of the three conditions, the PCBs all behave the same way. There was a linear relationship between time of exposure and percent weight gain, but this began to level off as the PCBs became saturated, evident in Figure 16. Based on Figure 16, it is also clear that saturation of the PCBs began around 8 hours. When the data is represented as the percent weight gain versus the time in hours squared, a linear relationship appears as shown in Figure 17. This demonstrates that the percent weight gain is proportional to the square of the time in hours.

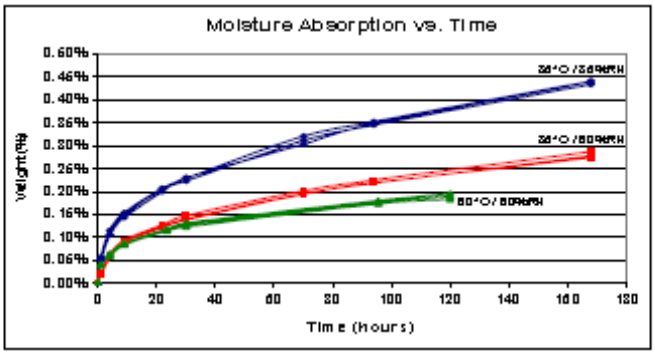


Figure 16: Representation of the relative moisture absorption of the boards subjected to different moisture sensitivity profiles. Increases in relative humidity and temperature both resulted in increased water absorption by the PCBs

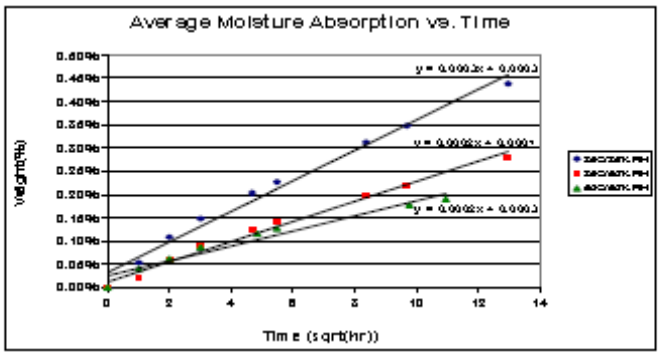


Figure 17: The plotted percent weight gain versus the time in hours squared, demonstrates that a linear relationship exists between these variables.

Results (Phase 2): Moisture Sensitivity and Capacitance Results:

The three moisture sensitivity profiles resulted in similar changes in capacitance for all PCBs; however variation existed when comparing changes across individual test structures. The capacitance measurements of coupon sections containing only shield-over shield layers showed the smallest change with respect to moisture absorption. This relationship was observed by looking at the data from test structure A because up to approximately 0.15% weight gain, no significant changes in capacitance occurred. After this point however, the data appeared to linearize, and as percent moisture absorption increased, capacitance measurements also increased (Figure 18). The shield-over-shield capacitance in test structures B and C showed a larger increase in capacitance with respect to increased percent moisture absorption. This is apparent in Figure 19, where the 2 traces for capacitance measurements of net B1-B2 and C1-C2 show a much greater change at 0.20% moisture absorption compared to the test structure A. The PTH-shield results were much more variable and although it is apparent that a larger change in capacitance resulted relative to the percent of moisture absorption, no clear trend in the data for these test structures exists (Figure 19).

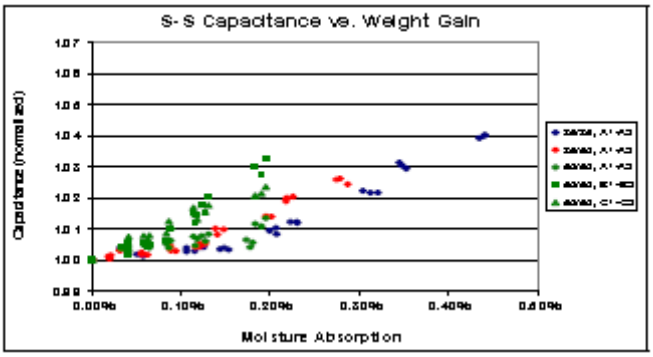


Figure 18: The normalized shield-over-shield capacitance is measured with the respect to the about of moisture absorption. As moisture absorption increases so does the increase in capacitance.

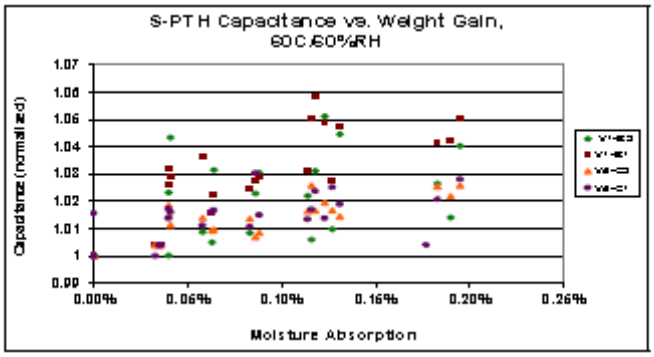


Figure 19: Normalized shield-PTH capacitance vs. weight gain for the MSL2 a moisture sensitivity profile. Capacitance measurements were obtained for both test structures B and C.

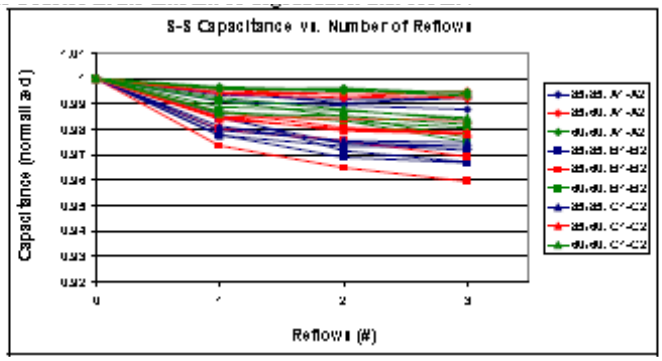


Figure 21: **The shield-PTH capacitance measurements for test structures B and C after exposure to moisture sensitivity profile MSL2a and repeated reflow cycles.**

The normalized capacitance changes from phase 1 were noticeably less compared to the capacitance changes in the boards exposed to the moisture profiles in phase 2. This is true even when the boards were subjected to fewer reflow cycles. Within this subset of data, the same trends observed earlier regarding the different test structures were also observed. Test structure A showed the smallest change in capacitance measurements while test structure B had the greatest. This suggests that the presence of PTHs increases the rate of degradation and that shielded PTHs consistently perform worse than unshielded PTHs. This data also suggests that a difference in the capacitance changes exists because of the different moisture sensitivity profiles the PCBs were exposed to. The 60°C/60%RH profile had the smallest measured degradation and it was also the profile with the lowest temperature and RH value. The higher temperature profiles resulted in more moisture gain and a larger increase in capacitance before being subjected to reflow testing. However when this data was normalized, the PCBs also demonstrated a greater decrease in capacitance after repeated reflows (Figure 20). With all conditions, the PTH-shield capacitance measurements degraded quicker compared to shield-over-shield capacitance measurements (Figure 21). The same trend in the moisture sensitivity profiles was seen when testing shield-PTH capacitance, with MSL2a showing the least amount of degradation compared to the other two profiles. The data suggests that when PTHs are present the temperature of the profile becomes more of a factor in the amount of degradation that occurs.

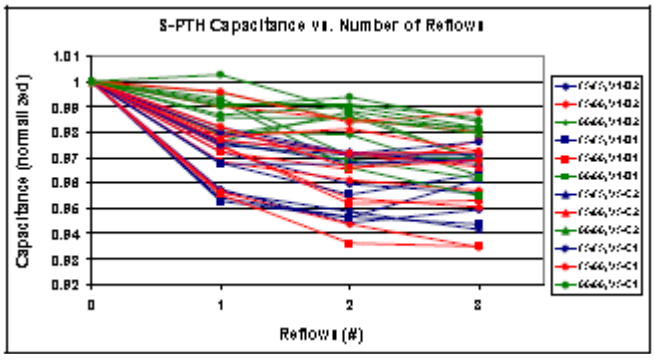


Figure 20: Shield-over-shield capacitance vs. number of reflows after being subjected to the respective moisture sensitivity profiles including MSL1, MSL2 and MSL2a. Capacitance was measured for test structures A, B and C.

Results: Delamination

Besides the discussed changes in capacitance that occurred as a result of moisture exposure and repeated reflows, delamination was visible evidence for PCB degradation (Figure 22). Delamination was only observed in featureless areas (see Figure 23) and evidence for delamination was only observed in PCBs subjected to moisture sensitivity profile MSL1. This profile had both the highest temperature and highest relative humidity, resulting in the largest percent weight gain in the PCBs. No visible delamination occurred in the MSL2 or MSL2a profile nor in any of the "dry samples" from phase one, which suggests that increases in moisture content facilitates the process of delamination in these PCBs.

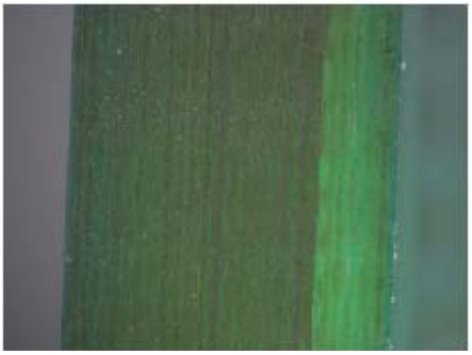


Figure 22: Delamination observed in cross-section of a test coupon subjected to MSL1 exposure (85°C/85RH) and subjected to 3 reflows at a peak temperature of 260°C

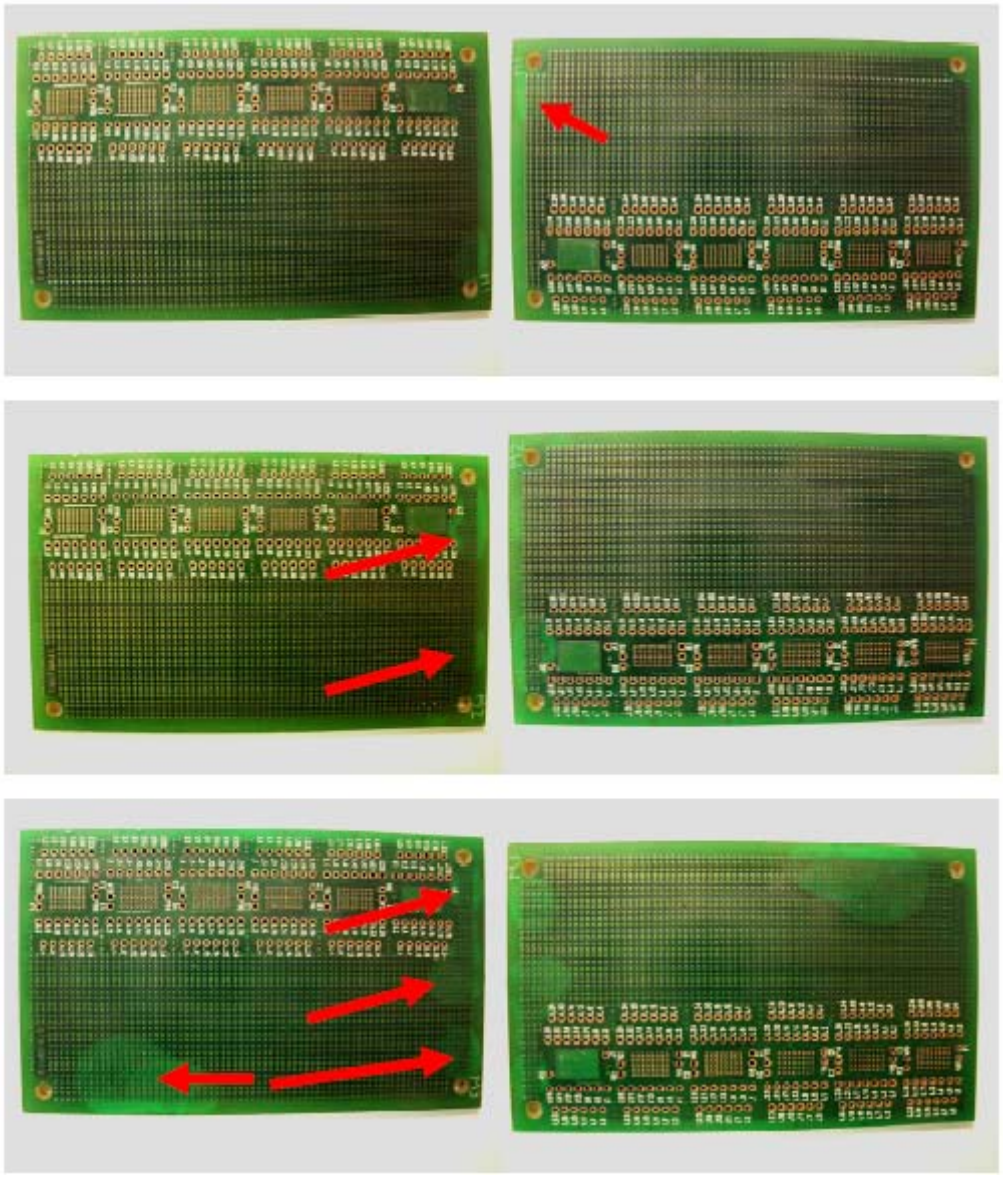


Figure 23: Photo documentation of delamination in PCB coupons subjected to MSL1 exposure (85°C/85%RH) and 3X reflow at peak temperature of 260°C. Delamination is highlighted by red arrows.

Discussion

Based the data presented it appears that a variable relationship exists between test structure type and the rate of degradation. One cause of the degradation observed in the PCBs may be due to micro-cracking and if this is the case, it appears that the different PCB structures influence the observed rate of board degradation. Based on the fact that test structure A has no PTHs and degraded the least compared to all other test structures across all trials, it appears that the presence of PTH exacerbates the development of micro-cracking. The fact that test structure B degraded faster than test structure C also suggests that the presence of non-functional pads also facilitates the micro-cracking process.

It was noted that the data for shield-PTH capacitance changes was extremely variable and that one board showed a significant decrease in capacitance measurements on all Shield-PTH nets. This was observed on both test structure B and C even though these structures were purportedly independent. There are several possible explanations for these abnormal results including that the capacitance measurements were taken at an elevated temperature, a shield-PTH short occurred, or the presence of extensive micro-cracking resulted in this accelerated degradation. Even with these proposed explanations this result cannot be fully explained. If the capacitance measurements happened to be taken at an elevated temperature or if it were due to extensive micro-cracking, this would have also affected the shield-over-shield measurement which wasn't the case. It is also unlikely for a short to occur in the PCB that would affect both test structure B and C simultaneously. Therefore at this point the results for the shield-PTH measurements are not clear and more data should be obtained before a conclusion can be made.

The only clear conclusion that can be made at this time is that the presence of PTHs resulted in a much higher rate of degradation.

From the data it was revealed that the 85°C/60%RH profile resulted in the greatest amount of water absorption although the precise reason why is unknown. It was also observed that test structures with PTHs showed a greater increase in capacitance for a given amount of water absorption. This difference could be due to damage that occurs during the drilling process to create the PTHs, which might result in tiny cracks or delamination that facilitated the absorptions of water. If this were the case it suggests that the assembly process for creating PTHs, not their inherent presence, accounts for the increase degradation rate that was observed.

The relationship between shield-PTH capacitance and moisture absorption produced no clear trend. However there was a clear difference between test structure B and C when comparing this data across the same level of moisture exposure. It was shown that test structure B generally showed a greater increase in capacitance and then a subsequent greater decrease in capacitance after repeated reflows. Moisture exposure also caused the boards to degrade much faster during reflow cycling compared to boards which were not subjected to moisture exposure. This is supported by comparing the data from phase 1, which showed approximant 1% degradation in capacitance of test structure A after 15 reflows to samples from phase 2, which showed a comparable decrease in capacitance after about 3 reflows. This trend was also observed in all Shield-over shield and shield-PTH nets. The results of these experiments lead to the conclusion that the changes in capacitance that occurred after each reflow was due to material degradation and not an increase in resistance due to oxidation. However to further prove this; contact resistance should be quantified through ESR measurements in the next round of testing. Also the differences in degradation rates between test structures B and C, due to the presence of nonfunctional pads, is very interesting. This difference should be further characterized by focusing on the clearance and pad dimensions of future board designs. Overall this study was successful in characterizing the effect of heat and moisture exposure on the degradation of different PCBs and although it helped answer some of the questions regarding this process it also exposed new ones which will continue to guide future studies.

Conclusion

Measurable change of capacitance was recorded after each reflow. Discrimination between different test structures and MSL exposures strongly suggests approach captures material degradation, as opposed to an increase in resistance at contact pads due to oxidation. However, contact resistance should be quantified in a next round of testing through ESR measurements. Strong difference in shield-over-shield capacitance between test structures B and C, due to the presence of non-functional pads, is very interesting and should be further characterized.