

White Paper

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Abstract

As silicon technology advances to enable higher density ASICs, the core logic voltage decreases. The lower voltage, in combination with higher current requirements, requires tighter tolerances on the power supplies. The control of the power supplies from the PCB to the die is the subject of this study. A frequency sweep simulation using typical bypass values shows that a discrete package capacitor is not a significant factor in reducing the chip core power supply fluctuation. A small voltage boost at the PCB supply can provide a more economical solution to managing the device supplies.

Introduction

Package design for high performance ASICs includes power plane optimization and appropriate placement of package bypass capacitors—in some cases with the addition of externally-placed discrete capacitors. This results in an optimal power supply network system and voltage tolerances that are within specification. This study focuses on the effects of low inductance package capacitors in reducing power supply jitter. Unlike I/O power supplies, the core current drawn by various frequency components is not easily determined. Therefore, the overall power supply bypassing scheme needs to cover the tolerance requirement for the entire estimated operating frequency range.

Substrate effective power supply inductance

One of the main functions of the IC package is to deliver core power from the PCB to the center of the chip. The power/ground pin assignments and the reference plane layer stack in the substrate are designed to minimize the parasitic resistance and inductance and hence minimize change to the supply voltage at the die. The AC fluctuation caused by the substrate inductance is discussed in this section. The substrate resistance also causes DC droop, which will be reviewed in a subsequent section.

As shown in Figure1, the core power supply network in the substrate includes the following interconnects:

Chip	->	Flip Chip (FC) bumps
FC bumps	->	Via from FC bumps
Via from FC bumps	->	VDD/GND trace/plane
VDD/GND trace/plane	->	Via to BGA pins
Via to BGA pins	->	Package pins
Package pins	->	PCB

Each interconnect section has a resistance (R) and an inductance (L), but negligible capacitance (C).

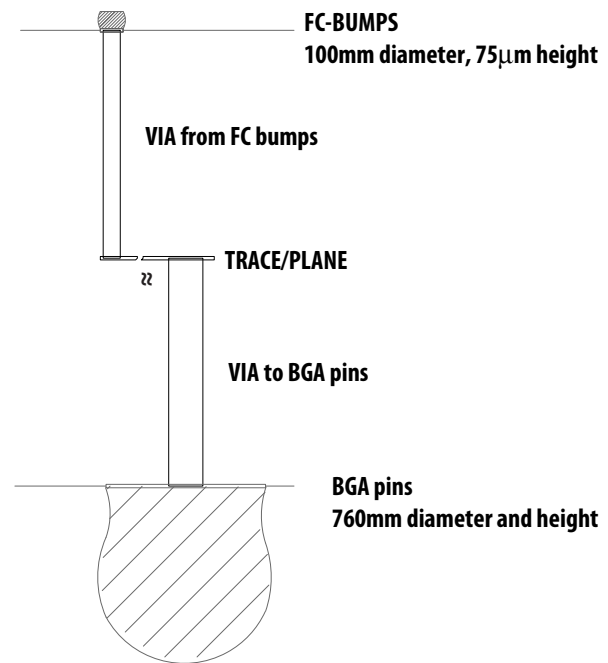


Figure 1. Substrate cross section.

Using a standardized core VDD/GND bump and pin pattern as shown in Figure 2, the resistance and inductance values for the substrate interconnects are shown in Table 1 for the following assumptions:

Chip core size of 8 mm x 12 mm

- Core bump column pitch of 2112 μm
- Number of VDD/GND pins based on a 1% DC voltage drop due to the substrate
- HITCE substrate of 2 mm thickness

For this evaluation, typical values for an Avago Technologies' 0.13 μm package design, as detailed in Table 1, are used.

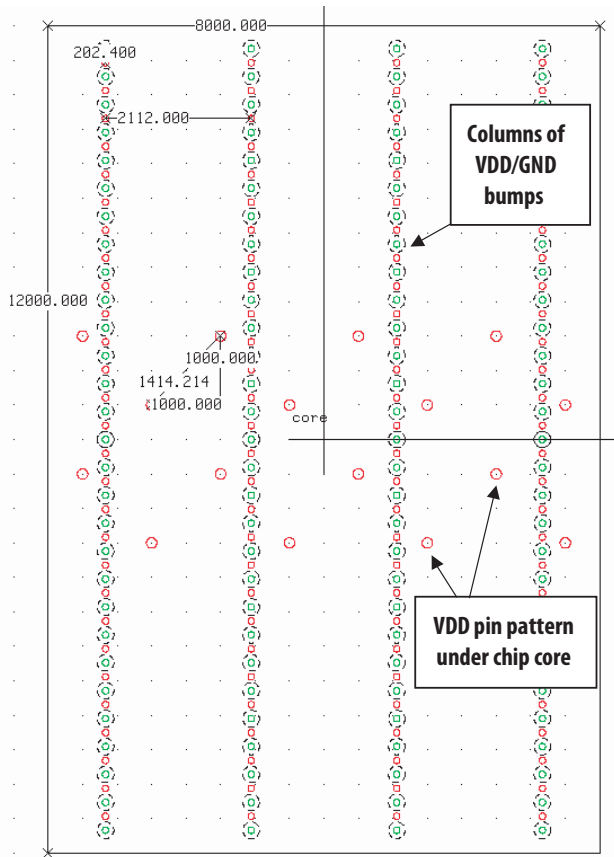


Figure 2. A package VDD plane showing the power connections to die (bumps) and package pins, VDD (red) and GND (green). The GND via connections are shown with the clearances cut out in the VDD plane.

The voltage fluctuation across the inductance is:

$$\Delta V_{DD} = L_{eff} * (di/dt)$$

Where:

ΔV_{DD} = AC power supply fluctuation due to the package inductance (V)

L_{eff} = substrate effective power supply inductance (H)

(di/dt) = the rate of change of the current drawn by the chip core circuitry (A/s)

For example, for high frequency applications, with a core di/dt of 1 A/100 ps, using the representative substrate,

$$L_{eff} = (0.26 + 4.64 + 7.07 + 52.9 + 8.68) \text{ pH} = 73.55 \text{ pH}$$

$$\Delta V_{DD} = 73.55/100 \text{ V} = 0.735 \text{ V}$$

Fortunately, this high frequency fluctuation is not seen at the chip core since it is mostly bypassed by the on-chip capacitance. With the on-chip bypass, the substrate effective power supply inductance is no longer the main factor in power supply jitter, particularly in high frequency applications.

PCB, package and on-chip bypass

A simplified power supply network, its AC equivalent circuit, and the transfer function are shown in Figure 3. This RLC band pass filter is characterized by the resonance frequency, ω_0 , and the quality factor of the tuned circuit, Q1.

$$\omega_0 = 1/[\text{sqrt}(LC)]$$

$$Q = [\text{sqrt}(L/C)]/R$$

Where:

ω_0 = the resonance frequency (rad/s)

Q = $\omega_0/(3\text{-dB BW})$ is the quality factor of the tuned network

R = total resistance in the loop (Ω)

L = total inductance in the loop (H)

C = total (series) capacitance in the loop (F)

Table 1. Representative Package Inductance and Resistance Values

	Bumps	Via from bump: total 116 pairs	VDD/GND plane	Via to pins: total 16 pairs	Package pins
Geometry	Diameter = 100 μm Height = 75 μm	Diameter = 75 μm Length = 1 mm	Width = 8 mm Length = 12 mm	Diameter = 150 μm Length = 1 mm	Diameter = 760 μm Height = 760 μm
L	0.26 pH	4.64 pH	7.07 pH	52.90 pH	8.68 pH
R	0.02 m Ω	0.30 m Ω	0.52 m Ω	0.51 m Ω	0.22 m Ω

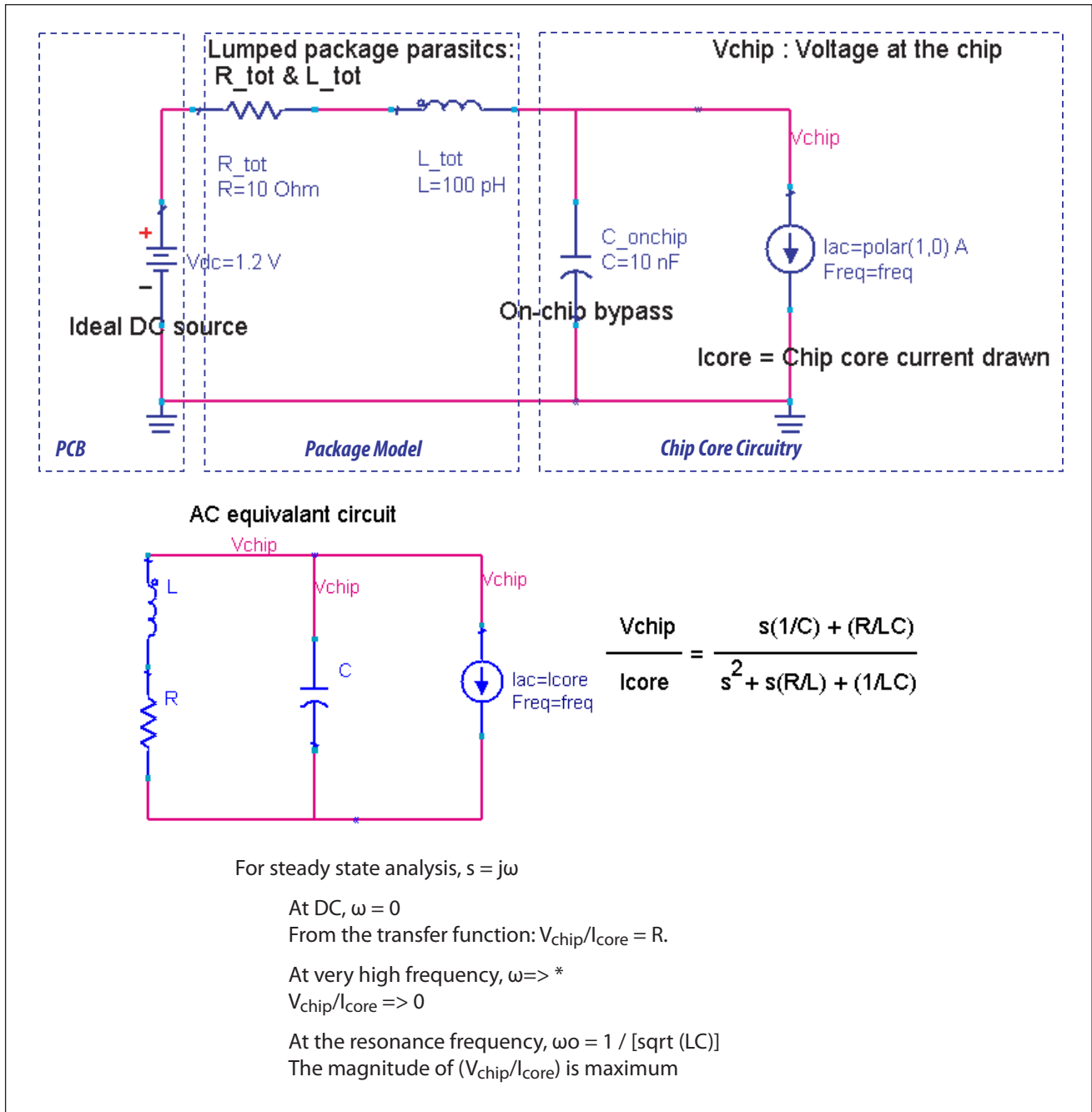


Figure 3. A simplified power supply network as a band pass second-order filter.

A more complete circuit showing the power delivery from the PCB to the chip core is shown in Figure 4. This circuit is used for the sensitivity analysis to determine the relative importance of the on-chip, package, and PCB bypass capacitance for core supply jitter. Since the investigation is focused on the chip voltage fluctuation contributed by the package parasitic inductance, an ideal DC voltage source of 1.2 V was modeled at the PCB, and a variable frequency current source of 1 A at the chip represents the current drawn by the core circuitry.

The effectiveness of the PCB, package, and on-chip capacitors at the low, medium, and high frequency ranges are shown in the following AC simulation results. For this simulation, the base case PCB bypass capacitance is $5 \times 0.22\ \mu\text{F}$, package bypass capacitance is $2 \times 56\ \text{nF}$, and on-chip bypass capacitance is $20\ \text{nF}$.

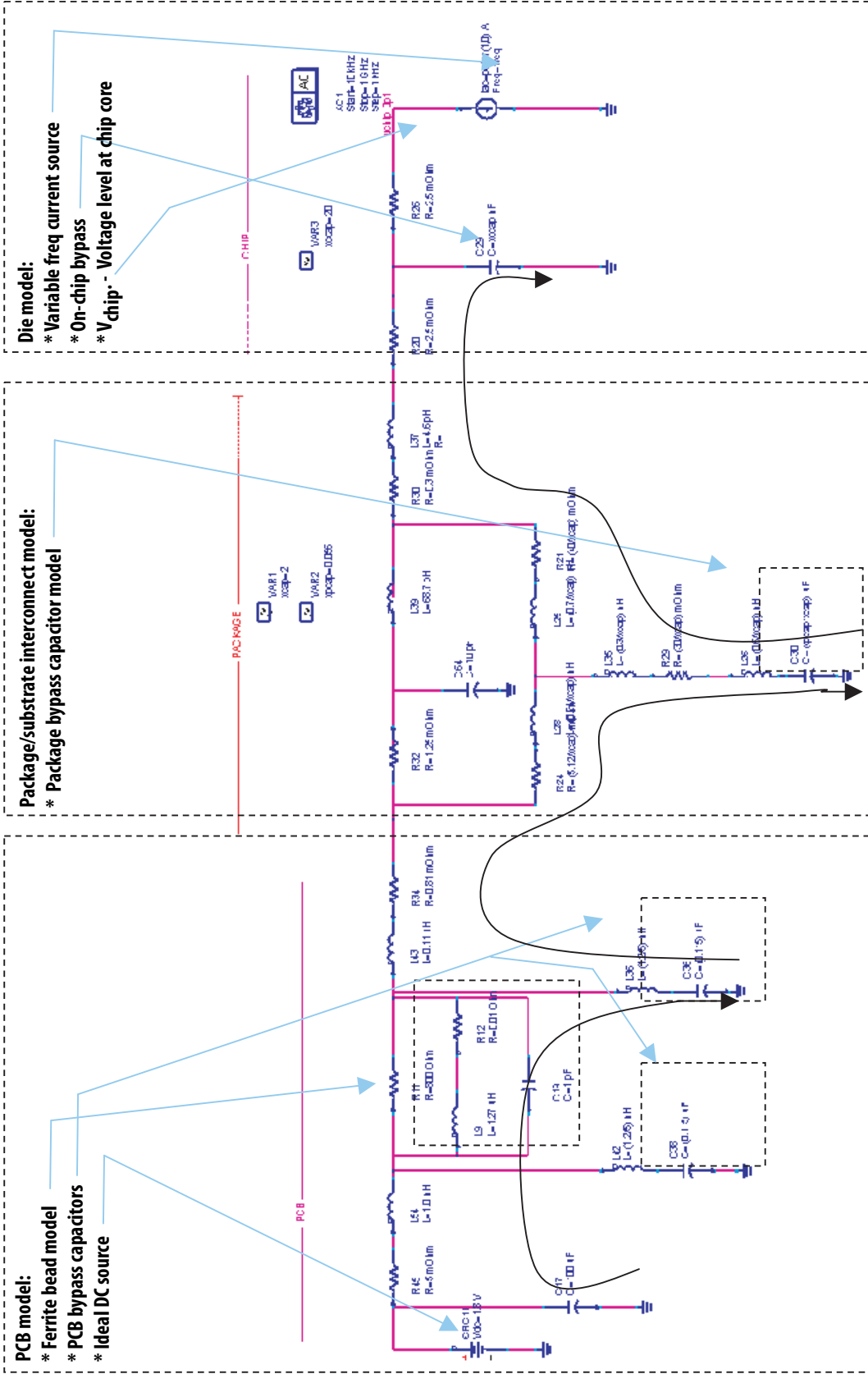


Figure 4. A more complete core power supply network which includes the PCB, package, and die models.

PCB bypassing for the low frequency range of < 5 MHz

An example π structure LC filter on the PCB that includes an RFI ferrite bead and the PCB bypass capacitors is shown in Figure 5. (This is just an example; the actual schematic changes with different PCB applications.) In the schematic, the two main components are the inductor L9 (ferrite bead) and the capacitor C36 ($5 \times 0.22 \mu\text{F}$) outlined in the rectangles.

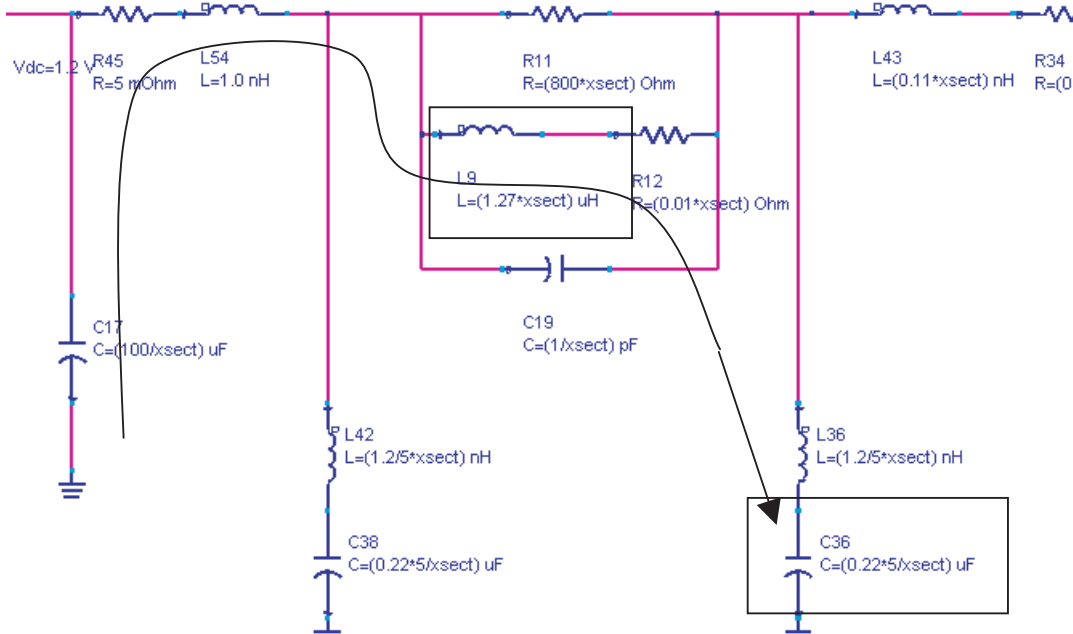


Figure 5. The low frequency band pass filter of the power supply network with series inductance of $1.27 \mu\text{H}$ and effective capacitor values of $5 \times 0.22 \mu\text{F}$.

Figure 6 shows the magnitude of die voltage fluctuations with various PCB capacitor values, assuming a flat 1 A core current drawn at all frequencies. The large capacitance and inductance values provide a low frequency band pass filter at the resonance frequency of less than 1 MHz. A larger capacitance value would shift the peak to a lower frequency and reduce the peaking amplitude.

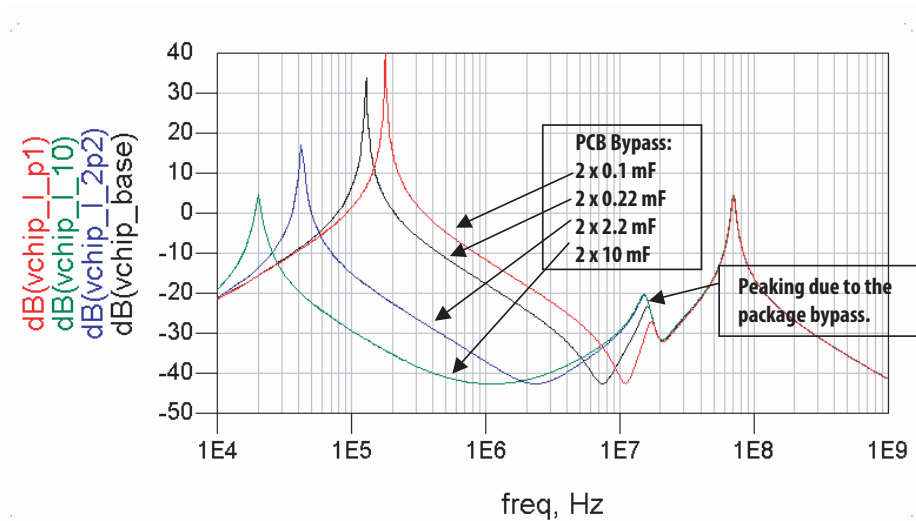


Figure 6. Vchip frequency spectrum for various PCB bypass capacitor values, base case package bypass of $2 \times 0.056 \mu\text{F}$, and on-chip bypass of 20 nF .

Figure 7 shows no change in the lower range (less than 1 MHz) frequency spectrum when the package bypasses of 2 x 56 nF are removed, even though the high frequency peak amplitude is larger.

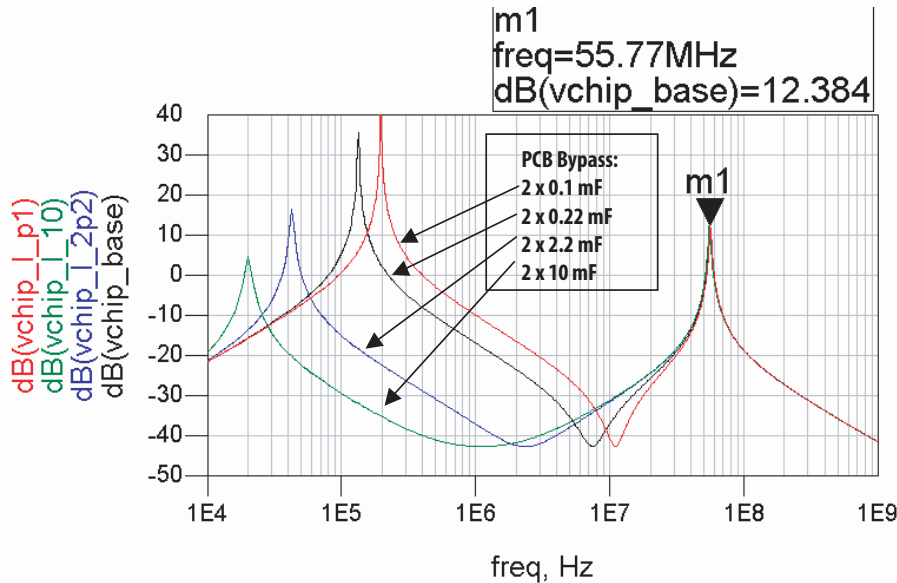


Figure 7. Vchip frequency spectrum using the same PCB and on-chip bypass capacitor values in Fig. 6, but no package bypass. Simulation results show medium frequency peaking, 8 dB higher peak at the high frequency range: the marker m1 shows peaking amplitude of 12.38 dB @ 56 MHz, in comparison with the 4 dB @ 70 MHz in Figure 6.

Package bypassing for the medium frequency range of 5 -100 MHz

Figure 8 shows the package core supply model using a typical chip core size of 8 mm x 12 mm, standardized TS13 core bumps, and 16 pairs of VDD/GND pins.

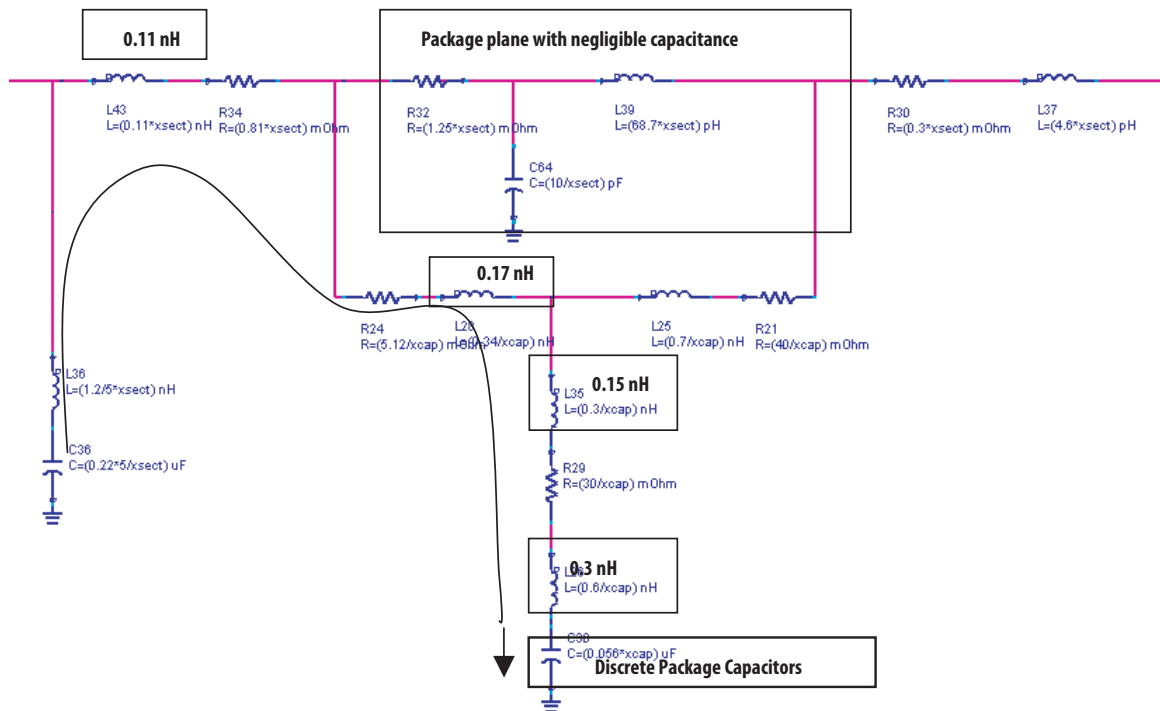


Figure 8. Package core supply interconnect model showing the long inductance path of 0.73 nH to the package capacitors.

Figures 9 and 10 show the simulation results when changing the number and the value of the package bypass capacitors. In all cases, the package capacitor does not offer improvement in reducing high frequency core power ripple. The curves converge at the frequency of 150 MHz in the case of two-package bypass (Figure 9) and at 300 MHz in the case of eight-package bypass (Figure 10).

The package bypass of 22-56 nF could reduce the supply ripple in some applications where the peak core current is in a very narrow medium frequency range of 20-70 MHz.

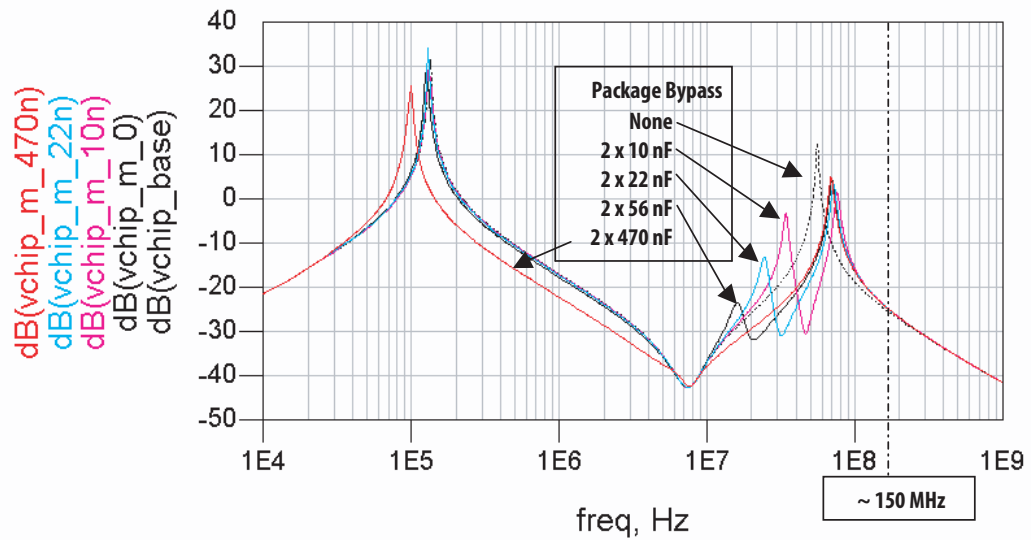


Figure 9. Vchip frequency spectrum for various values of package bypass, base case PCB bypass of 2 x 0.22 μ F, and on-chip bypass of 20 nF.

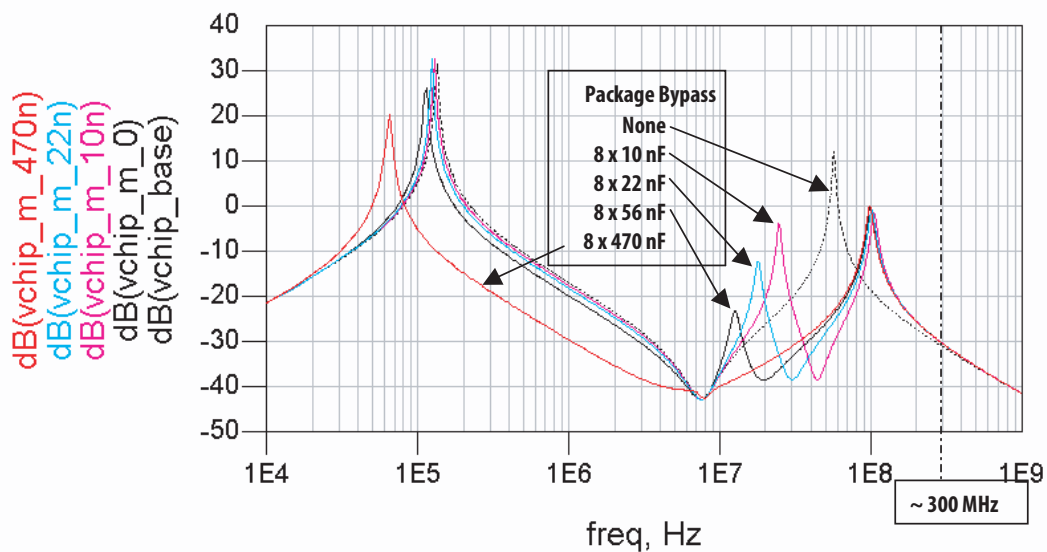


Figure 10. Same as Figure 9 with four times the quantity of package bypass, base case PCB bypass of 2 x 0.22 μ F, and on-chip bypass of 20 nF.

On-chip bypassing for the high frequency range of > 100 MHz

Figure 11 shows the high frequency loop where the main components are:

C = On-chip bypass

L = Inductance from PCB bypass // inductance from package bypass

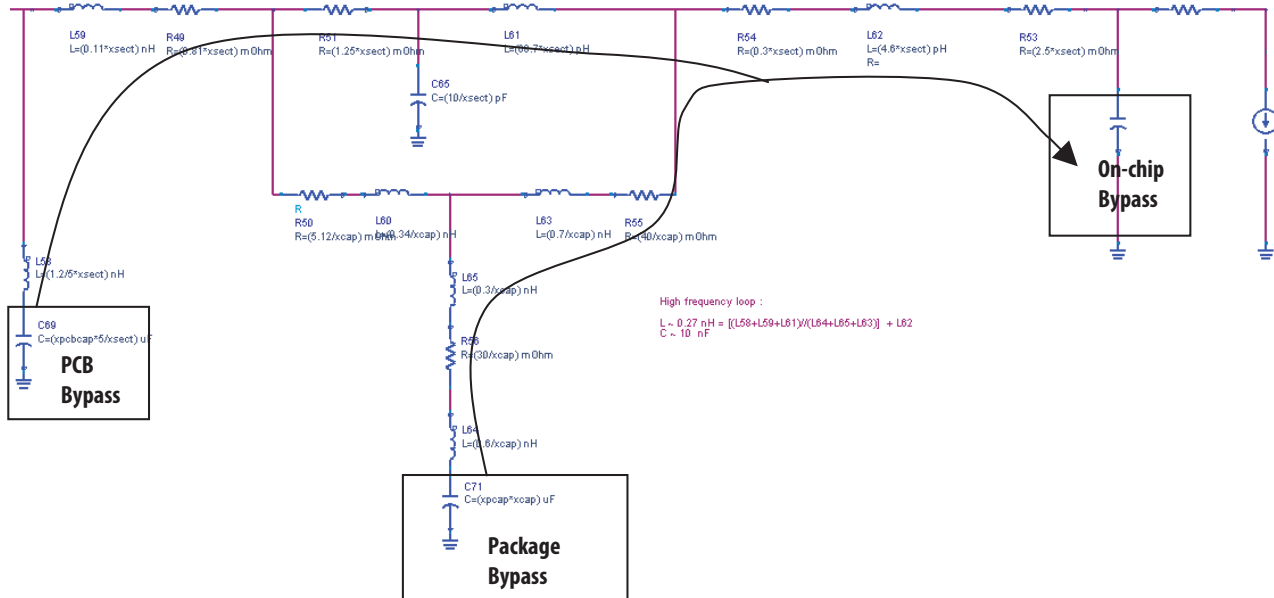


Figure 11. A section of the power supply network that represents the high frequency band pass filter where the on-chip bypass (smallest value) is the effective capacitance in the loop.

Figures 12 through 14 show the AC simulation for the combined lumped on-chip bypass capacitance value of 5-40 nF with 1A of AC current drawn by the core circuitry. In actual products, the on-chip capacitors are distributed throughout the die close to the core circuitry and, therefore, should supply better instantaneous current to different sections of the core.

Simulation results in Figure 12 show different high frequency responses for different values of on-chip bypass capacitors. For the representative power supply network used in this analysis, with a flat 1 A core current frequency spectrum, the 40 nF on-chip bypass capacitor limits the supply jitter to 50 mV for frequencies above 100 MHz, while an on-chip bypass of 5 nF provides the same 50 mV limitation for frequencies above 700 MHz. Figures 13 and 14 show no effect of package bypass for the high frequency range core ripple.

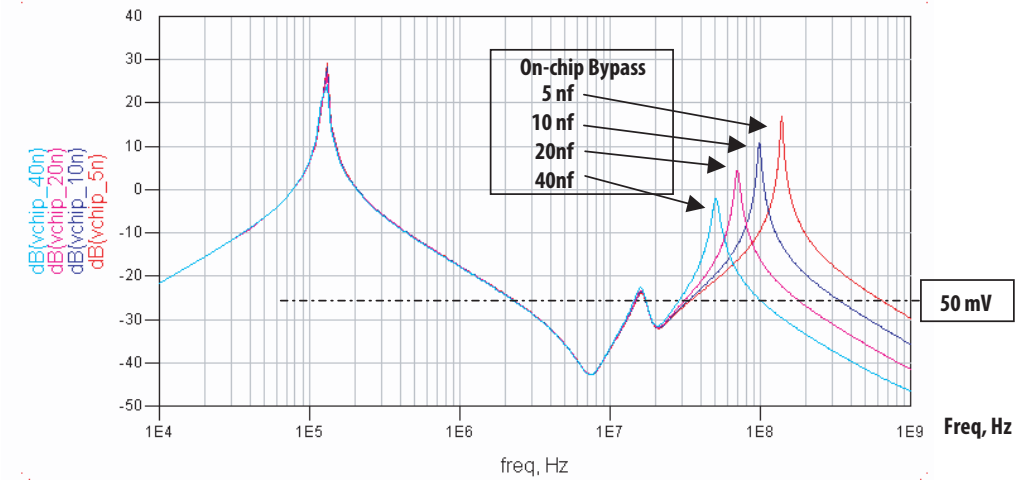


Figure 12. Vchip frequency spectrum for various on-chip capacitance values with the base case PCB bypass of 5 x 0.22 μ F, and package bypass of 2 x 56 nF.

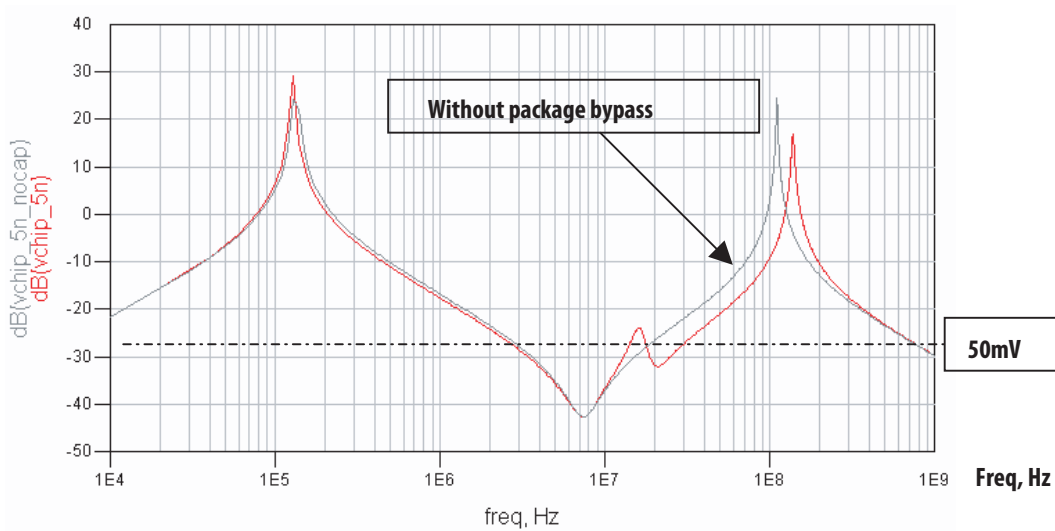


Figure 13. Vchip frequency spectrum comparison for on-chip bypass of 5 nF, base case PCB bypass, with and without package bypass of 2 x 56 nF.

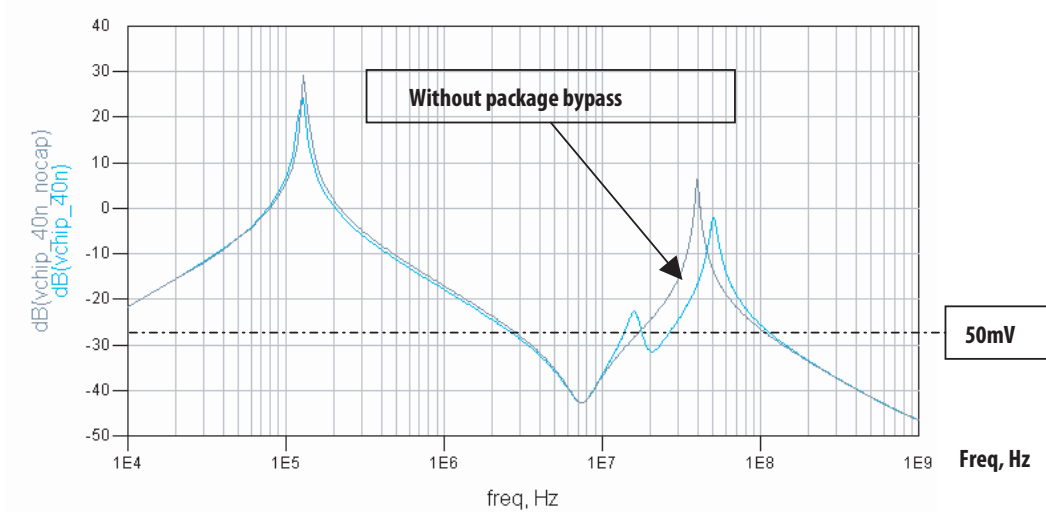


Figure 14. Vchip frequency spectrum comparison for on-chip bypass of 40 nF, base case PCB bypass, with and without package bypass of 2 x 56 nF.

DC droop

The analysis has addressed the AC voltage fluctuation, which is mostly determined by:

- The on-chip bypass for the high frequency range
- The PCB bypass for the low frequency range

The analysis indicates that package bypass can only help in low margin situations.

In addition to the inductance, the substrate also adds resistance to the power supply network. The higher resistance (lower Q) can help to dampen the resonance amplitude and distribute the noise over a wider frequency range. Unfortunately, the same resistance causes a DC voltage drop that offsets the AC fluctuation to a lower voltage level, and therefore, lowers the power supply noise margin.

The DC resistance includes the PCB interconnect from the DC-DC converter to the package pins (R_{pcb}), package interconnect (R_{pkg}) and the power grid on the die (R_{die}). The total DC resistance varies from system to system, depending on the part location in reference to the DC source on the PCB and the distance from the core circuitry to the closest bump.

The representative circuitry in Figure 4 shows $R_{pcb} = 5.81 \text{ m}\Omega$, $R_{pkg} = 1.55 \text{ m}\Omega$, $R_{die} = 5 \text{ m}\Omega$. If the R_{pcb} has been compensated for at the PCB, the total resistance is in the range of 3-6.55 m Ω . With this resistance range, a core RMS current of 5-10 A would cause a DC drop of 15-65.5 mV. For the core supply voltage of $1.2 \text{ V} * 10\%$ ($1200 * 120 \text{ mV}$), this DC offset lowers the allowed AC fluctuation to $120 - 65.5 = 54.5 \text{ mV}$. A better alternative is to boost the PCB supply voltage to compensate for the average DC drop of 40 mV. In this case, the allowed AC fluctuation amplitude will be 95 mV if the PCB voltage supply is 1.24 V.

In general, the package interconnect resistance can be reduced by increasing the number of VDD/GND pins. Table 2 provides a quick guide to the minimum number of core power pins required for different core power levels based on the allowed package DC drop of 1% to 5% and the maximum current carrying capability of substrate interconnects.

Table 2. Minimum number of core power pins for a HITCE flip-chip substrate to meet the specified DC drop due to the substrate.

Core power	Max current of 1 A/pin	Substrate DC drop = 1 %	Substrate DC drop = 2 %	Substrate DC drop = 2.5 %	Substrate DC drop = 5 %
5 W	8 pins	16 pins	8 pins	6 pins	3 pins
10 W	17 pins	32 pins	16 pins	13 pins	6 pins
15 W	25 pins	49 pins	24 pins	19 pins	10 pins
20 W	33 pins	65 pins	32 pins	26 pins	13 pins
25 W	42 pins	81 pins	40 pins	32 pins	16 pins
30 W	50 pins	97 pins	49 pins	39 pins	19 pins
35 W	58 pins	113 pins	57 pins	45 pins	23 pins
40 W	67 pins	129 pins	65 pins	52 pins	26 pins
45 W	75 pins	146 pin	73 pins	58 pins	29 pins
50 W	83 pins	162 pins	81 pins	65 pins	32 pins
55 W	92 pins	178 pins	89 pins	71 pins	36 pins

Conclusions

- Discrete bypass capacitors attached to the flip-chip package have minimal impact on the chip core supply voltage fluctuation. The on-chip bypass devices play a more critical role in meeting the core supply voltage specification.
- An accurate model of the core current frequency spectrum in the system application can help the designers meet the voltage specification without adding excess on-chip bypass. To minimize the possibility of operating at peak frequencies, this analysis should be jointly completed by the designers of the PCB, package, and chip at an early stage in the design cycle.
- For larger die with high currents, a slight boost in the PCB voltage level could relax the AC voltage ripple specification. This is true for all frequency ranges and is not limited to the core supply voltage.

References

- [1] Budak, Aram, *Passive and Active Network Analysis and Synthesis*, Houghton Mifflin, 1974.

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