DIGITAL WE DAYS 2023

CORRELATION BETWEEN CALCULATION AND PRACTICE FOR SIMPLE TOP-TO-BOTTOM PCB HEAT DISSIPATION USING TIM & VIAS

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

TODAY'S SPEAKERS

PRESENTATION
Andreas Nadler
Field Application Engineer

MODERATION
Markus Eberle
Marketing Department

INFORMATION ABOUT THE WEBINAR

You are muted during the webinar.
However, you can ask us questions using the chat function.

Duration of the presentation	30 Min
Q&A:	10 – 15 Min

Any questions?
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On our channel	Würth Elektronik Group
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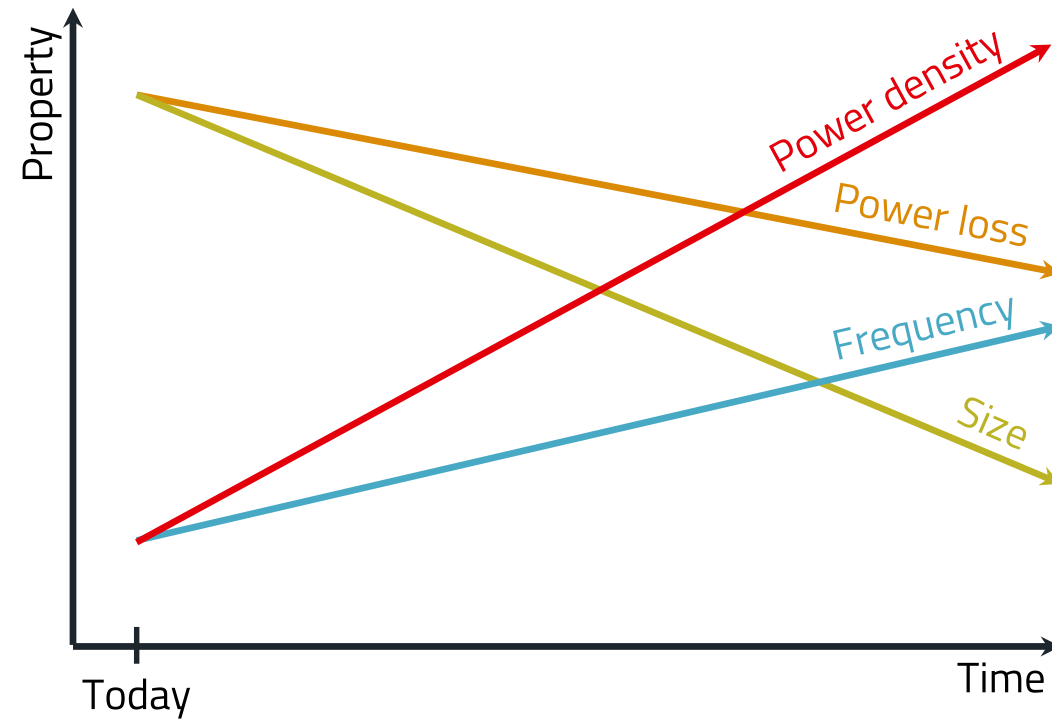
INTRODUCTION

The Need for Thermal Management

- Electronic design tendencies:



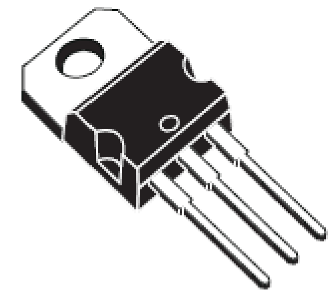
THERMAL DEMO PCB

Heat Source

- Thermal demo PCB with LDO (LD1086) and variable load → Pv is adjustable
- Different packages with different *Rth-JC* & *Rth-JA* are available

- For this demo / calculation / simulation we chose:

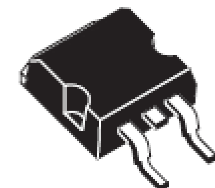
➢ TO220(Rth-JC = 5 K/W , Rth-JA = 50K/W) direct connected to a heatsink with 7,8K/W



TO-220

➢ D2PACK(Rth-JC = 3K/W , Rth-JA = 62,5K/W) indirect connected with a 11x11 via array from the PCB Bottom to TOP side, a Würth TIM and fineally a different heatsink with 3,5K/W

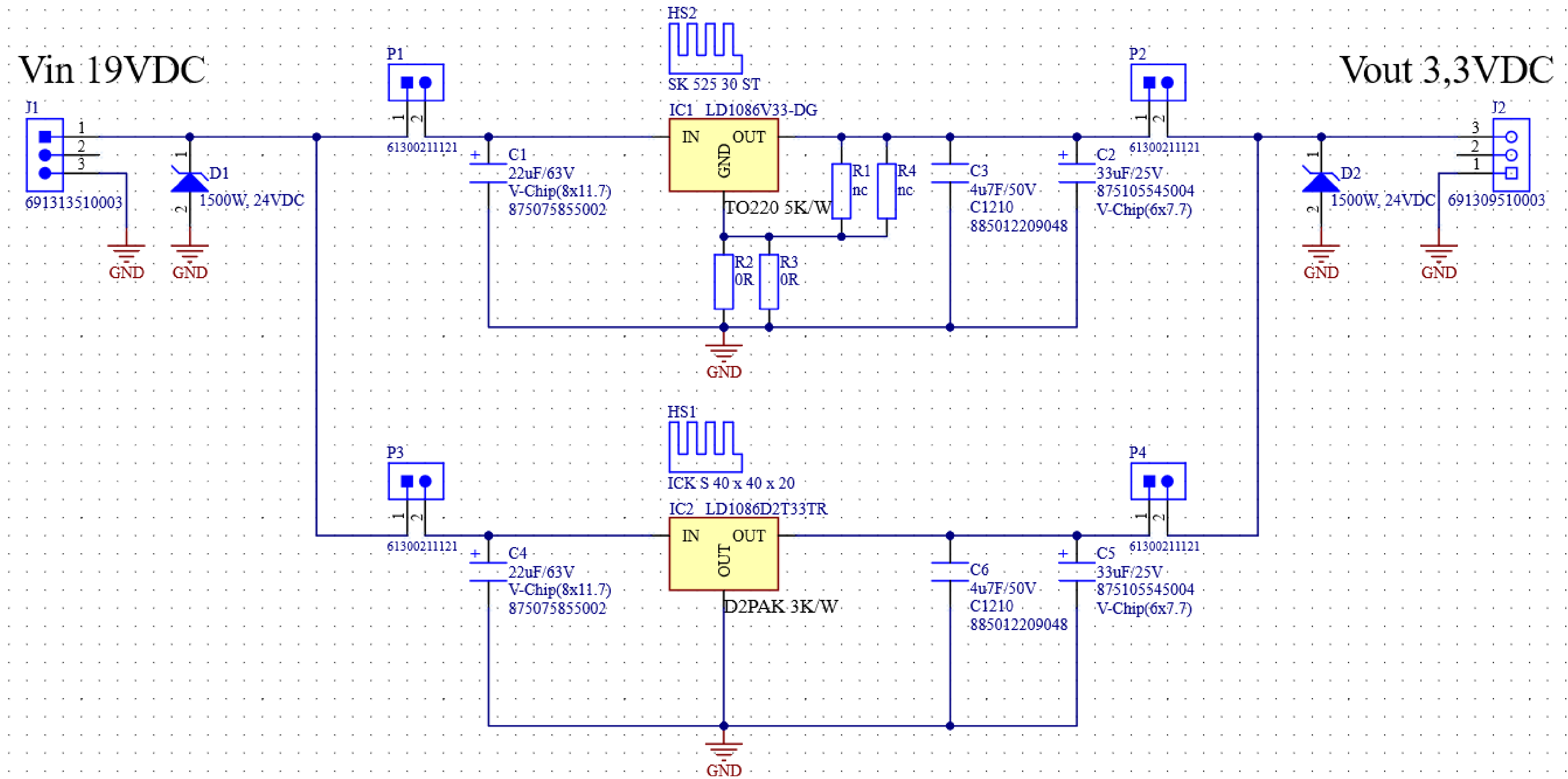
T_{STG}	Storage temperature range	-55 to +150	°C
T_J	Junction temperature range	-40 to +150	°C



D²PAK

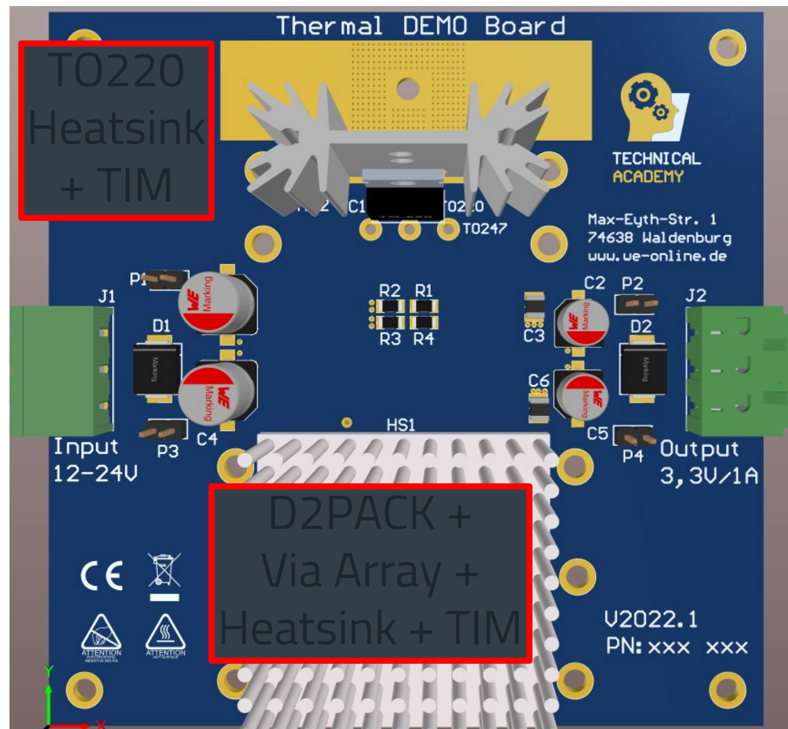
THERMAL DEMO PCB

Schematic

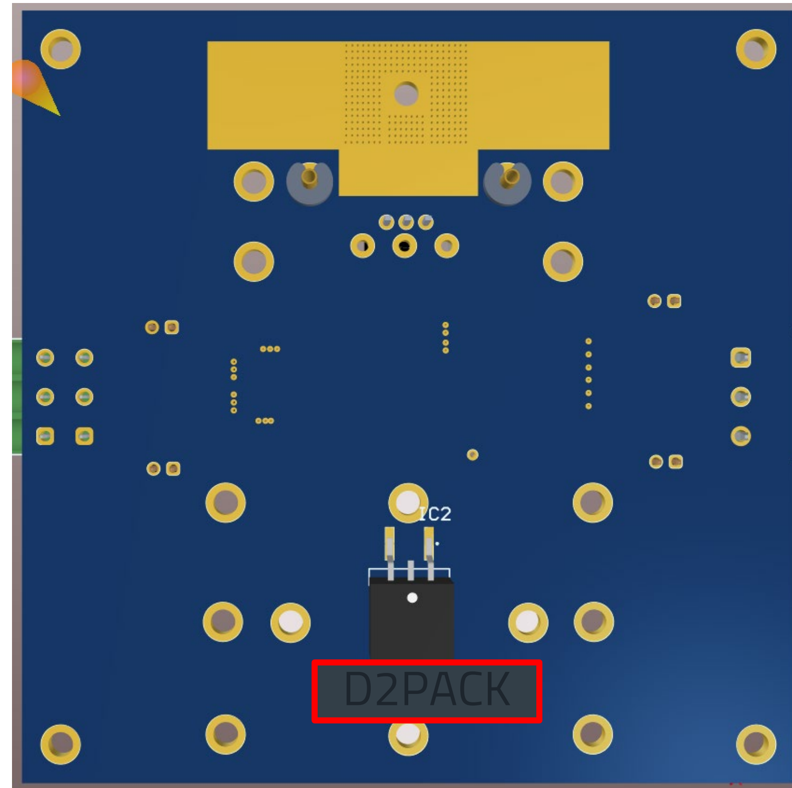


THERMAL DEMO PCB

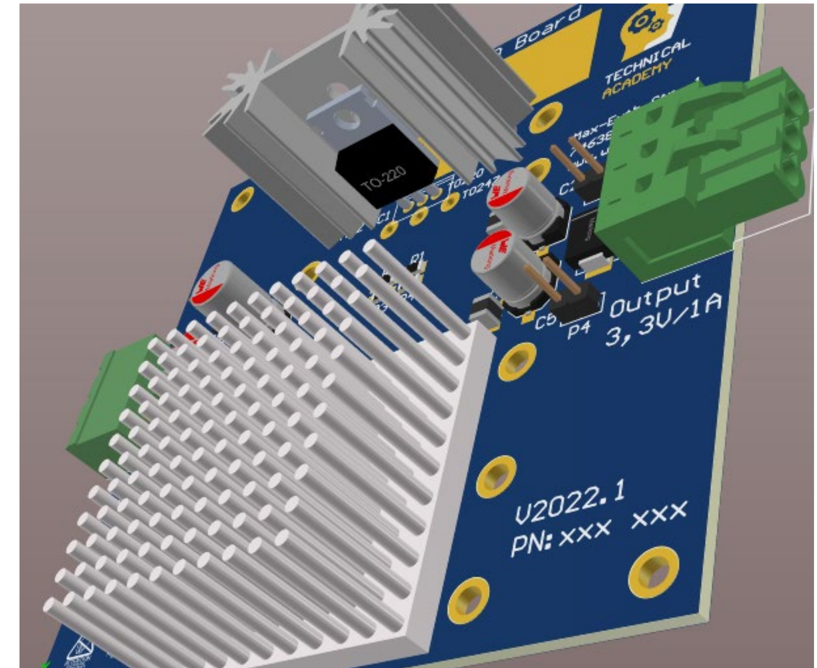
3D PCB View



Top View



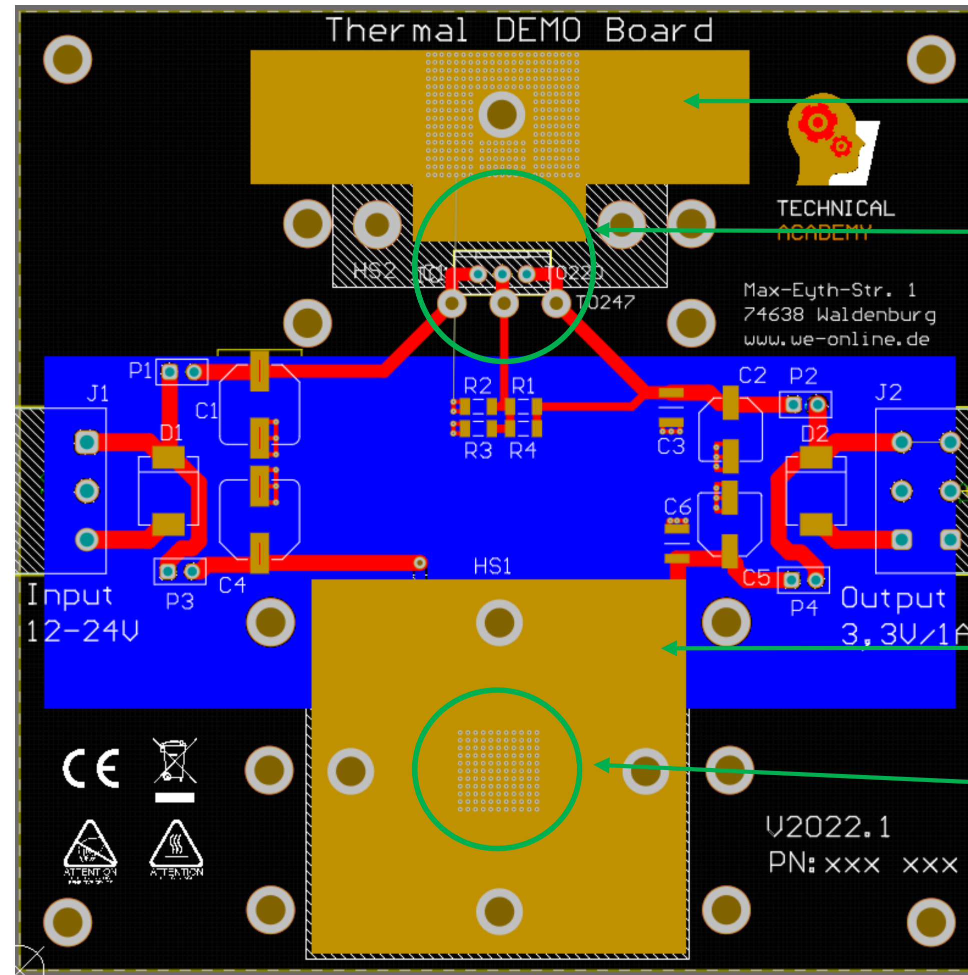
Bottom View



Side View

THERMAL DEMO PCB

2D PCB Top View



TIM Area TOP / Bottom Bare Copper

TO220/TO247

TIM Area TOP / Bare Copper

11x11 Via Array (no filling)

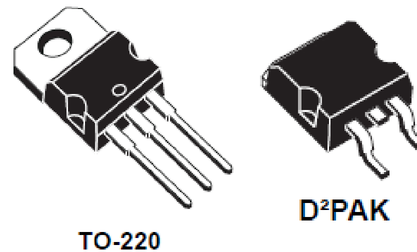
THERMAL DEMO PCB

Thermal Resistance of Different Packages

- **No heatsink used**
  - Lets look at the datasheet

Table 2. Thermal data

Symbol	Parameter	TO-220	D^2PAK D^2PAK/A	DPAK	DFN8 (4x4)	Unit
R_{thJC}	Thermal resistance junction-case	5	3	8	1.5	°C/W
R_{thJA}	Thermal resistance junction-ambient	50	62.5	100	33	°C/W



Without a heatsink:

$$R_{th-ja} = 50/62.5 \, \frac{\mathrm{K}}{\mathrm{W}}$$

THERMAL DEMO PCB

Thermal Resistance of D²PAK Package

- **Let's add a 2 Layer FR4 PCB with Via Array, TIM and passive heatsink!**

Table 2. Thermal data

Symbol	Parameter	TO-220	D²PAK D²PAK/A	DPAK	DFN8 (4x4)	Unit
R_{thJC}	Thermal resistance junction-case	5	3	8	1.5	°C/W
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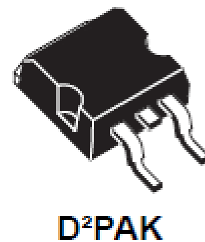


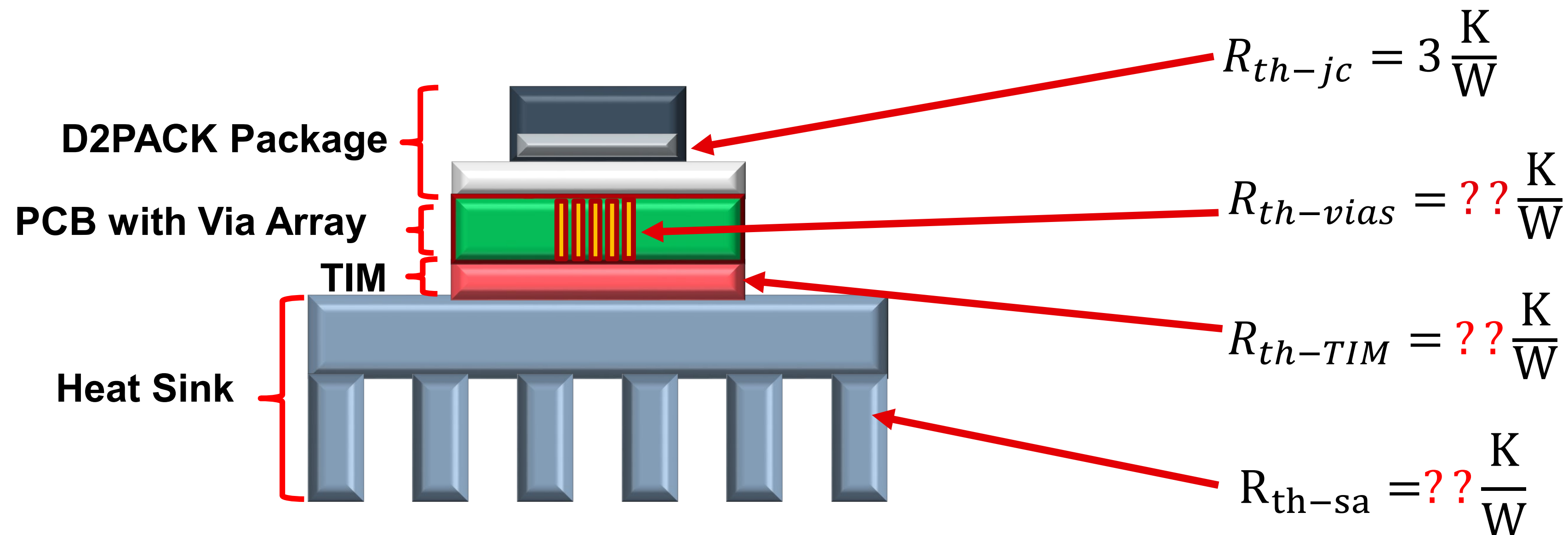
D²PAK

With a heatsink: $R_{th-jc} = 3\,\frac{\mathrm{K}}{\mathrm{W}}$

THERMAL DEMO PCB

Real Setup

- **2 Layer FR4 PCB with via array, TIM and passive heatsink!**



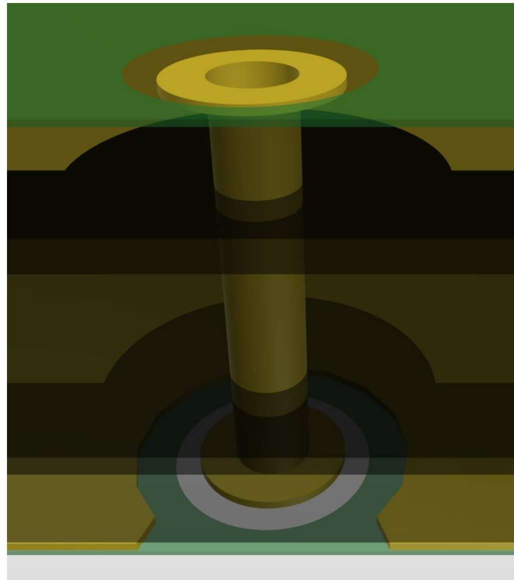
Notice: At first we ignore the copper and FR4 lateral heat spreading in this case! We only take care of the vertical heat spreading! We also ignore the thermal radiation and Rth-ja of the LDO package

THERMAL DEMO PCB

Thermal Resistance of Via

- Inner diameter: 0.6mm
- Length: 1.6mm

Type of Via	Thermal Resistance
Via 35µm copper plating, no filling	64 K/W
Via 35µm copper plating, solder filled	42 K/W
Via 70µm copper plating, no filling	34 K/W
Via fully copper filled	14 K/W



WE

THERMAL DEMO PCB

Modeling FR4 with Via Array (No Filling)

- $\lambda_{via_{array}} \approx \lambda_{Cu} \cdot \frac{[d_{via}^2 - (d_{via} - 2 \cdot d_{Cu})^2] \cdot \frac{\pi}{4}}{d_{pitch}^2}$

$\lambda_{via_{array}} = Thermal\ conductivity\ via\ array \left[\frac{W}{m \cdot K}\right]$

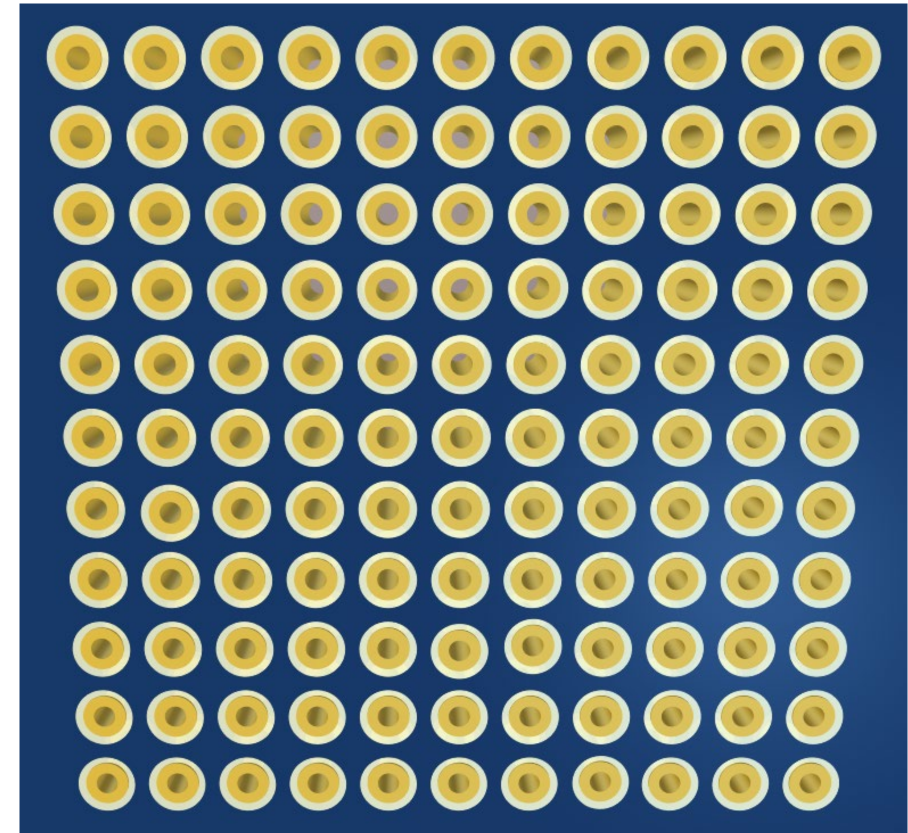
$\lambda_{Cu} = Thermal\ conductivity\ copper\ 380 \left[\frac{W}{m \cdot K}\right]$

$d_{via} = Outer\ diameter\ via\ hole\ with\ copper\ plating [m]$

$d_{Cu} = Via\ hole\ copper\ plating [m]$

$d_{pitch} = Distance\ via\ to\ via\ center [m]$

Standard vias are much cheaper than filled/plated ones!



11x11 via array(0.3mm drill) with 0.8mm pitch

THERMAL DEMO PCB

Example Calculation of Via Array (No Filling)

$$\lambda_{via_{array}} \approx \lambda_{Cu} \cdot \frac{\left[d_{via}^2 - (d_{via} - 2 \cdot d_{Cu})^2\right] \cdot \frac{\pi}{4}}{d_{pitch}^2} \approx 380 \frac{W}{m \cdot K} \cdot \frac{\left[0{,}0003m^2 - (0{,}0003m - 2 \cdot 0{,}0000175m)^2\right] \cdot \frac{\pi}{4}}{0{,}0008^2 m} \approx 9 \frac{W}{m \cdot K}$$

$$Rth_{Via_{array}} \approx \frac{l}{\lambda_{via_{array}} \cdot A} \approx \frac{0{,}0016m}{9 \frac{W}{m \cdot K} \cdot (0{,}011m \cdot 0{,}011m)} \approx 1{,}5 \frac{K}{W}$$

$\lambda_{Cu} = Thermal\ conductivity\ copper \approx 380 \left[\frac{W}{m \cdot K}\right]$

$d_{via} = Outer\ diameter\ via\ hole\ with\ copper\ plating (0{,}3mm)[m]$

$d_{Cu} = Via\ hole\ copper\ plating (17{,}5\mu m)[m]$

$d_{pitch} = Distance\ via\ to\ via\ center\ (0{,}8mm)[m]$

$N = Quantity\ of\ vias (121)$

$Rth_{Via_{array}} = Via\ array\ thermal\ resistance \left[\frac{K}{W}\right]$

$l = Via\ hole\ lenght\ (1{,}6mm)[m]$

$A = Pad\ size\ component\ (11x11mm)\ [m^2]$

$\lambda_{via_{array}} = Thermal\ conductivity\ via\ array \left[\frac{W}{m \cdot K}\right]$

TO220 effective cooling area is roughly 11mm x 11mm

THERMAL DEMO PCB

FEA Simulation of Different Via Arrays

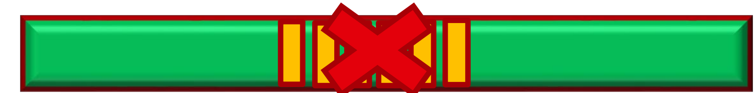
Matrix	Number of Vias	Via Pitch (mm)	Result in K/W	Reduction in %
0 x 0	0	N/A	15,9 (1,6mm FR4)	0%
1 x 1	1	10	14,2	10,8%
2 x 2	4	5	10,5	34,3%
3 x 3	9	3,3	7,3	54,3%
4 x 4	16	2,5	5,2	67,5%
5 x 5	25	2,0	3,8	75,8%
6 x 6	36	1,7	3,0	81,1%
7 x 7	49	1,4	2,5	84,6%
8 x 8	64	1,3	2,1	86,8%
10 x 10	100	1,0	1,7	89,6%
11 x 11	121	0,9	1,5	90,4%

THERMAL DEMO PCB

Thermal Resistance of FR4 Only

- Double layer 1.6mm FR4 without vias

$$R_{th-FR4} \approx \frac{\frac{1}{\lambda_{FR4}} \cdot d}{A} \approx \frac{\frac{1}{0{,}25\,\frac{W}{m \cdot K}} \cdot 0{,}0016m}{0{,}011m \cdot 0{,}011m} \approx 53\,\frac{K}{W}$$



$$\lambda_{FR4} = Thermal\ conductivity\ FR4 \approx 0{,}25 \left[\frac{W}{m \cdot K}\right]$$

$$d = FR4\ thickness[m]$$

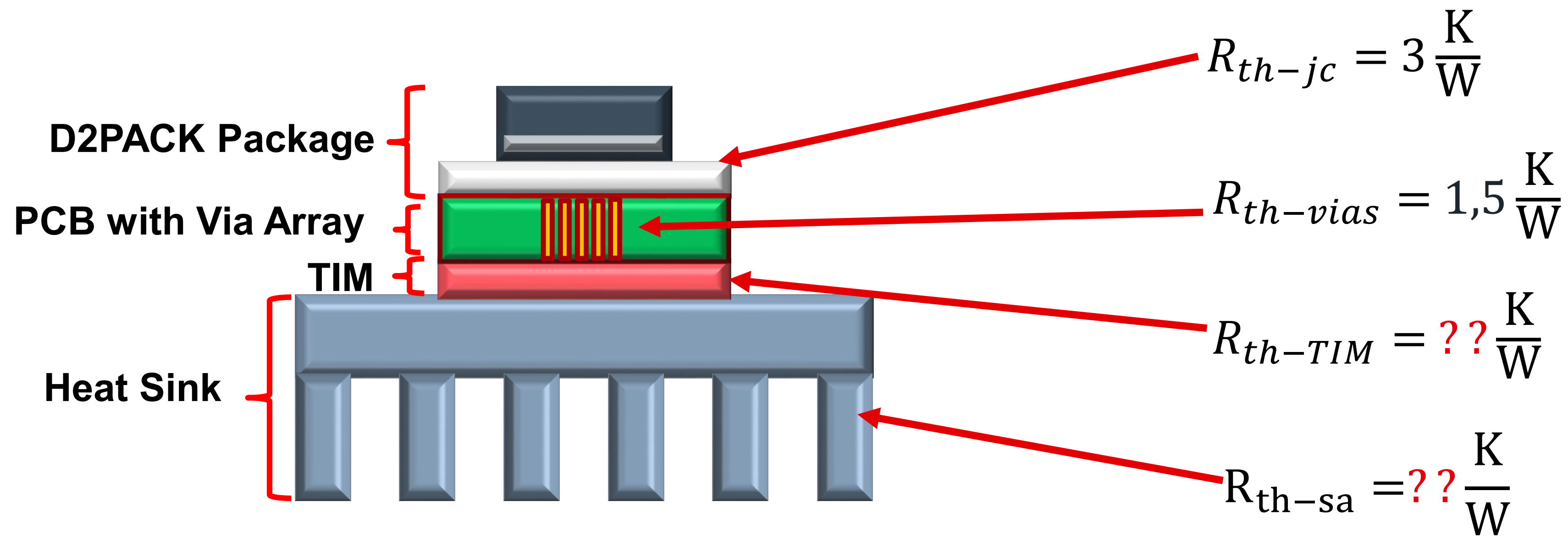
$$A = Cooling\ surface[m^2]$$

- The thermal resistance of FR4 only in this case would be 35 times higher !
- FR4 PCB with NO thermal vias

THERMAL DEMO PCB

Real Setup

- **2 Layer FR4 PCB with via array, TIM and passive heatsink!**



THERMAL DEMO PCB

Thermal Resistance of TIM

- Modeling thermal resistance of an insulator Pad
- 40x40mm/0,5mm 6W/m*K

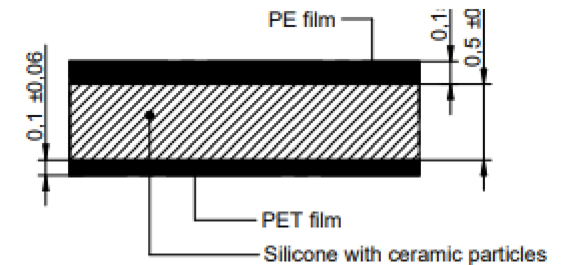
$$R_{th-TIM} = \frac{l}{\lambda \cdot A} = \frac{0{,}0005m}{6\frac{W}{m \cdot K} \cdot (0{,}04m \cdot 0{,}04m)} = 0{,}052\frac{K}{W}$$

$$l = Material\ thickness\ of\ TIM\,[m]$$

$$A = Contact\ surface\ area\ of\ TIM\,[m^2]$$

$$\lambda = Thermal\ conductivity\ coefficient\ of\ TIM\,[\frac{W}{m \cdot K}]$$

Calculation thermal resistance of TIM

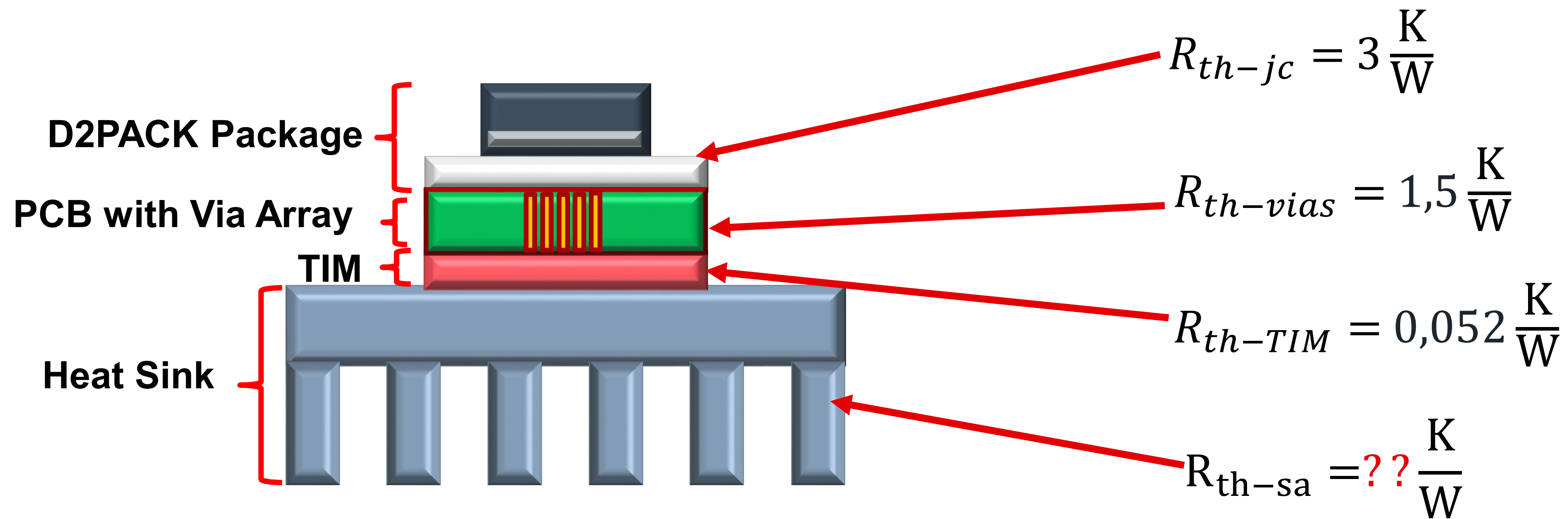


WE-TGF 40016005

THERMAL DEMO PCB

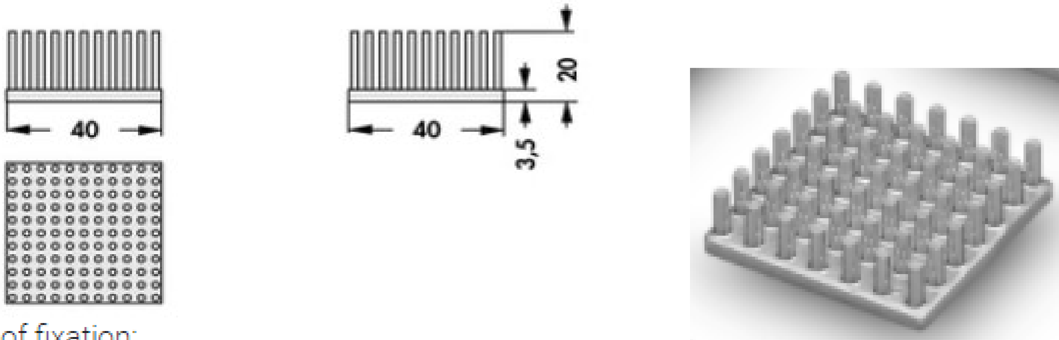
Real Setup

- **2 Layer FR4 PCB with via array, TIM and passive heatsink!**

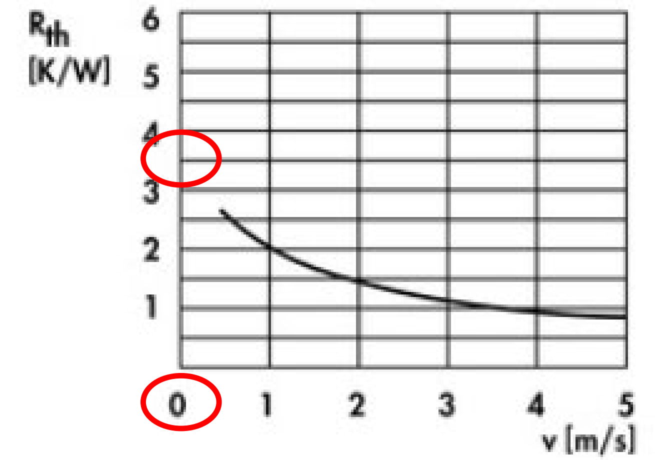


THERMAL DEMO PCB

Heatsink



way of fixation:	• therm. conductive foil • therm. cond. adhesive
socket:	universal
suitable for processor type:	universal
width:	40 mm
height:	20 mm
plate thickness:	3.5 mm
weight:	29 g
length:	40 mm
thermal resistance:	3.5 - 0.9 K/W
dissipation loss:	21.4 W
surface:	Al-natural



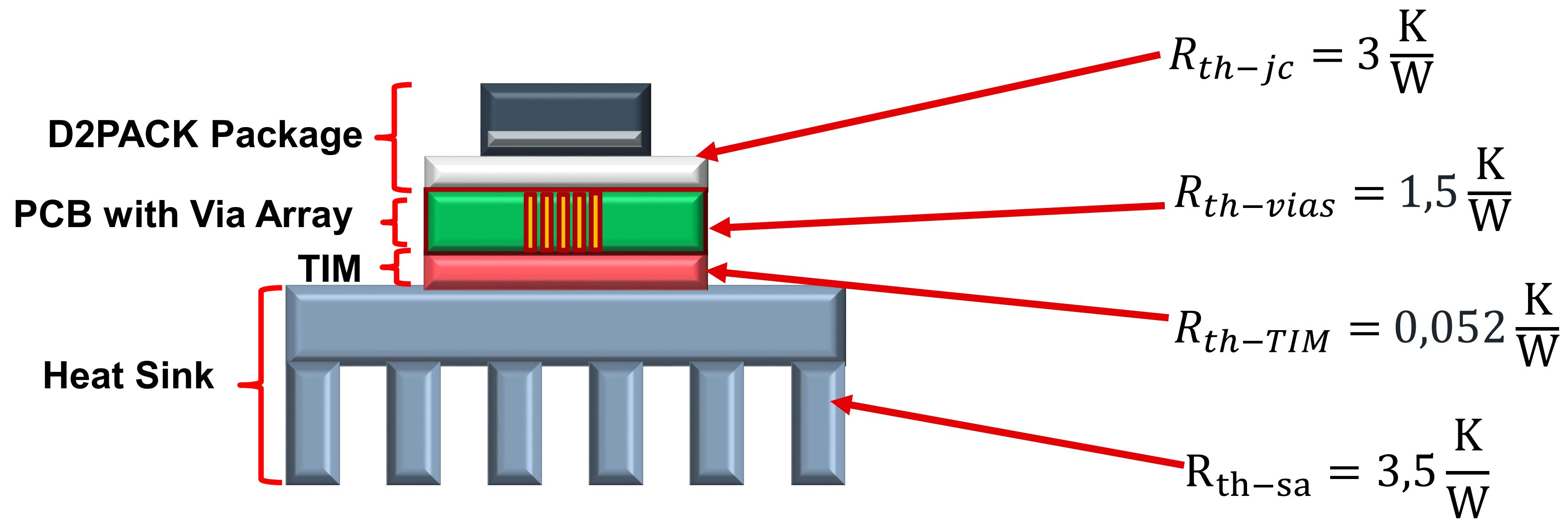
Natural convection:

$$R_{th-sa} = 3{,}5\,\frac{\mathrm{K}}{\mathrm{W}}$$

THERMAL DEMO PCB

Real Setup

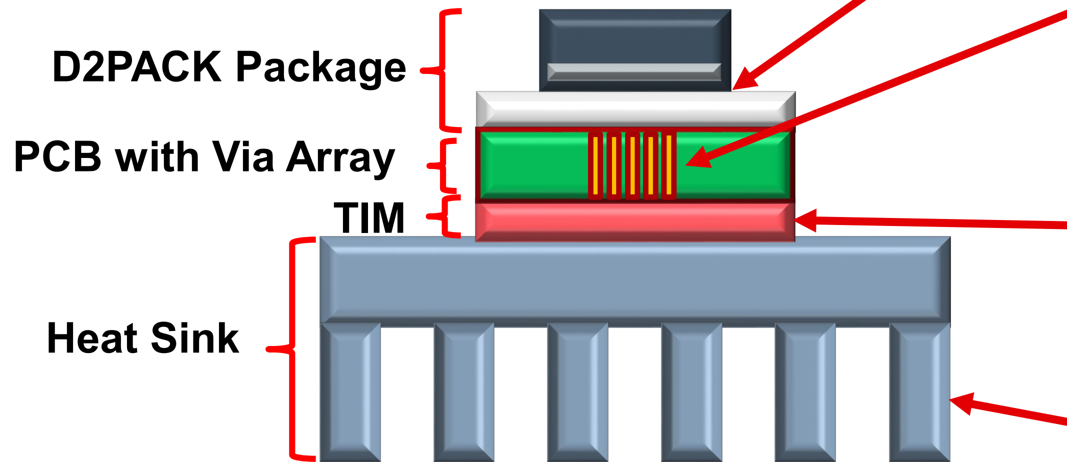
- **2 Layer FR4 PCB with via array, TIM and passive heatsink!**



THERMAL DEMO PCB

Maximum Junction Temperature

- **2 Layer FR4 PCB with via array, TIM and passive heatsink!**



P_{Loss} = 3,3W

$3K/W * 3{,}3W + 44\,ºC \approx$ 54°C

$R_{th-jc} = 3\,\frac{K}{W}$

$1{,}5K/W * 3{,}3W + 39°C \approx$ 44°C

$R_{th-vias} = 1{,}5\,\frac{K}{W}$

$0{,}052K/W * 3{,}3W + 38°C \approx$ 39°C

$R_{th-TIM} = 0{,}052\,\frac{K}{W}$

$3{,}5K/W * 3{,}3W + 26°C \approx$ 38°C

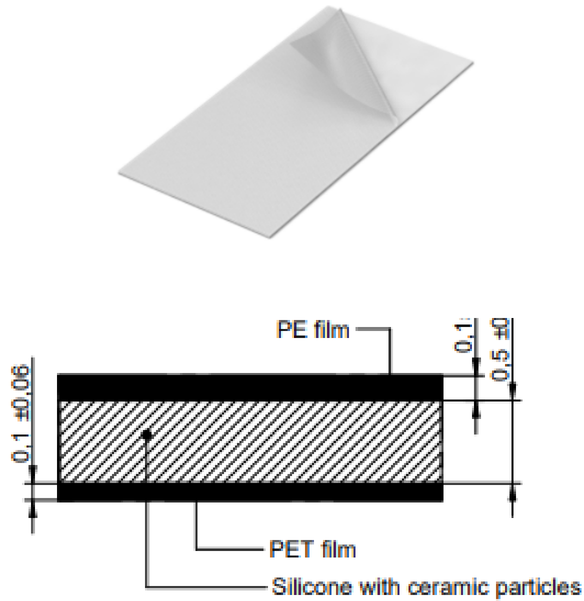
$R_{th-sa} = 3{,}5\,\frac{K}{W}$

Ambient Temp. 26°C

THERMAL DEMO PCB

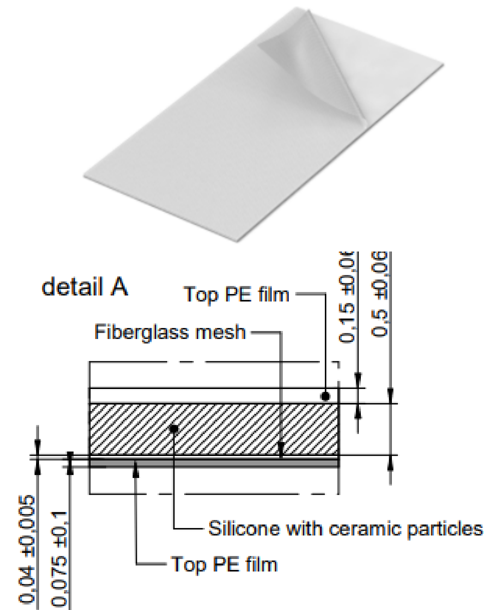
Impact of the TIM Thickness

- Reference: WE-TGF 40006005
- 40x40mm / 0,5mm / 6W/m*K
- 0,052 K/W



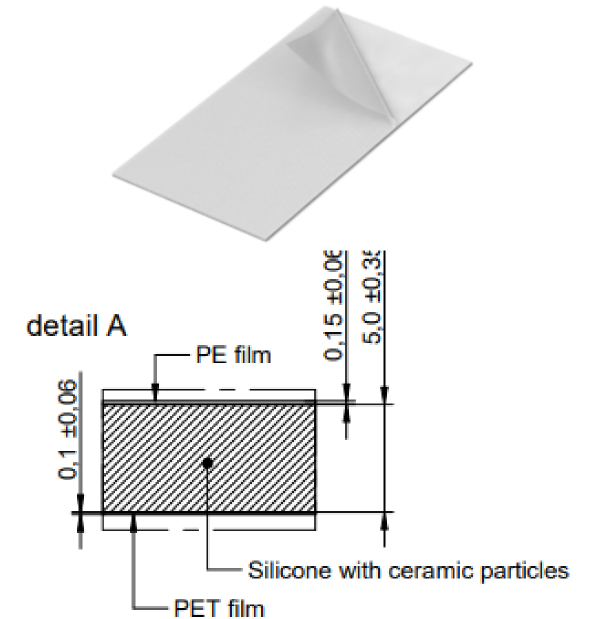
LDO Temp ≈ 49°C

- WE-TGF 40111005
- 40x40mm / 0,5mm / 1W/m*K
- 0,31 K/W



LDO Temp ≈ 50°C

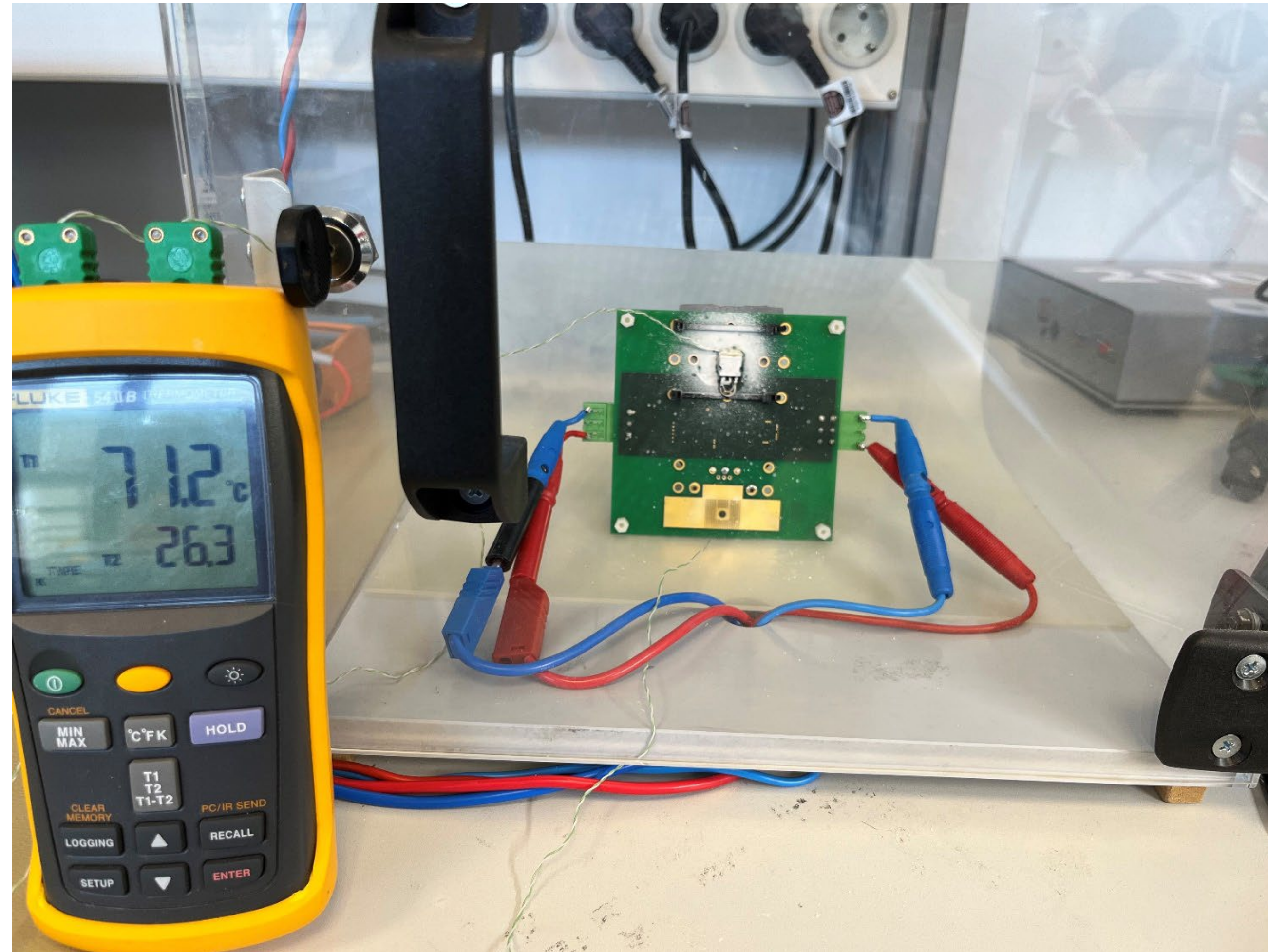
- WE-TGF 40011050
- 40x40mm / 5mm / 1W/m*K
- 3,1 K/W



LDO Temp ≈ 59°C

THERMAL DEMO PCB

Measurement Setup

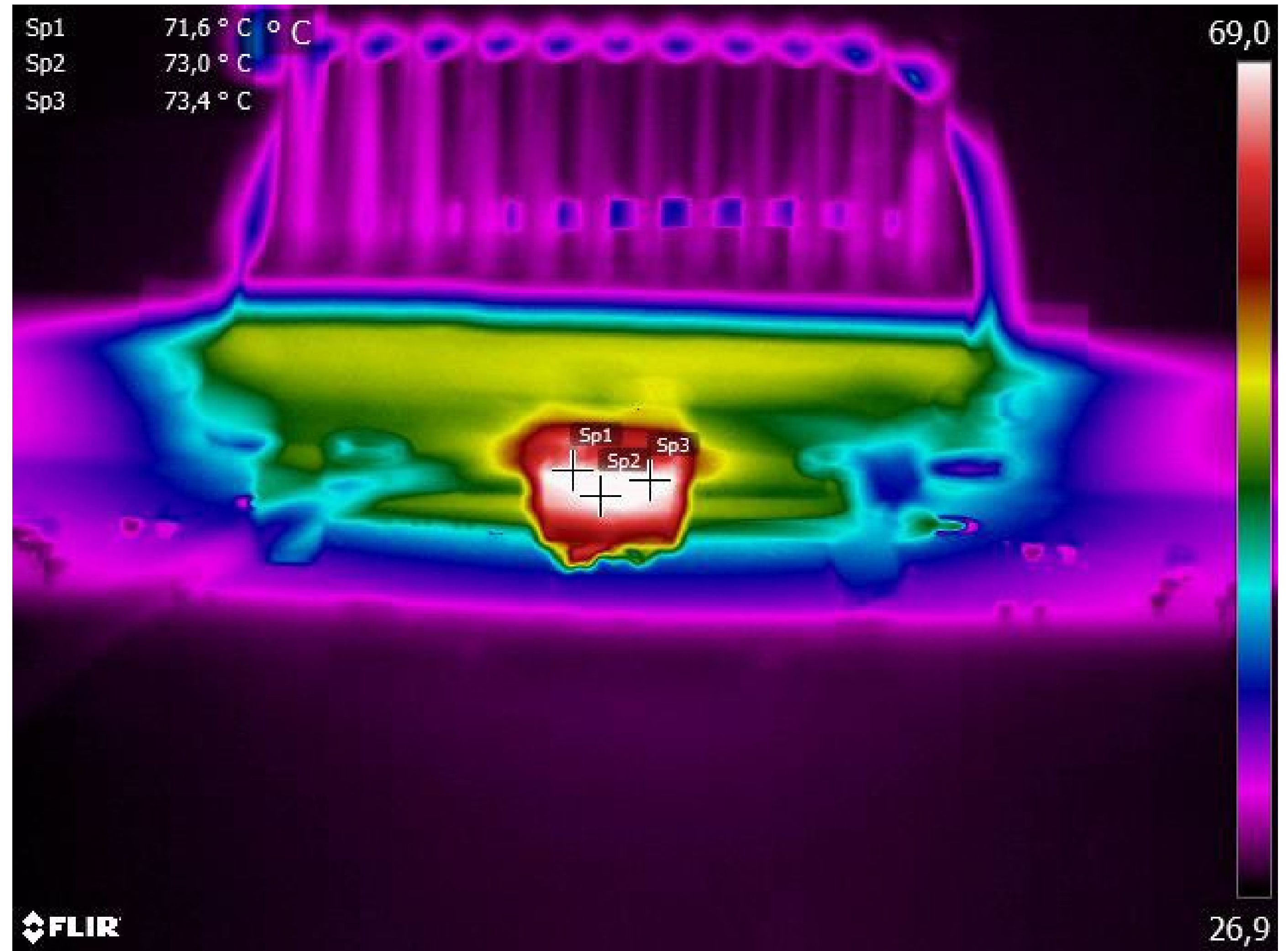


WE

THERMAL DEMO PCB

Measurement with Strapped Heatsink + WE-TGF

- Ambient temp = 26°C
- Max temp = 73.4°C (SP3)
- Fluke measurement point 71.6° (SP1)
- Calculated was 54°C
- Deviation between calculation & measurement is around **20°C**

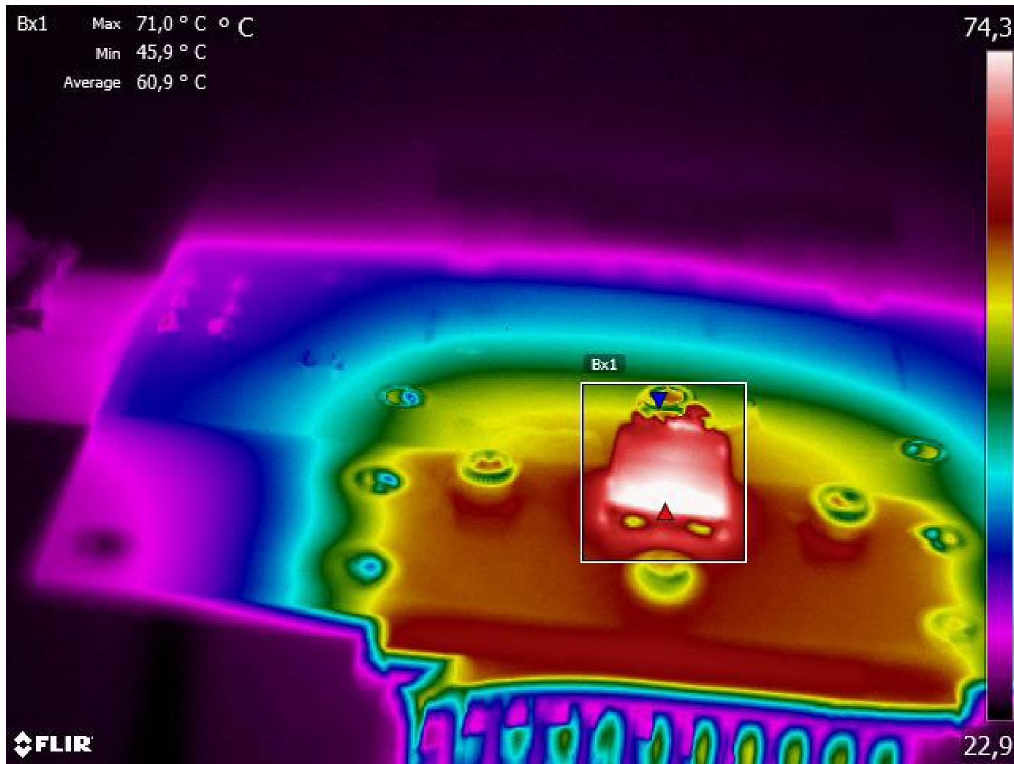


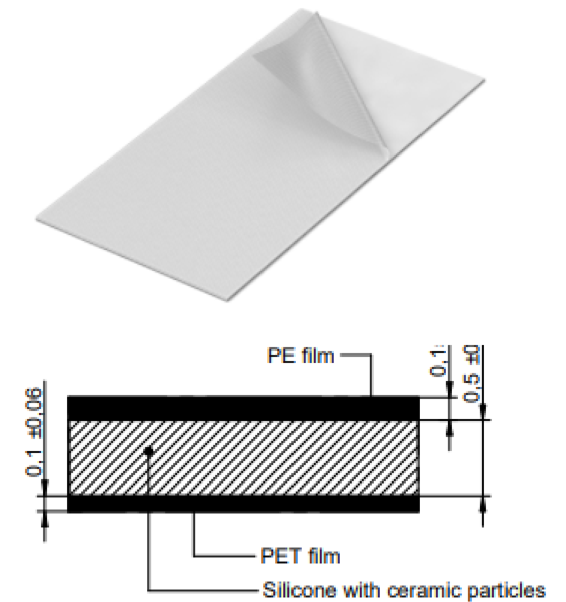
THERMAL DEMO PCB

Measurement with Screwed Heatsink + WE-TGF

- Calculated LDO Temp @3.3W is = **54°C**
- Measurement result LDO with ICKS404020 heatsink + srews @3.3W = **71°C**
- → **17°C** difference

- WE-TGF 40016005
- 40x40mm/0.5mm





THERMAL DEMO PCB

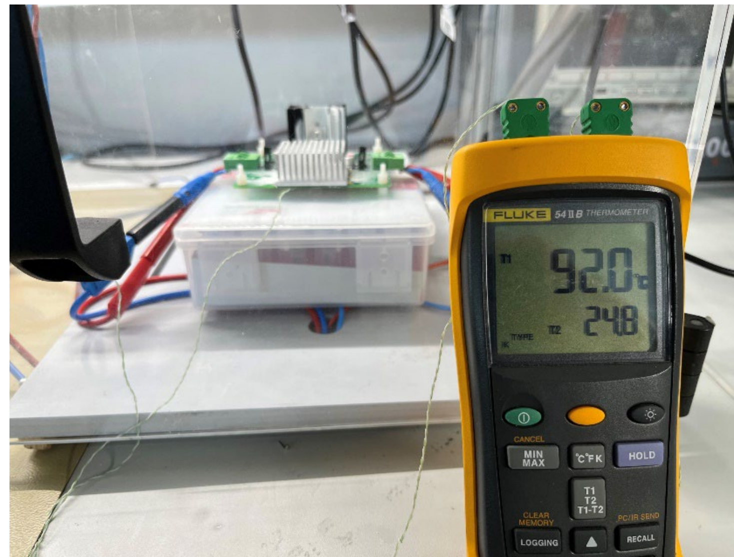
Measurement with Strapped Heatsink + WE-PCM

- Calculated LDO Temp @5W is = 66°C

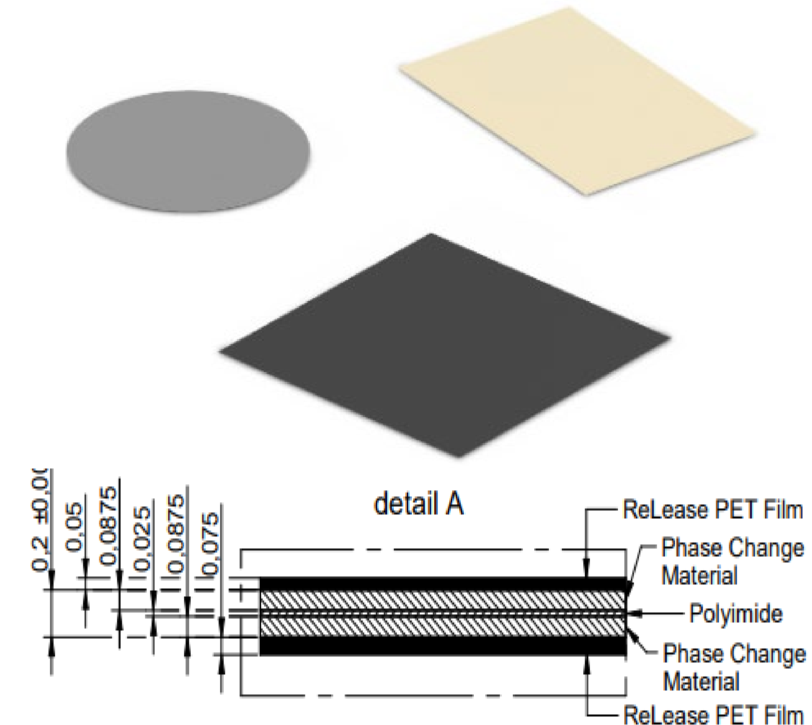
$$R_{th-PCM} = \frac{l}{\lambda \cdot A} = \frac{0{,}0002m}{5\frac{W}{m \cdot K} \cdot (0{,}04m \cdot 0{,}04m)} = 0{,}025\frac{K}{W}$$

- Measurement result LDO with ICKS404020 heatsink @ 5W = 92°C

- → 26°C difference



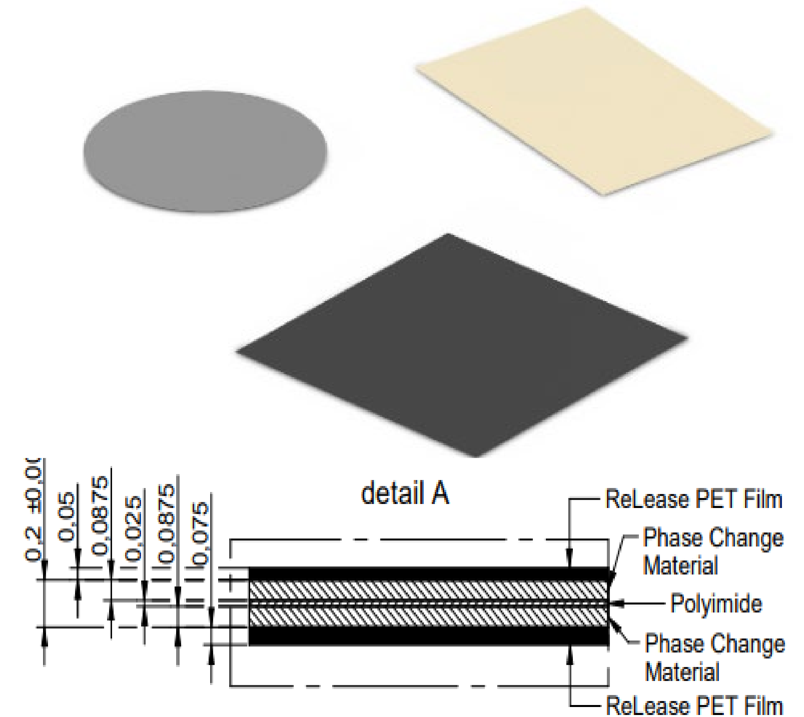
- WE-PCM **402150101020**
- Phase change material
- Phase change temp=60°



THERMAL DEMO PCB

Measurement with Strapped Heatsink + WE-PCM

- WE-PCM **402150101020**
- Phase change material
- Phase change temp=60°

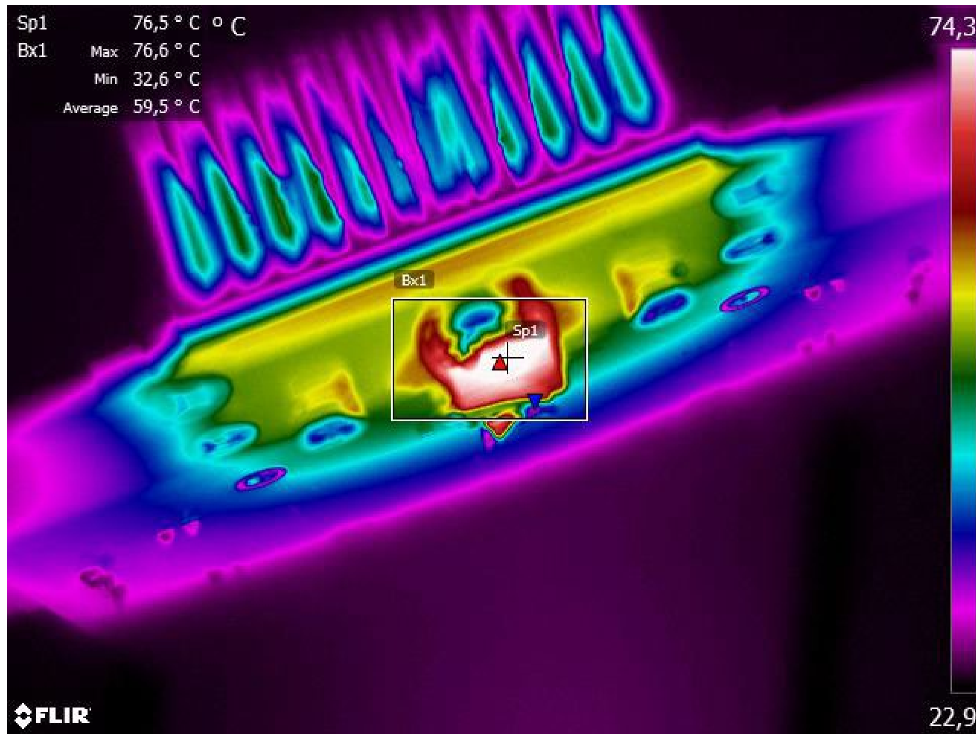


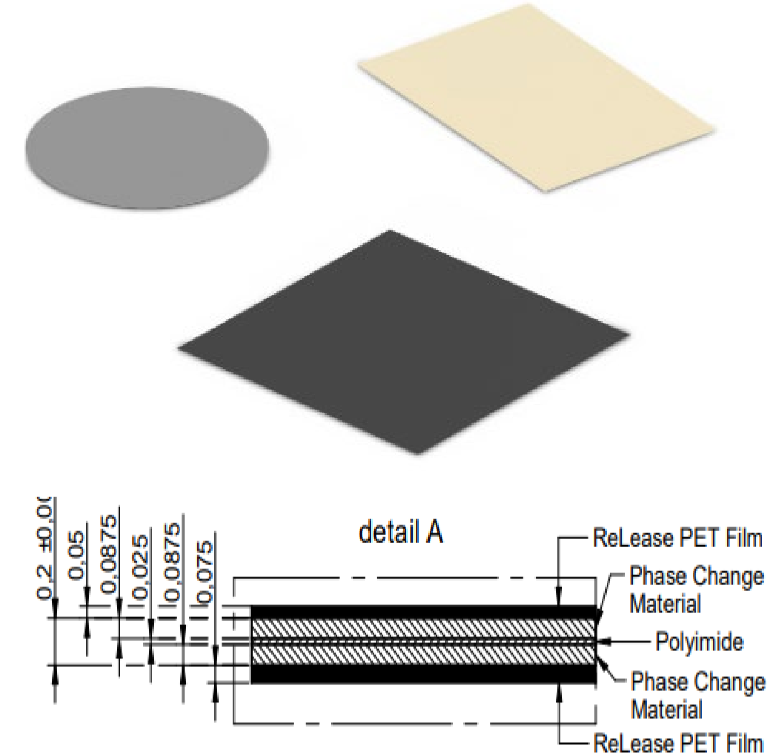
THERMAL DEMO PCB

Measurement with Screwed Heatsink + WE-PCM

- Calculated LDO Temp @5W is = **66°C**
- Measurement result LDO with ICKS404020 heatsink + srews @ 5W = **77°C**
- → **11°C** difference

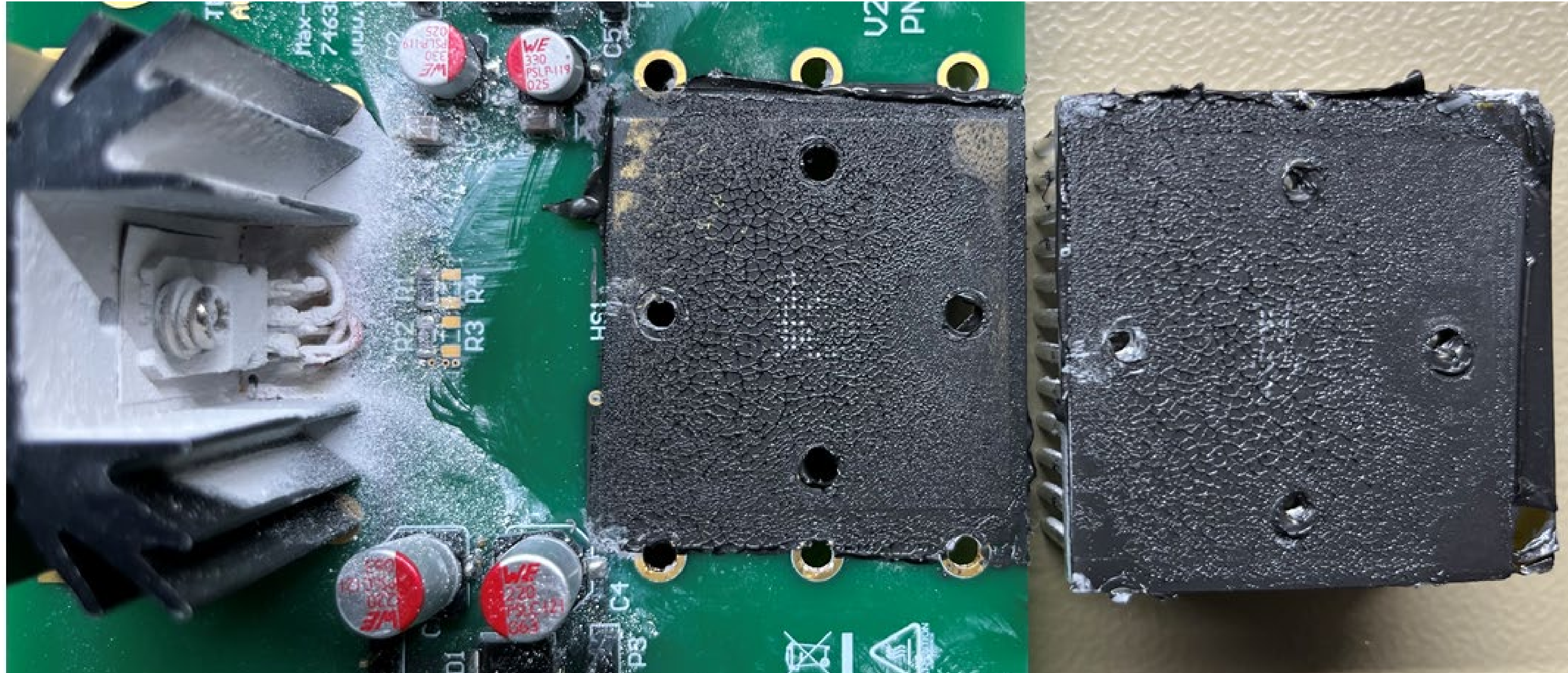
- WE-PCM **402150101020**
- Phase change material



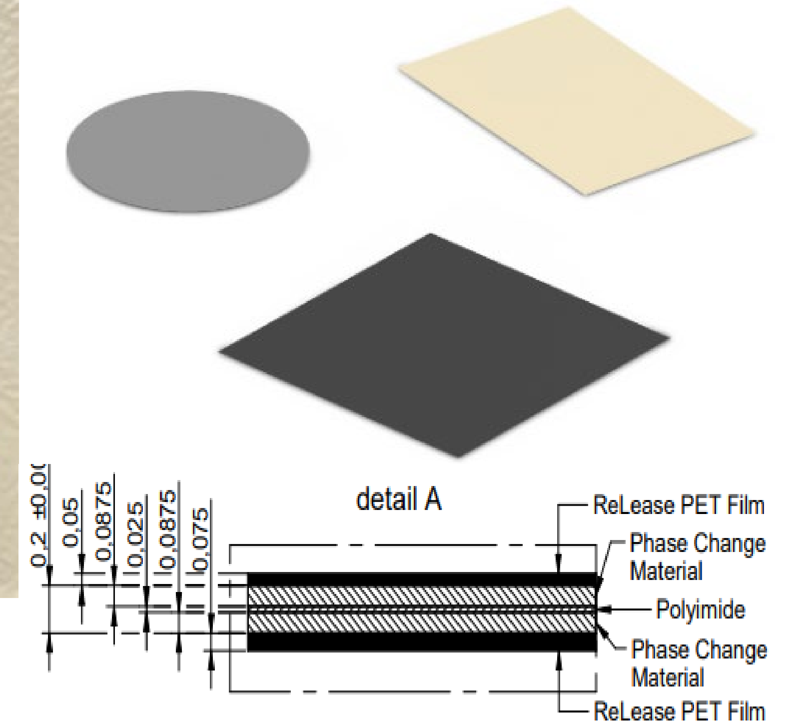


THERMAL DEMO PCB

Measurement with Screwed Heatsink + WE-PCM



- WE-PCM **402150101020**
- Phase change material
- Phase change temp=60°



THERMAL DEMO PCB

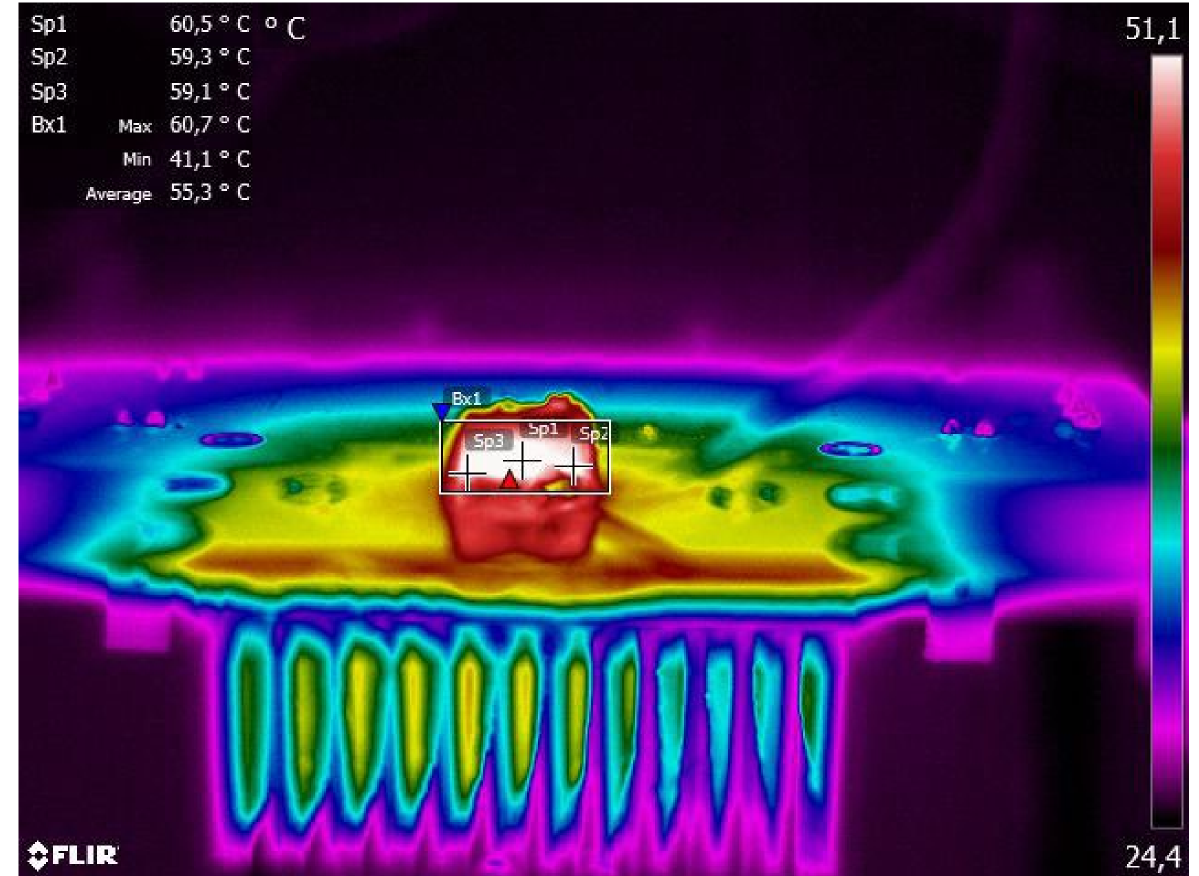
Measurement with Strapped Heatsink + **Thermal Paste**

- Calculated Temp is nearly same as with 0,5mm TIM = **53°C**

$$R_{th-paste} = \frac{l}{\lambda \cdot A} = \frac{0{,}0002m}{6{,}5\frac{W}{m \cdot K} \cdot (0{,}04m \cdot 0{,}04m)} = 0{,}02\frac{K}{W}$$

- Measurement result with ICKS404020 heatsink@**3,3W** = **61°C**

- **12°C** difference

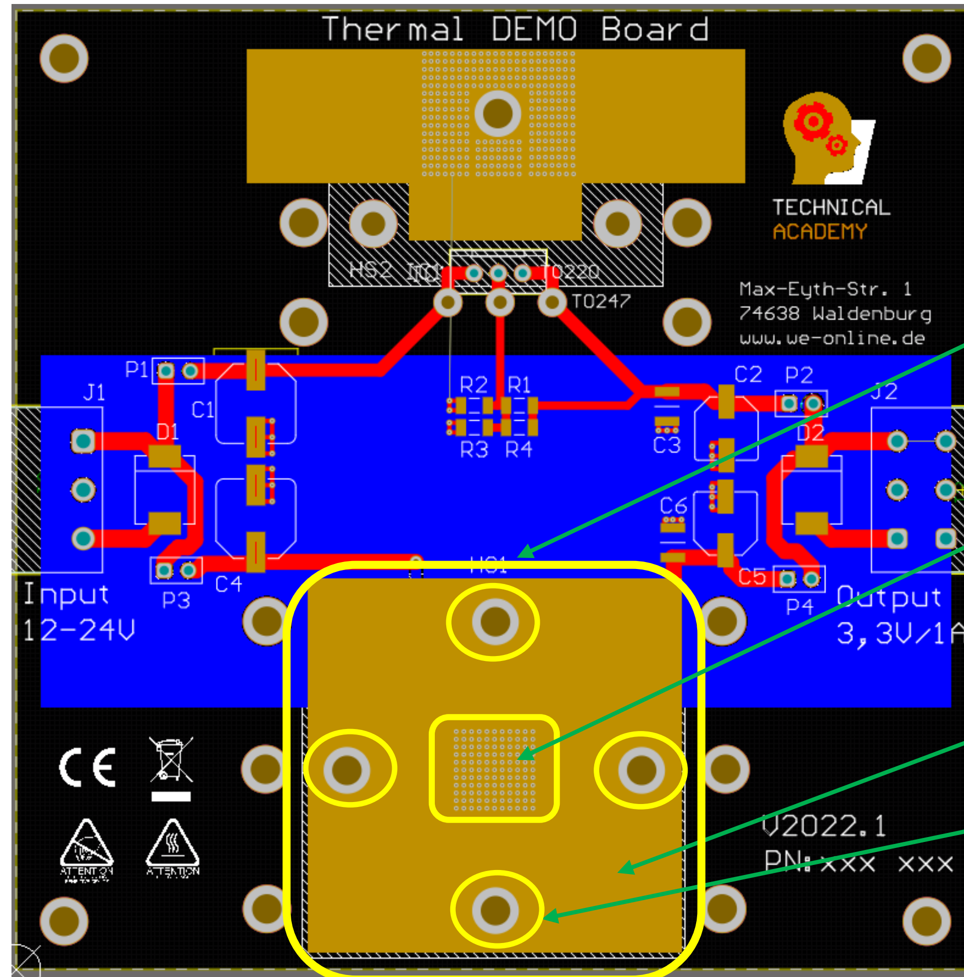


WE

THERMAL DEMO PCB

Where does the deviation come from?

- Horizontal thermal resistance of the copper plane, solder, holes and vertical contact resistance was not taken into account.



Used heatsink is a bit bigger than the copper array(2mm LxW)

Solder paste **vertical** Rth between D2Pack and copper on Bottom

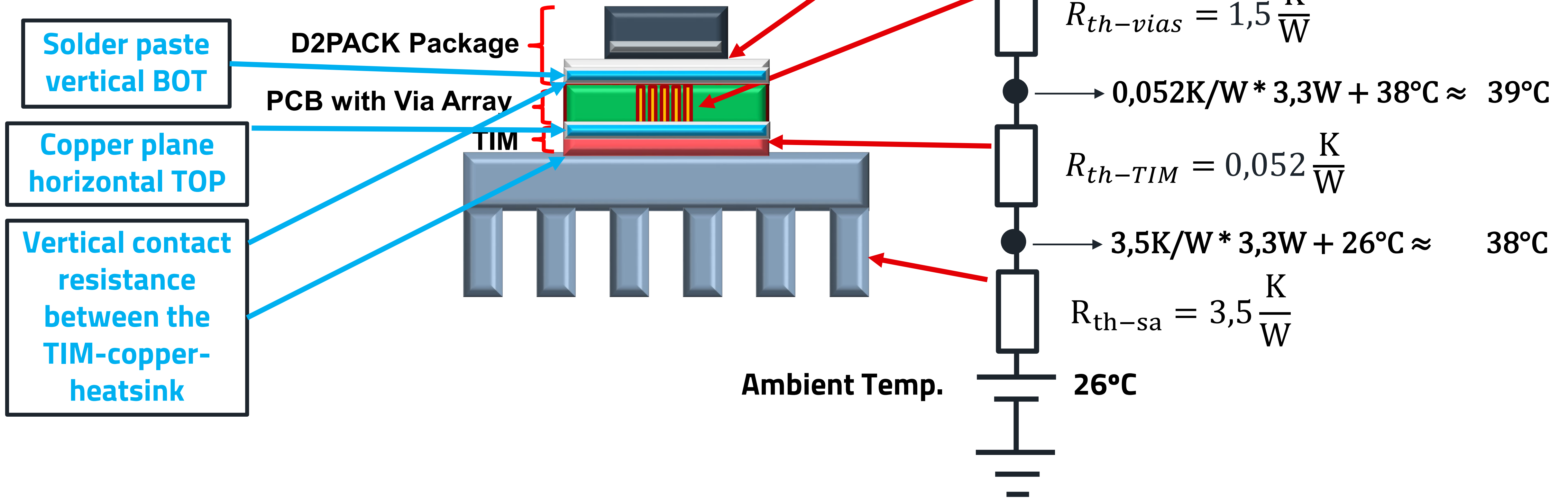
Copper **horizontal** Rth

Mounting Holes

THERMAL DEMO PCB

Missing Thermal Resistance

- $\Delta T \approx 12K@3{,}3W \approx \mathbf{3,5}\,\frac{K}{W}$



THERMAL DEMO PCB

Thermal Resistance of Solder on Bottom Side

- Calculation of the thermal resistance of the solder on bottom side after reflow:

$$R_{\lambda,\text{solder}} = \frac{\ell}{\lambda_{\text{solder}} \cdot A} = \frac{0.15\text{mm}}{60\text{W} \cdot \text{m}^{-1} \cdot \text{K}^{-1} \cdot 81\text{mm}^2} = 0.03\text{K} \cdot \text{W}^{-1}$$

- Parameters:
  - ℓ = Solder thickness after reflow
  - A = Contact surface area of D²PAK case
  - λ_{solder} = Thermal conductivity of solder @ 25°C

Solder	Thermal Conductivity (W/mK) @25°C	Melt Temperature (°C)
AuSi (97/3)	27	363
AuGe (88/12)	44	356
AuSn (80/20)	57	280
PbIn (80/20)	17	280 (liq.)/270 (sol.)
SnCu (99.3/0.7)	65	227
SnCuNi (Sn100C)	64	227
SnAg (96.5/3.5)	78	221
SAC (SnAgCu) 95.6Sn/3.5Ag/0.9Cu 95.5Sn/3.8Ag/0.7Cu	~60	217 Eutectic ~220-217
SnAgCuSb (96.2/2.5/0.8/0.5)	57	215-217
PbIn (50/50)	22	209 (liq.)/180 (sol.)
SnPb (63/37)	50	183
BiSn	19	138

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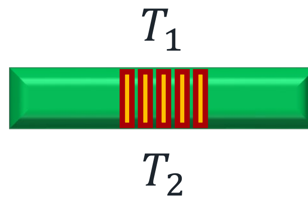
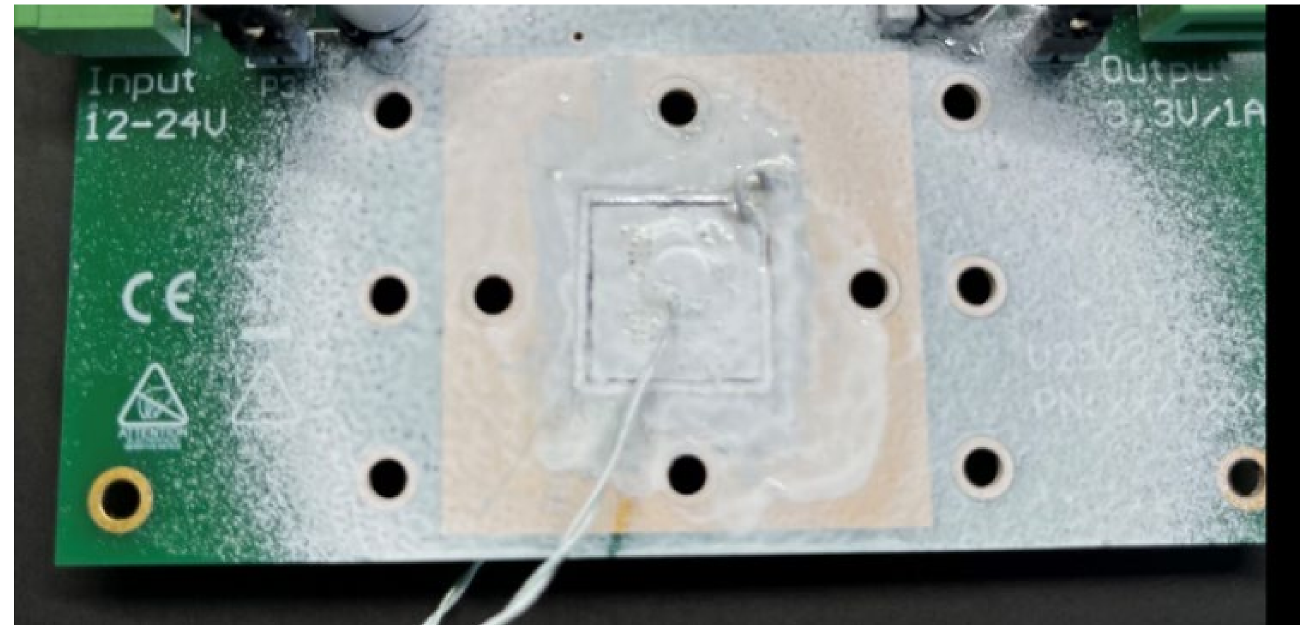
Measurement of Thermal Resistance of Via Array

- Measurement of the temperature difference through the thermal vias
- Calculation resulted in $R_{\lambda,\text{top-bot,calc}} = 1.5\,\frac{K}{W}$

$$R_{\lambda,\text{top-bot,meas}} = \frac{T_1 - T_2}{P_{\text{loss}}} = \frac{63.5°\text{C} - 61°\text{C}}{1\text{W}} = 2.5\,\frac{K}{W}$$

- Deviation due to missing heatsink





WE

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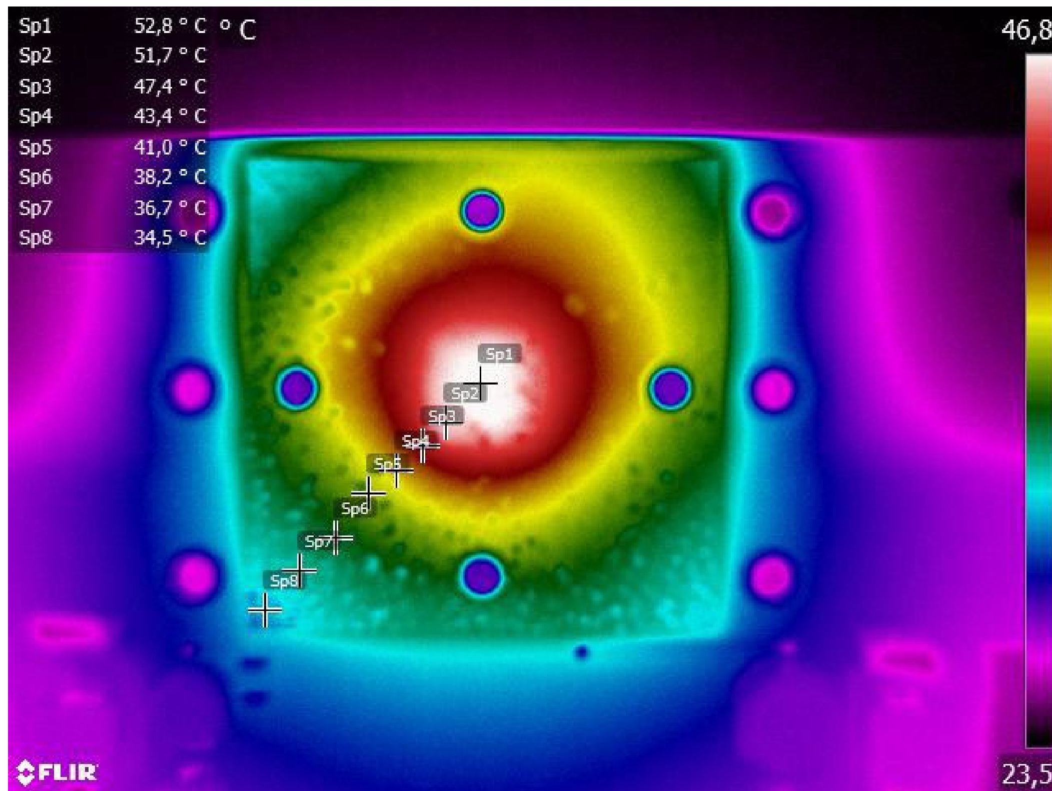
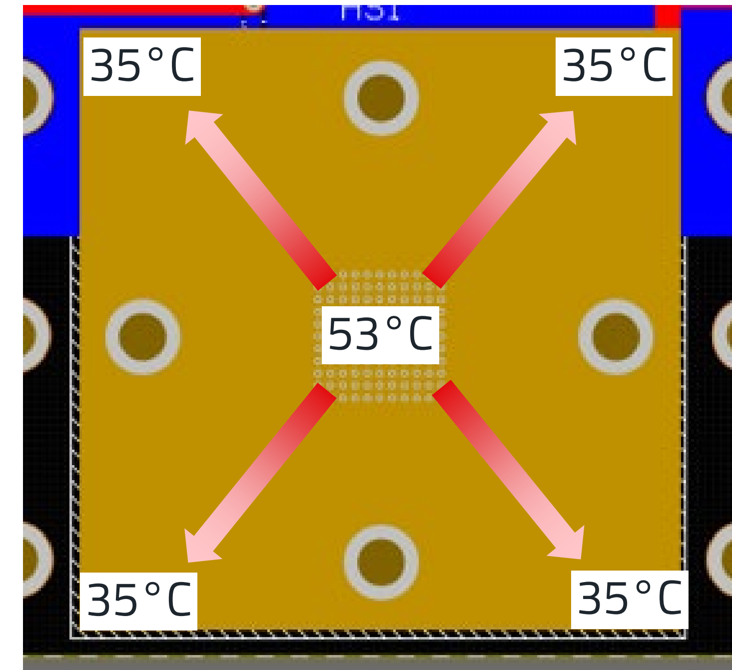
Measurement of Copper Plane Temperature Distribution

- Measurement of the temperature distribution inside the 40×40mm²/35µm copper plane (without heatsink)
- Temperature difference between the center and the edges @ $P_{\text{loss}} = 1\text{W}$: $\Delta T = 18\text{K}$



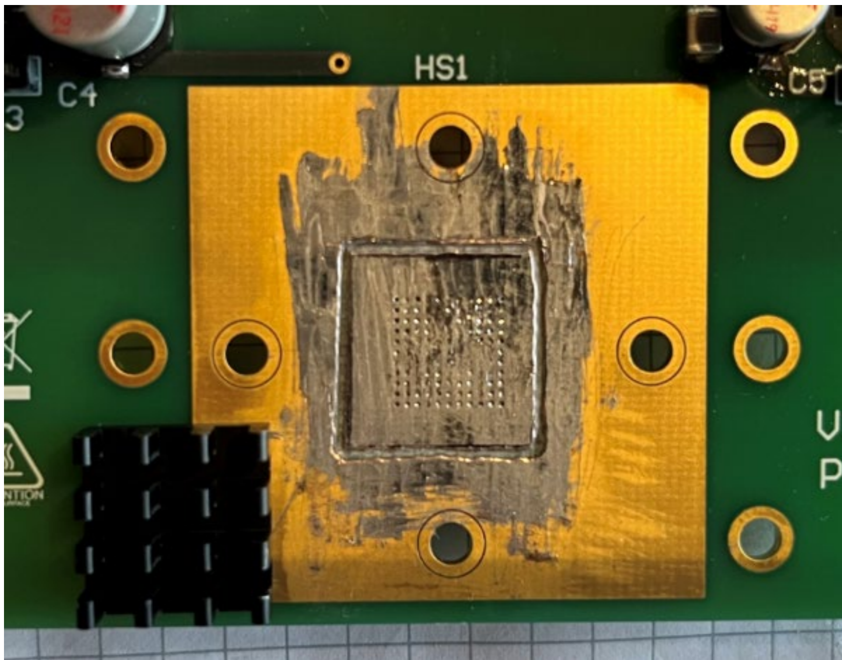


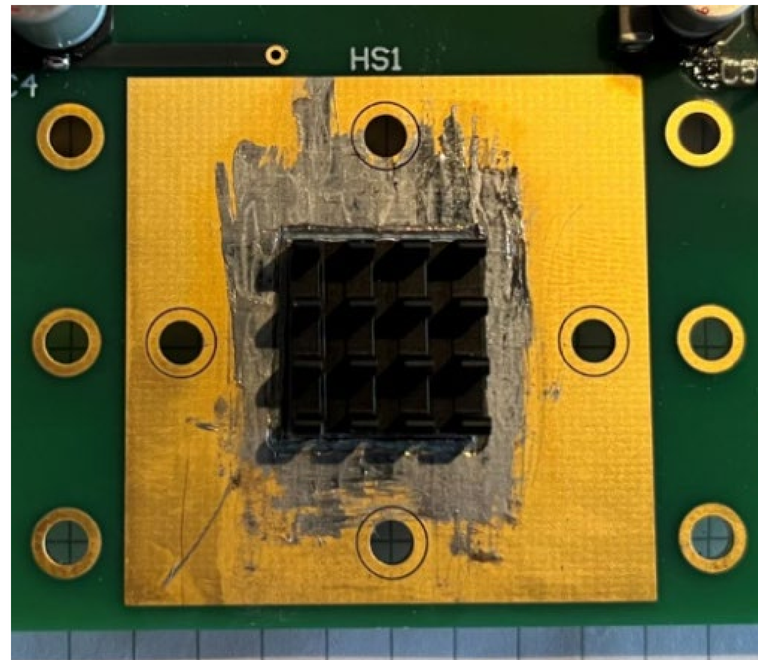
THERMAL DEMO PCB

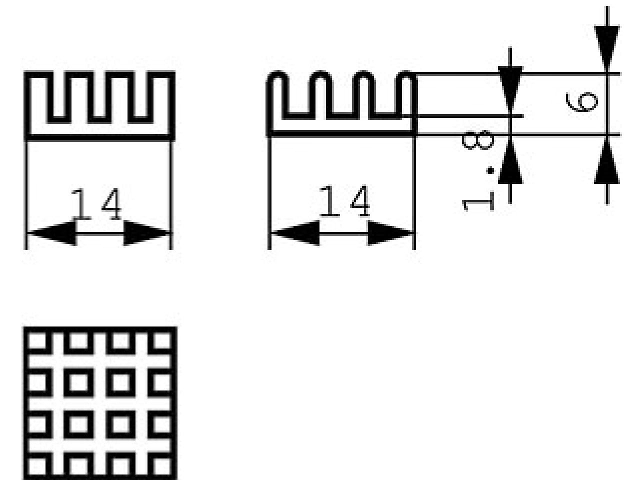
Effect of Smaller Copper Plane + Smaller Heatsink

- Reduced top copper area ($14 \times 14 mm^2$), with **WE-PCM** and fitting heatsink (ICK BGA 14 X 14, $30 K \cdot W^{-1}$)

$$R_{\lambda,\mathrm{TIM}} = \frac{\ell}{\lambda_{\mathrm{TIM}} \cdot A} = \frac{0.2\mathrm{mm}}{5\mathrm{W} \cdot \mathrm{m}^{-1} \cdot \mathrm{K}^{-1} \cdot 196\mathrm{mm}^2} = 0.2\mathrm{K} \cdot \mathrm{W}^{-1}$$



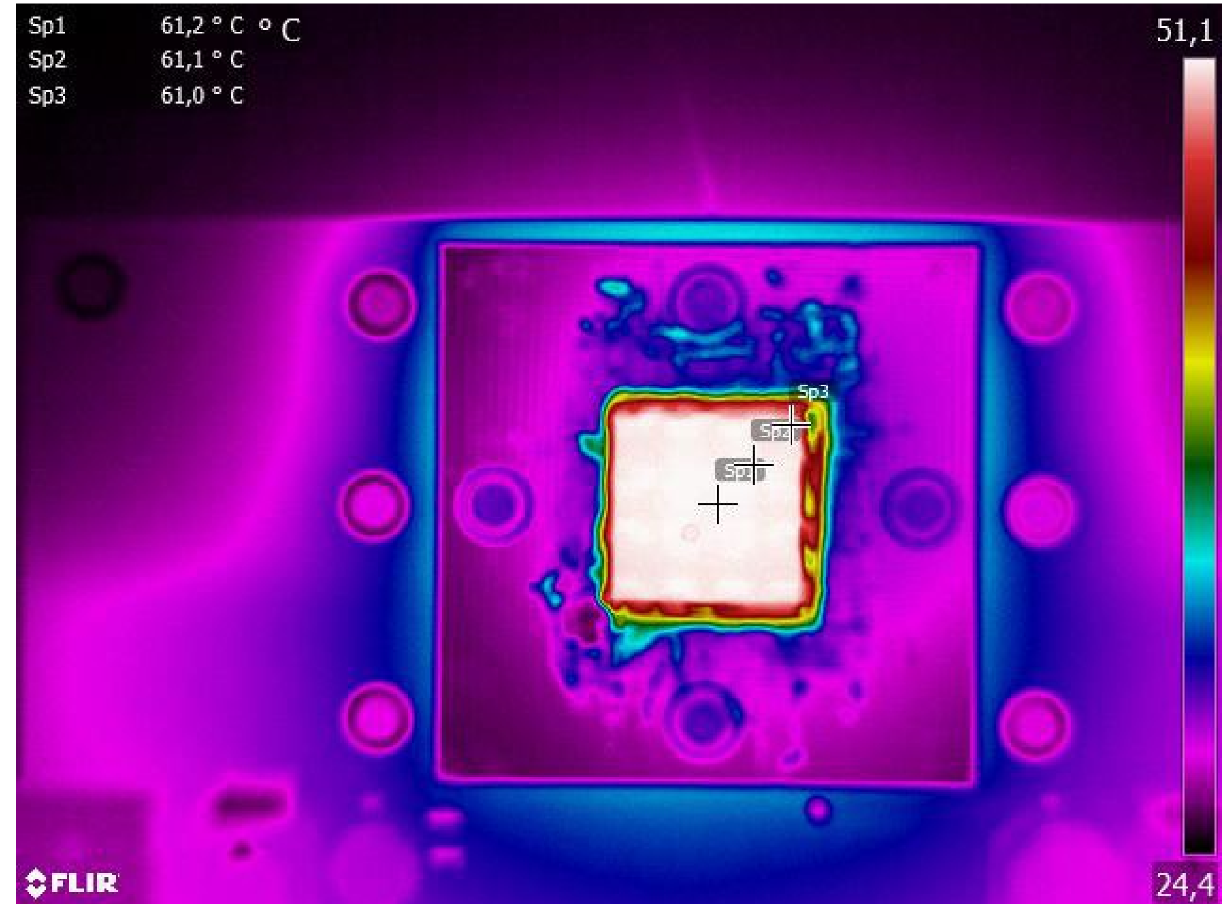




THERMAL DEMO PCB

Effect of Smaller Copper Plane + Smaller Heatsink + WE-PCM

- Measured temperature at LDO: 62.5°C
- Measured temperature at heatsink: 61.2°C
- Calculated temperature at LDO: 60.7°C
- Better agreement between calculation and measurement
- **1.3K** temperature drop across the WE-PCM



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Comparison Calculation vs. Measurement

- TIM contact pressure is critical
- Copper plane area in relationship to via array has a big influence
- Holes/cut outs in the copper plane should be minimized
- Via array Rth calculation is close to reality
- Via arrays only working proper with an attached heatsink on the other side of the PCB

THERMAL DEMO PCB

Conclusion

- The better the performance of the heatsink (=low Rth), the more influence the TIMs have
- The thickness of a TIM is often more critical than the thermal conductivity of the material
- The thermal resistance of the surface between the materials are most criticall
- Better use many small vias then few big vias!
- Plated or filled vias are very expensive to get, better try to stay with standard!

Questions

& Answers

We are here for you now!
Ask us directly via our chat or via E-Mail.

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