

Development of Ultra-Multilayer Printed Circuit Board

Yasuyuki Shinbo

Using the multilayer and characteristic impedance control technologies cultivated in the field of telecommunications, OKI Printed Circuits Co., Ltd. has been expanding to other ultra-multilayer board markets. In particular, the work with semiconductor test boards has led to the mass production of 50-layer class boards.

However, in recent years, there has been an increased demand on the wiring capacity of test boards to accommodate increases in memory while at the same time keeping the board size (thickness) within specification for incorporation into testing devices. To respond to these requirements with traditional board structure, 60 layers or more would be necessary, which is not possible with current manufacturing technologies. It is difficult to manufacture printed circuit boards using typical methods when the number of layers exceeds 40 layers. Therefore, it was urgent to develop an ultra-multilayer printed circuit board that can accommodate multi-wiring.

This article introduces the technical development that went in to realizing an 80-layer ultra-multilayer printed circuit board, which meets the market demand for a “semiconductor test board supporting memory increases”. The achievement of the ultra-multilayer board was accomplished by approaching the development from the perspective of ① manufacturing, ② board material and ③ design. Moreover, use of the developed technologies is not limited to semiconductor test boards, but they can be expanded to the telecommunications market where there is progression in high-speed, high-density boards.

Need for development of an ultra-multilayer printed circuit board

Printed circuit boards are, in general, components upon which electronic parts are mounted and circuits are formed. The structures of these printed circuit boards are sometimes utilized for special purposes such as semiconductor test boards that serve as test jigs in the semiconductor manufacturing process. In particular, the probe card (**Photo 1**) presented in this article is a jig used to test circuits (wafer test) that have been formed on the wafer while still in the manufacturing stage. On a

probe card, pins called probes are mounted on the board surface instead of electronic components. Recently, there has been heightened demand for probe cards with high-density wiring due to the increase in test circuitry resulting from expanded wafer diameters and miniaturized chips. This is especially true for memory testers.

In contrast to the overall size of the printed circuit board market, the market for semiconductor test boards is by no means large. However, each technical element used for the development of the ultra-multilayer board and presented in this article serves as a core technology for all printed circuit boards. With further cultivation, the technologies can be applied to other products (circuit boards) besides semiconductor test boards. That is, the following can be expected.

1. Market increase through deployment of technologies to other products.
2. Technical superiority.

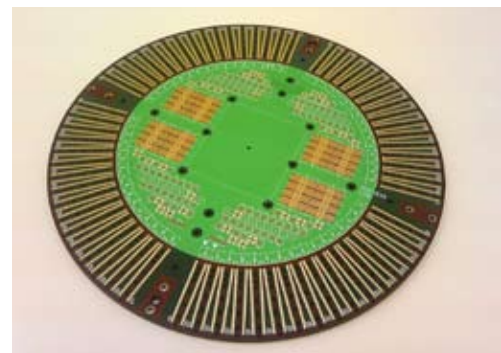


Photo 1. Probe Card

Development of manufacturing technology for ultra-multilayer printed circuit board

Opposed to a typical 1.6mm thick, 12-layer printed circuit board, the ultra-multilayer board targeted for development is to be 6.3mm thick with 80 layers. For this, the following technical issues in manufacturing needed to be resolved.

(1) Laminating technology

A technique was needed to suppress the layer shifts that occur as layers are laminated. The drilling process

for the holes used to align the layers was reviewed. The cushioning material used during lamination was also reviewed. As a result, maximum shift that was once greater than $150\mu\text{m}$ was reduced to under $60\mu\text{m}$. Furthermore, electrical shorts between the holes and adjacent internal wirings were now avoidable.

(2) Drilling technology

The ultra-multilayer board required a drilling technique that produced holes with precise positioning, cross-section and high aspect ratio. When drilling through a thick board with a small diameter drill, the drill may become bent leading to a shift in the hole's position or a broken drill. To prevent such events from occurring, different drilling techniques were developed including the use of several drills with varying blade length and drilling from both sides of the board. The result was an improvement in the position accuracy of the holes from a $\pm 100\mu\text{m}$ deviation down to $\pm 60\mu\text{m}$. Electrical shorts between the holes and adjacent internal wirings were also eliminated.

(3) Plating technology

High aspect ratio plating became necessary to cope with the thicker boards and smaller diameter holes. At the time of introducing new electroplating equipment, we simulated current distribution in the plating tank and developed the plating equipment. Additionally, by introducing new plating solution and optimizing plating conditions, we were able to meet an aspect ratio of 30. As far as electrolytic plating is concerned, an industry leading throwing power (ratio of bore plating thickness to surface plating thickness) of more than 50% was achieved for a board with a thickness of 6.3mm and hole diameter of $\text{Ø}0.20\text{mm}$ (aspect ratio of about 32).

(4) Characteristic impedance control technology

For high-speed, low-loss transmission, a technology for characteristic impedance control is required. Main factors that can be controlled with manufacturing technologies are ① wiring width and ② interlayer insulation thickness. Each requires precision control. ① wiring width is largely affected by the manufacturing equipment used to form the wirings (patterns). As for ② interlayer insulation thickness, the variation in thickness caused by the use of various board materials needs to be controlled. Simultaneously, expected finished thickness is simulated for each material, and the result is fed back to the setting of the wiring width so that the target value can be achieved. We obtained a more accurate impedance control characteristics by building our own simulator around a database containing information such as interlayer insulation thickness of

different board materials after lamination and dielectric constants ¹⁾.

Combining these manufacturing techniques, we were able to support 0.5mm pitch BGA with 4.8mm thick board using $\text{Ø}0.2\text{mm}$ drill, support 0.65mm pitch BGA with 6.3mm thick board using $\text{Ø}0.25\text{mm}$ drill and mass-produce 6.3mm thick 50-layer class boards (**Photo 2**). However, these manufacturing techniques are extensions of conventional technologies, and even with their combination, a limit can be seen due to the generally available board materials and design specifications. For the probe card, in addition to the 6.3mm thickness and $\text{Ø}480\text{mm}$ size requirement, there are constraints on the direct current resistance of the wiring and constraints on characteristic impedance control. This limits the number of layers that can be achieved to about 50 layers. In order to achieve the target of an 80-layer ultra-multilayer board, the manufacturing technologies described above are inadequate. Approaches from new perspectives are necessary such as development of an ultra-thin board material capable of higher multi-layering and design techniques to increase wiring capacity while reducing layers.

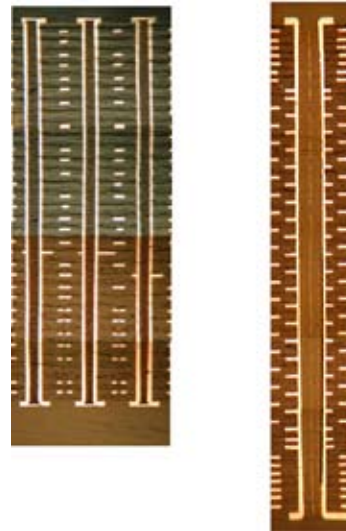


Photo 2. Board thickness
4.8mm, 0.5mm pitch

Board thickness
6.3mm, 58 layers

Developing board materials for the ultra-multilayer printed circuit board

The use of an ultra-thin board material will be required to achieve a higher level of multi-layering, but as interlayer insulation gets thinner, wiring width of the characteristic impedance becomes narrower. When wiring width becomes narrower, direct current resistance rises and

attenuation (loss) becomes larger.

The use of materials with low dielectric constants is effective in resolving these adverse effects. A composite material made of glass cloth and epoxy resin known as FR-4 is commonly used for printed circuit boards. The dielectric constant of FR-4 is about 3.8 to 4.7. To match direct current resistance and characteristic impedance with these materials and 35 μm thick copper foil, line width of 100 μm and layer thickness of 100 μm would be required. There are materials that have dielectric constants below 3.0 (PPE and PTFE resin), but their cost is high and workability poor making them unviable solutions. If an improvement can be made to bring down the dielectric constant of a FR-4 material below 3.5, wiring width can be maintained and layer thickness can be reduced. Therefore, to take advantage of the low cost and utilization of existing fabrication process, a study was conducted to reduce the dielectric constant of a FR-4 based board.

Conventional FR-4 is a composite material made from epoxy resin with a dielectric constant of 3.5 and glass cloth called e-glass with a dielectric constant of 6.0. Hence, the dielectric constant of FR-4 was limited to between 3.8 and 4.7. To reduce the dielectric constant of FR-4, the dielectric constant of the glass cloth must be reduced.

Therefore, development of a board material was undertaken by adopting a glass cloth with low dielectric constant, which is still rare, and changing the resin to glass cloth ratio.

By utilizing the low dielectric constant material, direct current resistance and characteristic impedance control were satisfactory even with thickness below 100 μm .

Developing design techniques for the ultra-multilayer printed circuit board

Even if an ultra-thin board material is adopted, there are limits due to the constraints in wiring width and manufacturing equipment. To suppress or reduce the number of board layers, it was necessary to approach the problem from a different perspective. The solution was looked for in the design techniques.

On a printed circuit board, structurally the wiring on the same layer cannot be crossed. When cross wiring is required, the crossing wire is passed through a hole to another layer. The number of layers can be suppressed if a design technique to cleverly cross wires can be developed.

Additionally, characteristic impedance control requires GND layers that act as reference layers to be placed both above and below the wiring layer. If wiring layers are

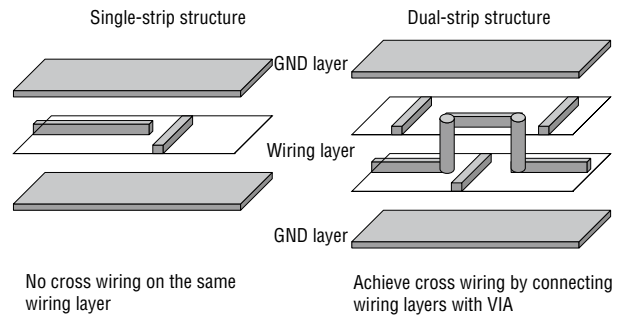


Figure 1. Cross Wiring Diagram Using Dual-strip Structure

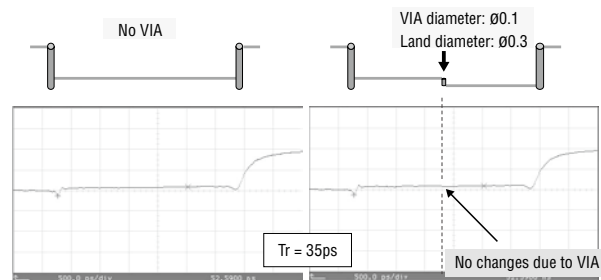


Figure 2. Characteristic Impedance Changes Due to Micro-VIA (Measured by Time Domain Reflection (TDR))



Photo 3. Laser Processed Ultra-small Diameter VIA

increased using a typical single-strip structure, an equal number of GND layers are also required. As far as overall number of layers is concerned, there is no efficient way to only increase the wiring layers. If a design technique can be developed, whereby only the wiring layers can efficiently be increased, the relative number of GND layers can be reduced.

1) Suppressing the number of layers (achieving cross wiring)

With a simple single-strip structure, there is only one wiring layer sandwiched between GND layers and wiring crossing is not structurally possible. If a dual-strip structure is used, wiring layer is increased to two layers between GND layers, and dimensional crossing is possible using VIA to connect the wiring layers (Figure 1).

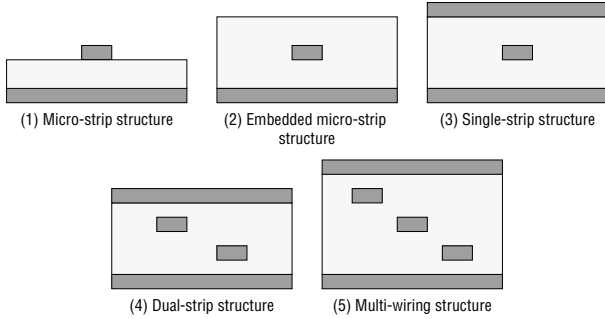


Figure 3. Structure of Characteristic Impedance Control Board

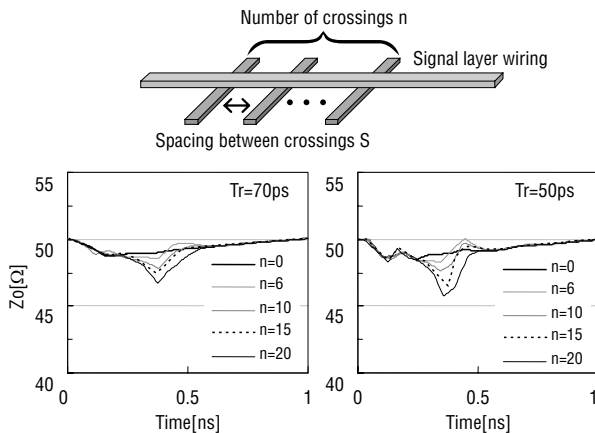


Figure 4. Characteristic Impedance Variations Due to Number of Crossings (TDR simulation response)

However, maintaining characteristic impedance control and transmission properties of the transmission path that includes the VIA becomes an issue.

Therefore, we checked the changes in characteristic impedance and transmission properties associated with the size of VIA and land diameters then optimized the design specifications. As a result, when hole diameter is 0.1mm and land diameter less than 0.3mm, variance in characteristic impedance was held to within 3% (Figure 2)²⁾.

Such fine machining of small diameter VIA was achieved using the UV-YAG laser machine (Photo 3).

(2) Reducing the number of layers (possibility of multi-wiring structure)

Besides micro-strip structures and single-strip structures, we are currently supporting characteristic impedance control on dual-strip structures (Figure 3). In this case, a design technique is needed to reduce the impact of crosstalk.



Photo 4. Cross-sectional View of an 80-layer Board

In developing the ultra-multilayer board, reducing the ratio of reference layers and increasing ratio of wiring layers will be the key to the efficient use of the total number of layers. To achieve this we are working on a structure that incorporates three wiring layers between reference layers. With such a structure, preventing characteristic impedance variations, crosstalk and other property changes caused by the effects of adjacent signals are extremely difficult. Therefore, to ensure the electrical properties, design criteria are established through simulations and measurements (Figure 4)³⁾.

A relative increase in the wiring layer can be expected through the establishment of a multi-wiring structure. Furthermore, even though each layer is made thinner, the middle layer of the three wiring layers will have adequate spacing from the GND reference layer to prevent drops in characteristic impedance and allow for wider wiring width.

These synergistic effects will allow more for wiring layers compared to the single-strip structure.

An 80-layer prototype employing the multi-wiring structure was exhibited at the 2009 JPCA show (Photo 4).

Our future actions include establishing design techniques for the multi-wiring structure and commercialization.

Conclusion

The feasibility of an 80-layer ultra-multilayer printed circuit board has become apparent with the combination of technical elements presented in this article. The application of these technologies is not limited to semiconductor test boards, and we plan to use them in other products to expand the market. Furthermore, we are aiming to establish technical superiority with these technologies, and transforming ourselves from an order-type business to a proposal-type business (total board solution) providing proposal of board structure, various simulations, design, manufacturing and implementation. ◆◆

References

- 1) Isao Kanada, et al., "Impedance Control Board", Denshi Zairyou, October 2001 Issue, pp.96-100, 2001
- 2) Takahiro Yagi, et al., "Layer Control Methods of High-speed High-density Multilayer Printed Circuit Boards", 22nd Japan Institute of Electronics Packaging Lecture Convention, 17A-06, 2008
- 3) Jun Kamiya, et al., "A Study on Signal Capacity of Ultra-multilayer Printed Circuit Boards", 23rd Japan Institute of Electronics Packaging Lecture Convention, 12B-05, 2009

Authors

Yasuyuki Shinbo, Prototype Development Team, Product Development Department, Engineering Division, OKI Printed Circuits Co., Ltd.